UC1860 – NEW IC CONTROLS RESONANT MODE POWER CIRCUITS

Larry Wofford
Unitrode Integrated Circuits Corporation
7 Continental Boulevard, Merrimack, NH 03054

ABSTRACT

A new integrated circuit, the UC1860, is introduced. Its prime purpose is to provide the control function in resonant mode power supplies operating at frequencies up to 3 MHz. A frequency modulated, fixed on-time control scheme is implemented. Additional features include a programmable under voltage lockout circuit and a programmable soft-start/hic-up circuit.

BACKGROUND

For years, rumblings of the coming (or perhaps more correctly, reapplication) of resonance as a useful tool in the power control world have been growing progressively louder. Being a recognized manufacturer of pulse width modulation control ICs, some of these noises have been focused directly at Unitrode Integrated Circuits Corporation. Receiving, conditioning, filtering, and discriminating these signals, however, has been somewhat of a frustrating chore. Information indeed has been sought to aid in the definition of chip to perform all required resonant mode control functions. Too often the response was an inverse request: "Tell me what the chip looks like and then I can design my power supply." The immaturity of the technology has naturally made the sharing of information somewhat less than authorative. Finally there came a day when a best guess architecture and specification goals list had to be embraced as presumed gospel. It is that choice that has resulted in the chip to be discussed in this paper.

This paper, then, will describe the UC1860 with respect to its architecture and the specific features and performance of some of the sections. The chip is intended to fully implement all features necessary for the control function in a resonant mode power supply.

BLOCK DIAGRAM

The UC1860 control IC is designed to control power conversion circuits requiring frequency modulated fixed pulse widths such as resonant or quasi-resonant mode power supplies (figure 1).

The central section of the system is composed of 6 main blocks. A precision reference is provided for the error amplifier. These serve as the basis to control a variable frequency oscillator (VFO) which in turn triggers a one-shot. The programmable one-shot determines the output pulse width of the output drivers which are specifically designed to drive power mosfet gates. Finally a toggle flip flop steers the one-shot signal to the appropriate output stage.

In a typical application, the error amplifier is used to compare power supply output voltage to the internal reference. The error amplifier is also used as a gain block with which to compensate the overall power supply control loop. The output of the amplifier is resistively coupled to the VFO to control frequency. VFO frequency is directly proportional to error amplifier output voltage. Output pulse width is selected by an external RC pair. Pulses are sequenced to the output pins to activate the switches in the power circuit.

On chip peripheral housekeeping blocks are under voltage lockout (UVLO), fault management, and start-up/restart sequencing. The UVLO block forces the chip to wake up in a consistent and intelligent state when power is applied.

An additional uncommitted open collector comparator is on chip. This comparator can be used to accomplish a host of user defined functions.

ERROR AMPLIFIER

Understanding the chip requires considering the blocks one by one. The first block of interest in the main control section of the chip is the error amplifier. This amplifier is a high bandwidth, low offset, clamped swing design (figure 2). The non-inverting input is internally connected to a resistive divider from the reference voltage. While the divider is set for 3V, the combination of offset voltage and divider accuracy is specified as a ratio of the reference voltage. This allows an external reference of greater accuracy to drive the chip reference for better system accuracy.

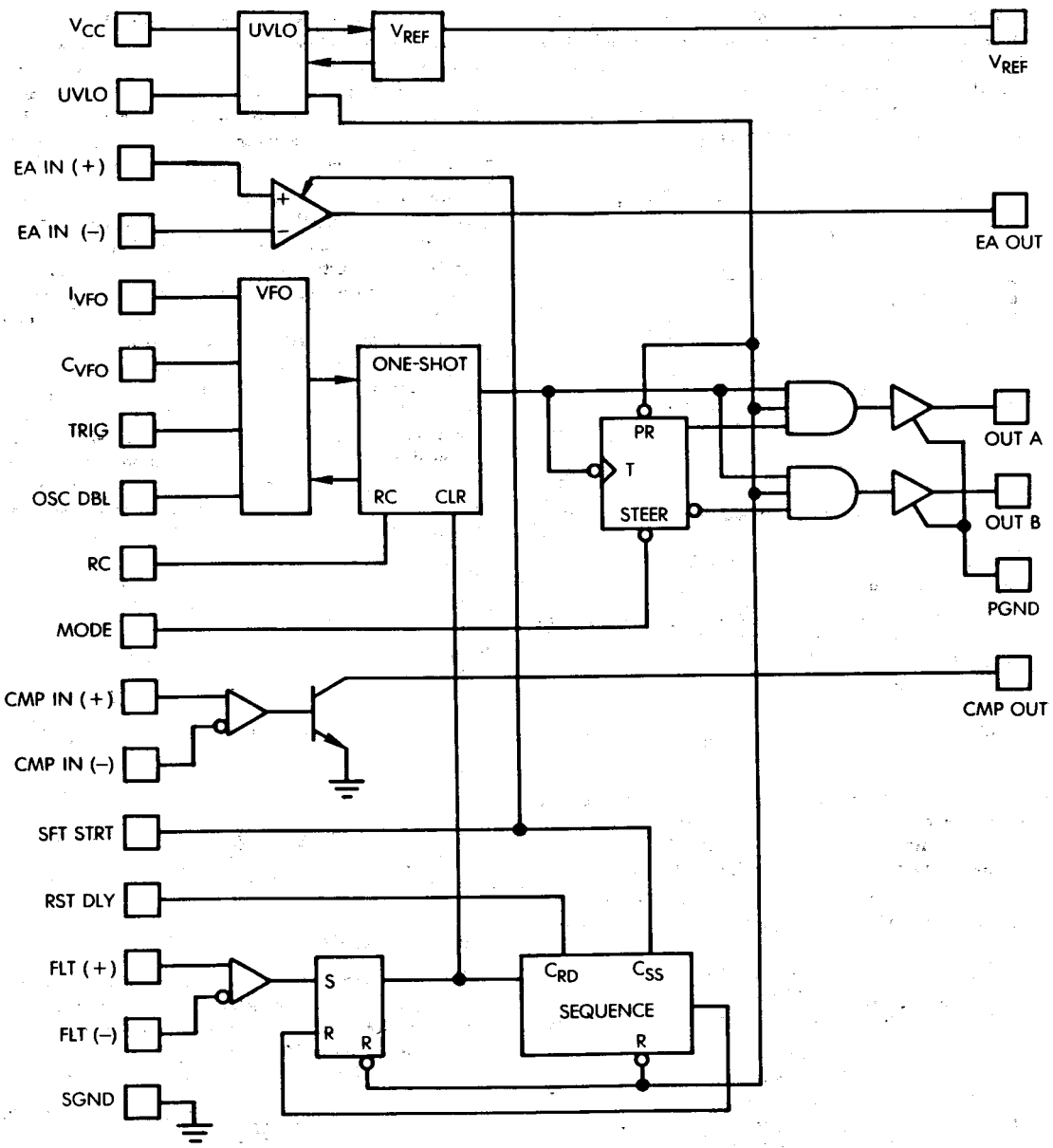


FIGURE 1. UC1860 SIMPLIFIED BLOCK DIAGRAM.

With three gain blocks (transconductance, transresistance, and voltage), the amplifier is compensated by two capacitors. The first feeds forward around the first stage directly to the second stage. This is because the first stage is designed for high gain and low offset but has poor high frequency characteristics. The second capacitor, the main

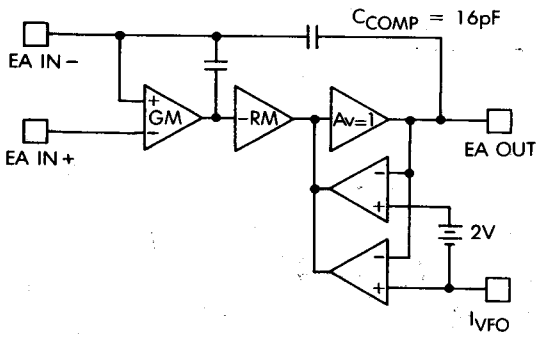


FIGURE 2. ERROR AMPLIFIER WITH OUTPUT SWING CLAMPS.

compensation capacitor, is connected from the output to the inverting input.

Amplifier bandwidth is controlled by the impedance seen by the inverting input terminal. To the first order, bandwidth in a simple feedback configuration is easily calculated by the equation

$$fo = \frac{1}{2\pi(Rin)(Ccomp)} \quad \text{(eq. 1)}$$

where Ccomp is the internal 16 pF compensation capacitor that appears between the output and inverting input pins. The amplifier is unity gain stable for unity gain bandwidths less than 5 MHz (ie. Rin > 2 kohm).

Higher gain bandwidth products can be obtained by choosing Rin and closed loop gain appropriately. Figure 3

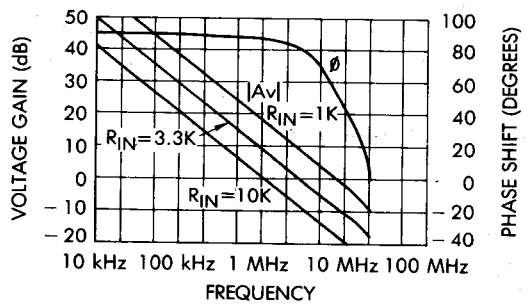


FIGURE 3. ERROR AMPLIFIER FREQUENCY RESPONSE.

shows the gain and phase characteristics of the amplifier for various resistive input impedances. Note that the phase curve is the same at higher frequencies for all three values of Rin shown. This is to be expected, since the higher order poles are internal to the amplifier. The combination of Rin and Ccomp primarily adjust the first pole position leaving higher frequency phase response unchanged.

Since the error amplifier is intended to control the frequency of the VFO, the outputs are clamped to obtain predictable minimum and maximum frequency. Each clamp circuit is actually an independent amplifier that monitors the output of the error amplifier and compares it to a reference. The reference for the lower clamp amplifier is the voltage at the I_{VFO} pin while the upper clamp is 2V higher. If the error amplifier attempts to exceed either of these levels, the appropriate clamp amplifier overrides the third stage of the error amplifier and the output is held at the clamped value. Figure 4 shows a plot of typical input offset voltage as a function of output voltage. In the figure, the horizontal axis is output voltage referenced to the I_{VFO} voltage. Note the sharp edges at the two extremes indicating clamped operation.

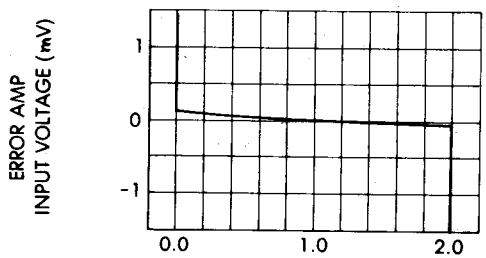


FIGURE 4. ERROR AMPLIFIER DC CHARACTERISTICS.

VARIABLE FREQUENCY OSCILLATOR

The variable frequency oscillator and one-shot functions are closely integrated to achieve the desired operating characteristics. ECL type logic gates and comparators are used to facilitate high frequency (3 MHz) operation. The oscillator will free run at a frequency of approximately

$$f(osc) = \frac{I_{VFO}}{C_{VFO}} \quad \text{(eq. 2)}$$

In no case, however, can the frequency of the oscillator ever exceed the frequency required to support a complete pulse width from the one-shot.

Figure 5 is a detailed block diagram of both the VFO and the one-shot. The frequency of the VFO is proportional

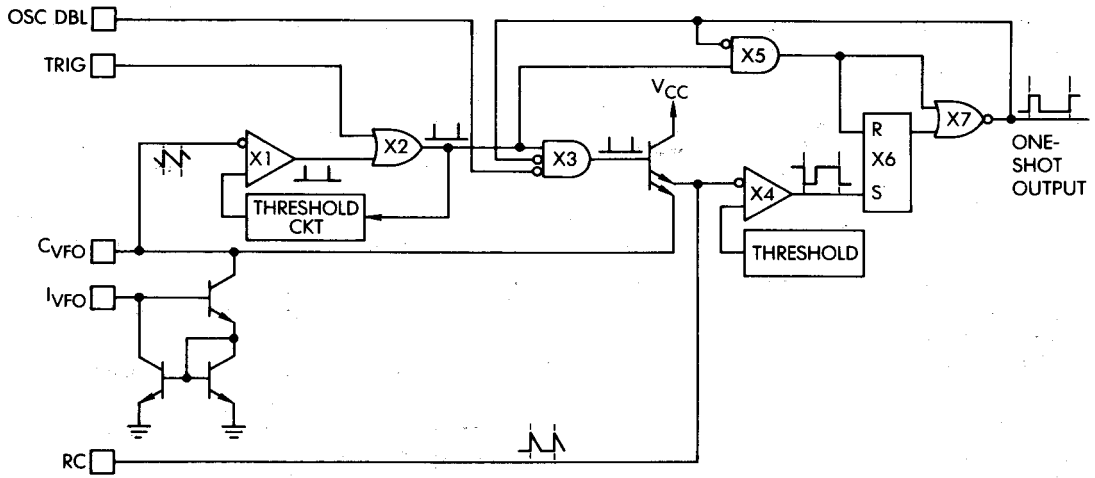


FIGURE 5A. DETAILED BLOCK DIAGRAM OF VFO AND ONE-SHOT.

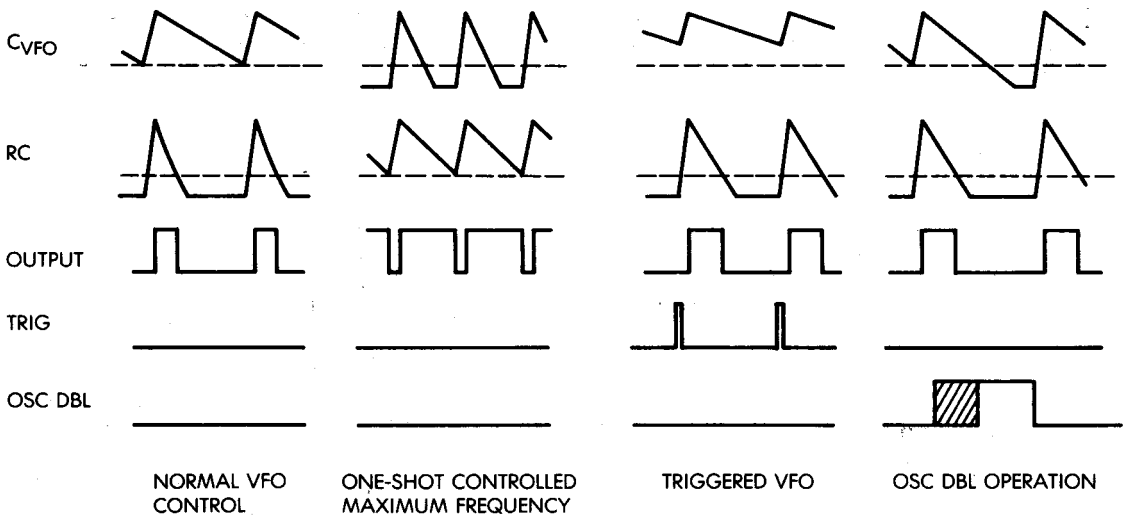


FIGURE 5B. TIMING DIAGRAMS FOR THE VFO AND ONE-SHOT.

to the current into the I_{VFO} pin. This pin is the input to a Wilson style current mirror and exhibits the temperature coefficient of two diodes (approximately 1.4V at 25C with a temperature coefficient of −4mV/C). I_{VFO} current is mirrored about to discharge the timing capacitor, C_{VFO}. Under normal operation, when C_{VFO} discharges to the lower oscillator threshold, hysteretic comparator X1 changes state causing gate X3 to recharge both C_{VFO} and the timing capacitor on the RC pin. Hysteretic comparator X1 then resets and the oscillator recycles.

The trigger (TRIG) and oscillator disable (OSC DBL) inputs can be used to modify the free running characteristics of the oscillator. If TRIG is raised above its threshold during the discharge time of the oscillator, the recharge sequence is immediately executed, resulting in synchronous operation. If, however, OSC DBL is true when either the lower threshold is crossed or the trigger input is received, X1 will change states, but X3 will not recharge the capacitors. They will continue to discharge until a lower retaining level is reached. As soon as OSC DBL returns false, then recharge action occurs immediately.

When the error amplifier output and the oscillator input, I_{VFO} are coupled with a resistor, R_{VFO}, then the oscillator frequency is determined by

$$f(osc) = \frac{V_{EA} - V_{IVFO}}{R_{VFO} * C_{VFO}} \quad \text{(eq. 3)}$$

where V_{EA} is the output voltage of the error amplifier and V_{IVFO} is the input voltage at the IVFO pin. The VFO gain, df/dV_{EA} is

$$\frac{df(osc)}{dV_{EA}} = \frac{1}{R_{VFO} * C_{VFO}} \quad \text{(eq. 4)}$$

With this simple arrangement the maximum frequency is given by

$$f(max) = \frac{2V}{R_{VFO} * C_{VFO}} \quad \text{(eq. 5)}$$

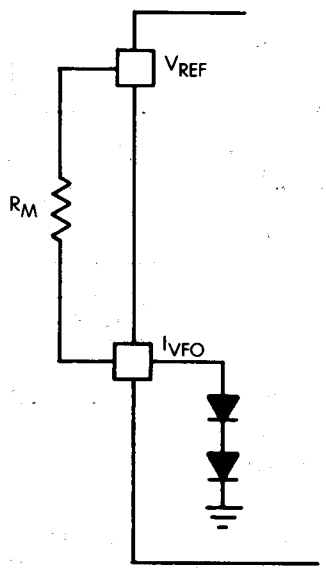
since the error amplifier maximum output is clamped two volts above the IFVO pin. Likewise, the minimum frequency should be zero. There is, however, an obvious limitation of minimum frequency in the input offset voltage of the lower clamp amplifier. Actual minimum frequency is

$$f(min) = \frac{vio}{R_{VFO} * C_{VFO}} \quad \text{(eq. 6)}$$

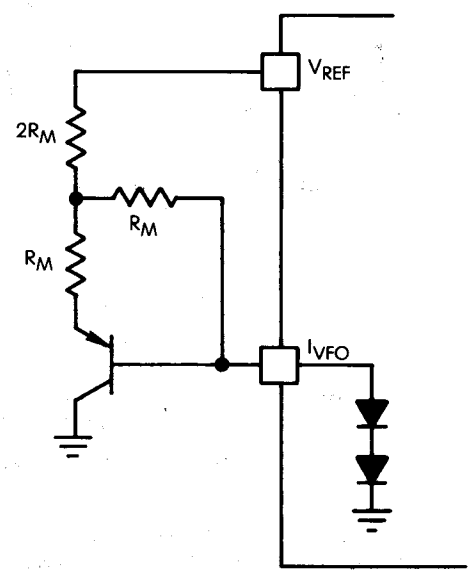
For lower clamp offsets less than 5mV, the maximum range of frequency would be the ratio of 2V and 5mV, or 400 to one.

When a nonzero minimum frequency is desired, an additional current can be injected into the I_{VFO} pin independent from the error amplifier. This can be most easily accomplished by a single resistor from the I_{VFO} pin to V_{REF} (figure 6). In this case, minimum frequency is given by

$$f(min) = \frac{V_{REF} - V_{IVFO}}{R_M * C_{VFO}} \quad \text{(eq. 7)}$$



$$f(min) = \frac{V_{REF} - V_{IVFO}}{R_M * C_{VFO}}$$



$$f(min) = \frac{1V}{R_M * C_{VFO}}$$

FIGURE 6. MINIMUM OSCILLATOR FREQUENCY.

where R_M is the external resistor. It is important to note that this method is not inherently flat over temperature since the voltage at the I_{VFO} pin varies as two diodes. If this variation is unacceptable, three resistors and a pnp transistor can overcome this problem resulting in a minimum frequency of

$$f(min) = \frac{1V}{R_M * C_{VFO}} \quad \text{(eq. 8)}$$

ONE SHOT

The one-shot capacitor at the RC pin is recharged concurrently with C_{VFO}. This sets the output of comparator X4 to a low state allowing S/R latch X6 to be reset. The latch is reset by the signal coming from the output of X2 in the oscillator section via gate X5. The output of X5 also blanks the one-shot off. This is done for accuracy reasons so that the on time is solely a function of the resistive discharge of the RC pin. When both caps have been charged fully, the oscillator circuit drives the output of X2 low allowing both caps to discharge. The timing cap is discharged by an external resistor. The threshold of comparator X4 is set at 80% of the timing capacitor's full charge value. 0.22 time constants are required to reach this threshold making the on time

$$t(on) = 0.22 * RC. \quad \text{(eq. 9)}$$

When the lower threshold is reached, X4 output goes high setting S/R latch, X6, and the one-shot pulse is terminated.

It is important to observe two interactions between the VFO and the one-shot. While the one-shot is high, gate X5 prevents the oscillator from erroneously blanking the output low. The high output also prevents X3 from recharging the timing capacitors in the same way that OSC DBL does. This insures that in no case can the oscillator period (the inverse of eq. 2) be shorter than the time required for the one-shot. In cases where the VFO attempts to overrun the one-shot, the one-shot dominates and establishes maximum frequency.

TOGGLE FLIP FLOP

The output of the one-shot, in addition to limiting the VFO from out running the one-shot, performs two other functions (figure 1). A logic high level from the one-shot causes one or both of the outputs to drive high. The falling edge of the one-shot not only turns the output(s) off, but it triggers the toggle flip flop to change state. The toggle flip flop selects the output to be driven if the output mode control pin is low. If the output pin is high, both toggle outputs are high causing outputs A and B to operate in unison.

OUTPUTS

The output blocks are well suited to driving the active capacitive load presented by power mosfet gates. With this load in mind, they are designed to deliver currents up to 3A in both source and sink directions. Current rise times are in the order of 75A/us. This results in rise and fall times of 50 ns when driving series loads of 10nF and 2.4 ohms (figure 7). Unloaded transitions are 12ns. Of course, cross conducted charge has been minimized within the constraints of high speed design goals.

It is well worth noting that careful attention to low inductance printed circuit board layout along with proper damping and application of schottky clamp diodes are necessary when driving a large capacitive load directly. Disregard for this caution will result in the output/load combination becoming a highly excited tank that will ring and inject current into the chip substrate. Such injection is almost always a sure cause of problems in bipolar ICs.

REFERENCE

The bandgap reference needs little mention since it is a standard, borrowed from many previous designs. Trimmed for precision at wafer probe to 5V, it is specified at 1% tolerance at room temperature with no more than a 2% spread over temperature. While intended as a reference, not a voltage regulator for external use, it has line and load rejection capabilities that will allow it to be used as such for loads under 10mA. A bypass capacitor is required on the reference.

UVLO

The UVLO block (figure 8) consists of three comparators arranged to allow for flexibility of application. They can accommodate off-line, DC to DC, and even operation from a 5V supply.

The first of the three comparators monitors V_{cc}. It has hysteretic thresholds of 17 and 10V. This spread is ideally suited to off-line applications. The output of the V_{cc} comparator is an emitter follower that can go no higher than approximately 6.5V.

The second comparator monitors the UVLO pin which is resistively driven from the output of the V_{cc} comparator. This comparator turns the reference on or off, controlling the bias in the chip. When the reference is off, I_{cc} is less than 0.5mA. After operation commences, I_{cc} increased to approximately 35mA. The thresholds of this second comparator are 4.0 and 3.5V.

The third comparator monitors V_{REF} and has a threshold of 4.5V. If either this comparator or the second has a low output, then the chip is disabled and reset. When this is the case, both output are driven to a low state, the toggle

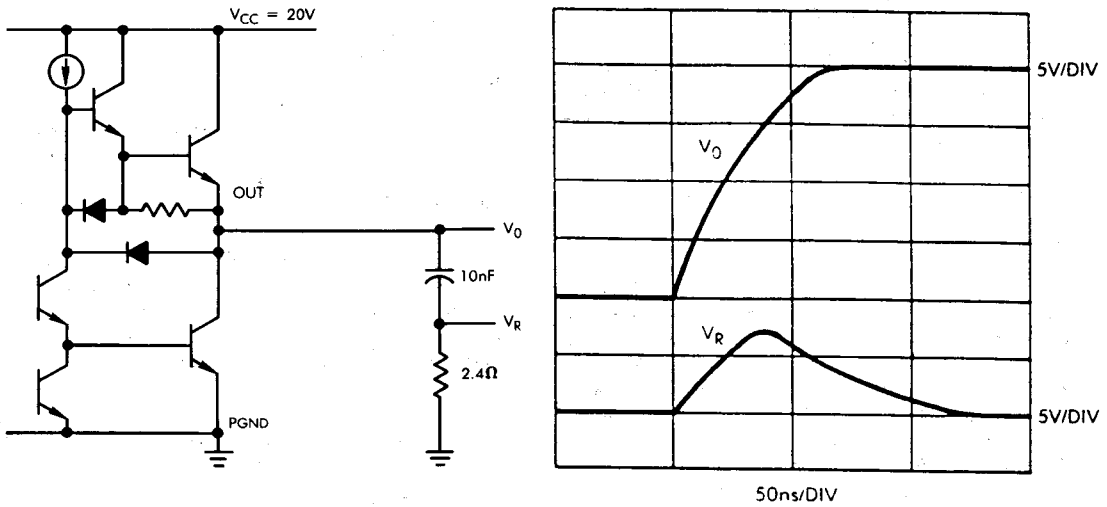


FIGURE 7. OUTPUT STAGE MEASURED PERFORMANCE.

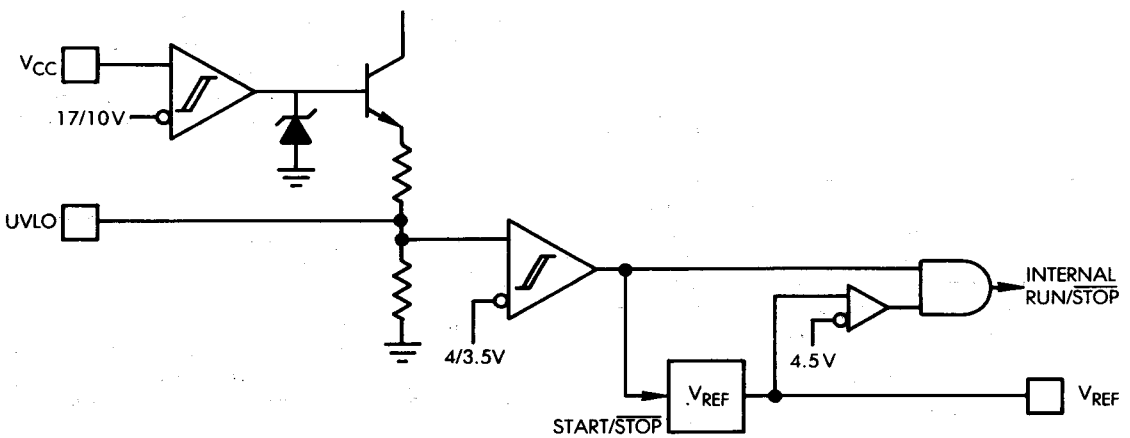


FIGURE 8. UVLO DETAILED BLOCK DIAGRAM.

flip flop is preset to select ouput A, the soft-start capacitor is discharged, and the fault latch is reset.

Application of the UVLO features is simple. With no connection to the UVLO pin, the behavior of the UVLO block is dominated by the V_{cc} comparator and is suited for off-line usage. DC to DC applications can be made by two external resistors, one from V_{cc} to UVLO and the other from UVLO to ground. This exploits the 4V hysteretic threshold of the second comparator. Keep in mind that the UVLO pin has an input impedance of 23 kohm when selecting the two external resistors. Operation from a 5V supply is achieved by tying UVLO, V_{cc}, and V_{REF} all to the external 5V supply. The UVLO pin can also be used to disable the chip at any time by pulling it below 3.5V. The UVLO pin will source no more than 1.5mA when pulled to ground.

FAULT MANAGEMENT AND RESTART SEQUENCING

The fault comparator and latch along with the soft-start and restart delay functions are shown in (figure 9). When the chip is powered up, UVLO resets the fault latch and discharges the soft-start capacitor, C_{SS}. The restart delay capacitor, C_{RD}, is also discharged since the latch is reset. After UVLO, C_{SS} is charged by an internal 5μA current source. The voltage at the soft-start pin is used to modify the upper clamp voltage of the error amplifier. In this way, a slow frequency ramp is obtained from zero to the point where the control loop takes over.

The chip is designed for easy implementation of a hic-up style of fault management. The fault comparator will sense signals with a common mode range of −0.3 to 3.0V. If (hopefully never in your application) the input to the fault comparator causes its output to go high, the fault latch is set. Immediately the one-shot is cleared and the outputs turn off. C_{SS} is also discharged. C_{RD} is then allowed to be charged by an internal 5μA current source. This is the zero power dissipation time in the hic-up cycle. Until the restart delay capacitor charges to 3V, the fault latch cannot be reset. When both the fault comparator output is low and C_{RD} is over 3V, the fault latch is reset. At this point in time, C_{RD} is discharged and C_{SS} is allowed to soft-start the chip. If the cause of the original fault is still present, the chip will continue to hic-up until the fault condition is removed, when normal operation will resume.

Note that the internal 5μA sources are not tightly controlled. However, if either soft-start or restart delay time is critical, a 50k resistor to V_{REF} will provide a precise current that is sufficient to swamp out any inaccuracies of the internal source.

Two variations of the hic-up are possible. Selecting a value of zero for C_{RD} will cause the chip to immediately attempt to restart upon removal of the fault signal. If, on

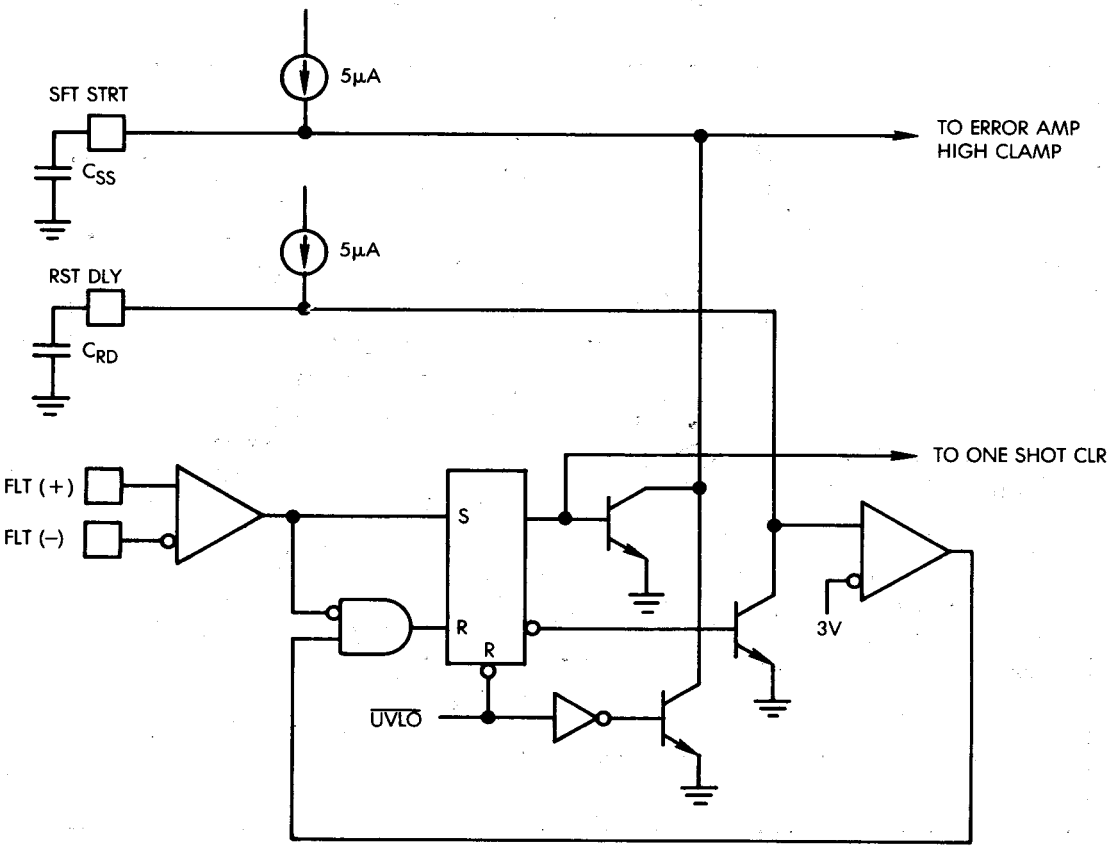


FIGURE 9 FAULT MANAGEMENT AND RESTART SEQUENCING BLOCK DIAGRAM.

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the other extreme, fully latched fault behavior is desired, then the restart delay pin (RST DLY) can either be grounded or tied to the open collector output of an external logic gate. This uncommitted comparator could be used for this application. When Restart Delay is held low, then the only ways to reset the fault latch and reinitiate operation of the chip are to remove V_{CC} (UVLO will clear the latch) or release RST DLY, allowing it to exceed 3V.

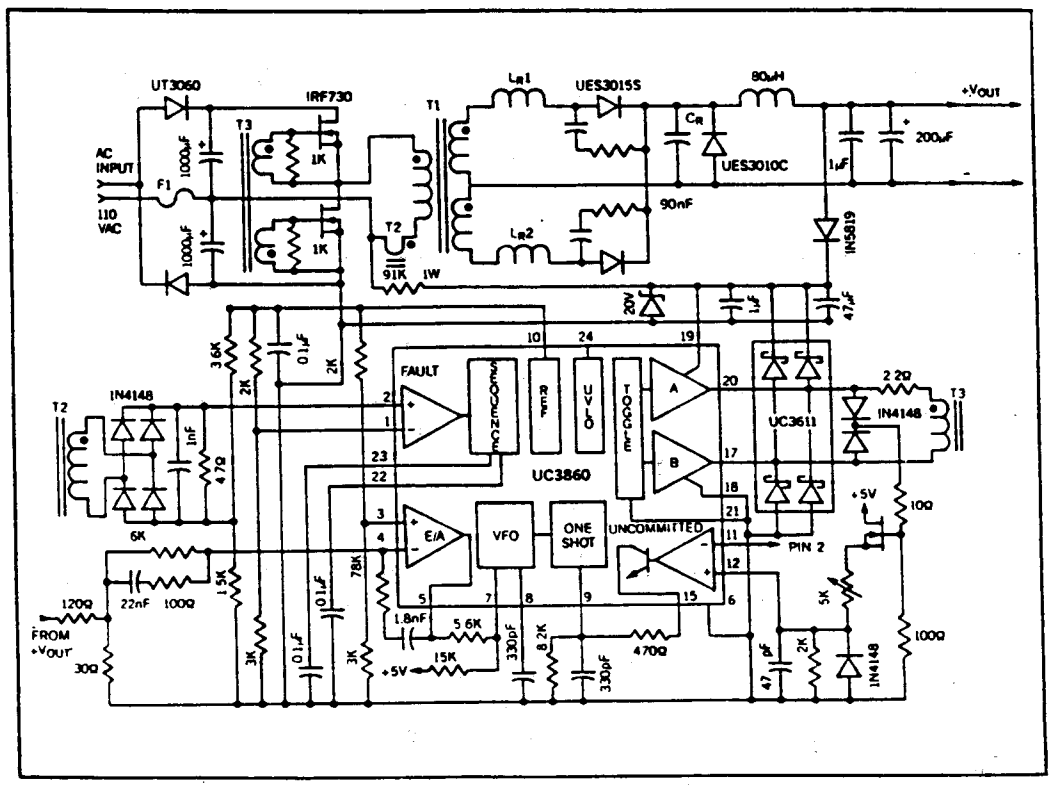
UNCOMMITTED COMPARATOR

The uncommitted comparator is similar in design and speed to the fault comparator except its output drives an open collector npn transistor. This output can be used in a variety of applications. One would be to shunt the RC pin with a second resistor causing a reduction in one-shot pulse width. The input common mode range is identical to the fault comparator, -0.3 to 3.0V.

SUMMARY

The UC1860 control chip has been designed with the necessary features to implement the control function in resonant mode power conversion circuits operating at frequencies up to 3 MHz. While some publicized applications have been considered in the design of this chip, its versatility should accommodate many specific adaptations of resonant mode power systems as well.

150 Watt Quasi-Resonant Power Supply



UC3860 RESONANT CONTROL IC REGULATES OFF-LINE 150 WATT CONVERTER SWITCHING AT 1 MHZ

ABSTRACT

This paper is intended to explore in significant detail the intricacies of the quasi-resonant half bridge topology. Voltage and current waveforms in addition to transferred charge and energy will be analyzed as functions of time, and input/output conditions. Specific and generalized equations are given for this example, also applicable to other topologies by those skilled in modern power supply design.

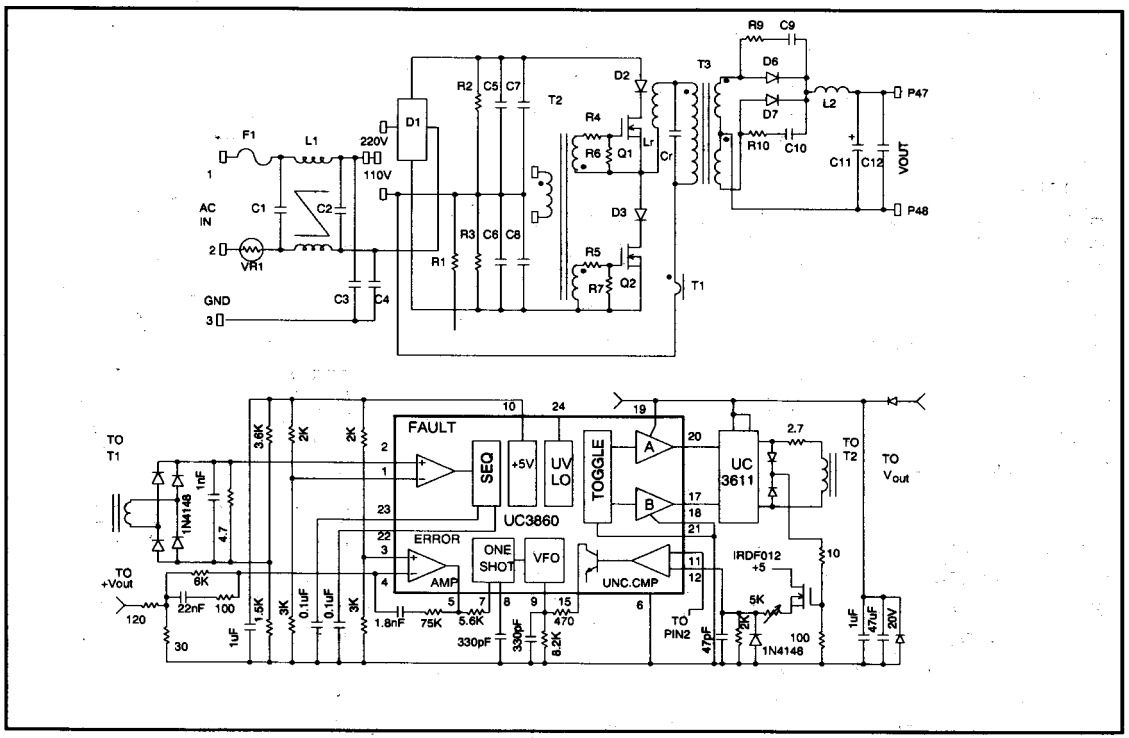
INTRODUCTION

The thrust towards resonant mode power supply designs has been fueled by the industry's demands for increasing power densities and high overall efficiency. Coupled with the additional requirements for low EMI, many designers are exploring the most likely candidate for todays sophisticated, high frequency power supplies; resonant mode power conversion.

amperes of load current, it operates from a 110/220 AC input, or 220 to 380 VDC at high efficiency.

DESIGN CONSIDERATIONS AND OVERVIEW

Although several basic topologies deserve consideration in this off-line application, only the Half Bridge configuration offers numerous key advantages. As opposed to the single-ended Forward converters, the half bridge provides bidirectionial utilization of the transformer, thus eliminating the need to incorporate dissipative or complex flux reset mechanisms. In addition, the primary switched voltage is one-half that of its single ended or full-bridge counter-part, significantly reducing the turn-on losses. As a reminder, zero current switching minimizes ONLY the turn-off losses. During turn-on, however, the current rises linearly before resonance commences, and the half bridge results in lower turn-on losses due to the lower voltage.

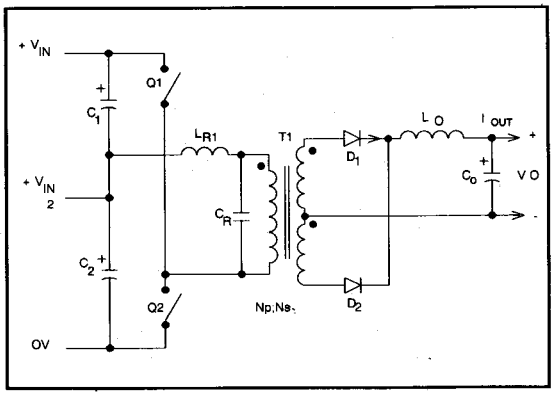


While a bewildering selection of possible resonant mode topologies and configurations exist, this paper will focus on the quasi-resonant half bridge topology. Primary side resonance and zero current switching will be incorporated into the design, with the control circuit essentials performed by the UC3860 resonant mode control IC.

Described in the text is a 150 watt off line converter switching at maximum frequency of 1 megahertz resulting in an effective 500 kilohertz utilization of the main transformer. Delivering 15 volts at 10

Primary side resonance will be utilized in this design, but not as an attempt to minimize the core size. Instead, this technique will reduce the peak secondary currents and rectifier losses. transferrring them to the primary side where the diode voltage drop is less significant, thus enhancing overall efficiency. Additionally, this design can be compared to a previous example [ref. 1] which incorporated secondary side resonance and operated over similar line, load, frequency and power variations.

Half cycle conduction in both design examples accomplishes a undirectional current flow at each of the primary switches. Unlike its full counterpart, all the energy stored i n the resonant capacitor must be transferred to the output, without returning the excess back to the primary storage capacitors.



The UC3860 resonant control IC will adjust the conversion frequency to regulate the fifteen volt output over all line and load combinations. Zero current switching is facilitated by modulating the programmed maximum on-time with the controller's uncommitted comparator. In addition, overload protection is provided by means of a programmable restart delay circuit (hiccup) which reduces the conversion retry rate following a fault detection.

DESIGN SPECIFICATIONS

An off-line 150 watt, single output design has been selected as a typical application. Several items common to most designs will not be highlighted, for example, primary to secondary isolation and input filter calculations.

INPUT VOLTAGE

110 VAC INPUT = 85 MIN, 132 MAX (VAC)

220 VAC INPUT = 170 MIN, 270 MAX (VAC)

DC INPUT = 220 MIN, 380 MAX (VDC)

AC LINE FREQUENCY = 50 HZ MIN

OUTPUT VOLTAGE = 15 VDC

OUTPUT CURRENT = 10 AMPS MAXIMUM CONTINUOUS, 2.5 AMPS MIN

LINE REGULATION = 15 MILLIVOLTS

LOAD REGULATION = 15 MILLIVOLTS

OUTPUT VOLTAGE RIPPLE=

100mV (Pk-Pk), DC-20 MHZ

EFFICIENCY = 75% TYP. AT FULL LOAD

TOPOLOGY FUNDAMENTALS AND OVERVIEW

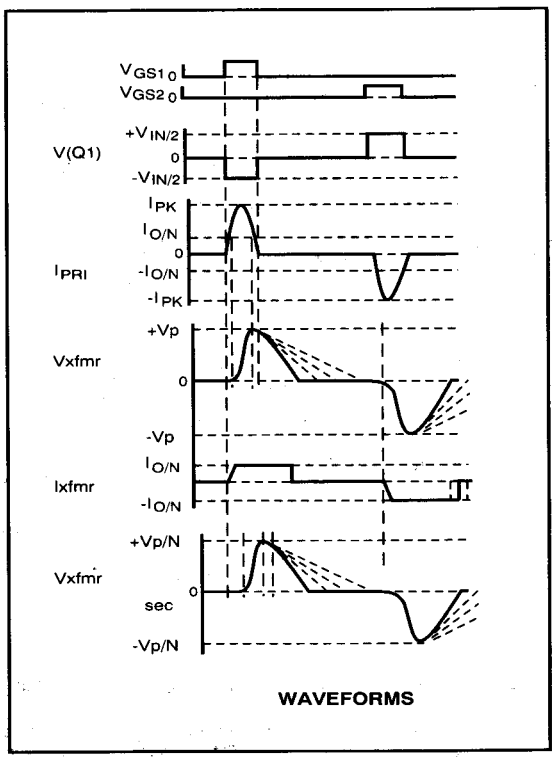
The general circuit diagram for a quasi-resonant half bridge converter using primary side resonance is shown with the corresponding waveforms. Transistors Q1 and Q2 are alternately driven from the control circuitry at a repetition rate determined by the UC3860's error amplifier output voltage and turned off at zero current by the detection circuitry..

Transistor Q1 turns on at time t(0), connecting the series resonant L C tank across the bulk storage capacitor C1, with a voltage potential of +Vin/2. The primary current ramps up linearly at the rate of +Vin/(2*Lr) from zero to Iout/N which is intersected at time t(1). During this interval dt(1-0) all primary current is delivered to the output, and no voltage is across the resonant capacitor Cr.

Beginning at time t(1), primary current can be expressed by adding the two individual components; the "constant" output current Iout/N, and the sinusoidal current (Ir) flowing through the resonant capacitor. The peak resonant current is determined by the iput voltage (+Vin/2) divided by the characteristic tank impedance, Zn. Primary current rises to its peak of Ir plus Iout/N, and decreases sinusoidaly. It intersects the output current (Iout/N) again at time t(2), and crosses zero at time t(3) when the transistor switch is turned off.

In a sinuosidal manner, the resonant capacitor voltage begins its rise at time t(1) and continues to its peak at time t(2). The voltage then decreases until time t(3) where it then begins a linear discharge at the rate of Iout/Cr. Zero voltage is reached at time t(4) when all stored charge in the resonant capacitor has been transferred to the output. This waveform is also the transformer primary voltage, and is reflected to the secondary side by the turns ratio N.

Secondary current has a linear leading edge until reaching its plateau of Iout, assuming a negligible magnetizing current for the output inductor. The resonant capacitor provides a constant current to the output until its charge is totally transferred. At this point, the energy is stored in the output LC section provides a regulated output until the next cycle is initiated. Consecutive switching cycles will repeat the conversion process and corresponding waveforms.

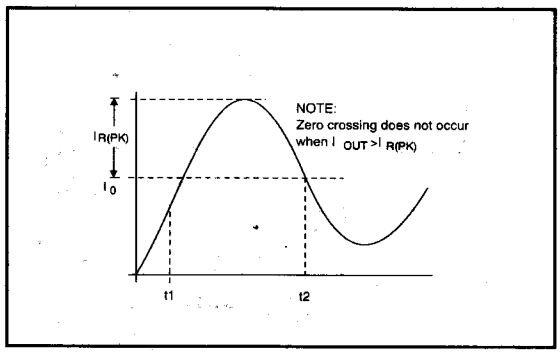


WAVEFORMS

QUASI-RESONANT CIRCUIT LIMITATIONS

In order to facilitate zero current switching, the peak resonant current component I(r) must always be greater than Iout, or the zero inersect will not be reached. Specifically, the output impedance (Zo) must always be greater than the characteristic tank impedance, (Zn). This relationship also specifies the minimum input voltage (Vin min) and maximum output current (Iout) limits for proper circuit operation.

The ideal ratio of the full output current (Iout max) to the minimum resonant peak current Ir(peak) min is unity. This insures resonance at all loads while preventing excessively high peak resonant tank currents, and losses. A twenty-five percent overload current will be used as a guardband in this design. Typical of many current limit thresholds, it corresponds to an 0.75:1 ration of Iout(max) to Ir(peak)min.



Being a Buck derived topology, the secondary input and output volt-second products must be equal, thus defining Vin (secondary) minimum. The resonant tank inductor and capacitor can be transposed to the secondary also, and calculated knowing Vin min(sec), F(res) and Z(o)min. Once the transformer turns ratio has been determined, these can be appropriately scaled to the primary side.

The resonant L-C components are now uniquely defined by:

$$L(r)sec = \frac{.75 * Vsec(min)}{2 * Pi * Fres * Iout} = \frac{0.12 Vsec(min)}{Fres * Iout(max)} = 175nH$$

C(r)sec = 1 [(2*Pi*Fres)^2*L(r)=91nF

Z(r)sec = (L(r)/C(r))$^{0.5}$ = 1.39 ohms,

and Fres = 1.25 MHz

TRANSFORMER TURNS RATIO

The determination of the transformer turns ratio for this design will begin similarly to that of conventional square wave converters. Obviously, the required output volt-second product must first be satisfied with the most difficult condition being low line and full load. A topology coefficient, K(t) is introduced to specify the maximum ratio between the conversion (switching) frequency and the resonant tank frequency. This is somewhat analagous to maximum duty cycle is a square wave converter. As K(t) approaches unity, the utilization is maximized and turns ratio is optimized.

Charge is taken from the bulk storage capacitors during each cycle and stored in the resonant capacitor. The output load discharges this at a rate determined by the output currrent, and the discharge time varies inversely with load current. At full load, the minimum discharge time is reached, reduceing the topology coefficient, K(t), to 0,8 in this application.

To satisfy the required output volt-second product of this Buck derived converter at low line:

$$Vout = \frac{Vpri * K(t)}{2 * N}, \text{ or } N = \frac{K(t) * [Vp(min) - Vloss]}{2 * (Vo + Vd + Vloss)} = 5.1:1$$

More specifically, the turns ratio can be calculated by examining the total charge transferred per cycle, Q(t). This varies as a function of Vin, Iout and Vout, assuming C(r) is fixed and zero current switching. [ref 2] Using the specified parameters for this design, the relationships are combined and the quadratic equation is solved, resulting in a turns ratio (Np/Ns) of 5.1:1 also. The design will proceed using a 5:1 ratio for simplicity.

$$N^2\left[\frac{Lrs * Io}{(Vo + Vd)} - Tc\right] + N\frac{(Vpri - Vx)}{4 * Fr * (Vo + Vd)} + \frac{Crs * (Vp - Vx)^2}{2 * (Vo + Vd) * Io} = 0$$

where Tc= 1/Fconv(max) = 1us; Vx= Vloss primary MOS switch

Vd=Vrectifier (output); Io=Iout maximum

and Vpri=Vp(minimum)

MAIN TRANSFORMER DESIGN

Off-line transformers lend themselves to low, wide bobbin windows, typical of the ETD geometry. This shape window provides adequate room to accomodate the creepage and clearance distances required for international safety specifications. Transformer losses will be held around one-percent of the total input power, or approximately 2 watts with a temperature rise not to exceed 40 degrees Centigrade. A core size is selected with a thermal impedance R(t) in the neighborhood of 40°C/2W, or 20°C/W. The precise size will be calculated using the area-product formula for core-loss limited conditions, typical in a high frequency power supply.

$$AP = \left[\frac{P_{in} * 10^4}{120K2f}\right]^{1.58} * (K_h f + K_e f^2)^{0.66} \quad cm^4$$

WHERE:

Pin = Input Power - 180 Watts

K = Winding Factor = 0.163 for a half bridge

f = Transformer Frequency = 500 KHZ

Kh = Hysteresis Coefficient = 4*10^-5 for 3C85

Ke= Eddy Current Coefficient = 4*10^{-10} for 3C85

A calculated area-product of 0.543 cm^4 steers the selection towards the ETD-34 geometry and size, and 3C85 material. Since the core volume is slightly larger than required, the actual core losses (per cm^3) will be lower than first estimated.

Calculating the volt-second product for this primary side resonant design is more difficult than for that of its secondary side counterpart. Integrating the complex voltage waveform over the conversion period is the most exact method, as detailed in the charge transfer equations [ref2]. A less precise, yet fairly accurate technique is to assume a triangular voltage waveform, breaking the period into on-time and off-time sections. Addition of these geometric areas (V*t) results in an estimate of the actual primary volt-second product. Core losses will need to be analyzed over the full range of line, load and conversion frequency ranges. The minimum number of primary turns will be calculated using low line conditions, and the cross sectional core area of 0.971 cm^2. A total flux density swing of 1 kiloGauss (per manufacturers data) is recommended not to exceed the allocated temperature rise.

$$Np(min) = \frac{PrimaryV * t\,product * 10^4}{FluxSwing * CoreArea}$$

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Using low line condition and 10V MOS drop.

$$Np\,(min) = \frac{0.5*200*10^{-6}*10^{4}}{0.100\ T*0.971\ cm^{3}} = 10.3\,Turns$$

(Use 10 Turns)

The actual core power density is calculated from the following equation, allowing a 20 degree temperature rise due solely to core losses.

$$Power\ Density = \frac{T_r}{R_t \cdot Vol} = \frac{20^{\circ}C}{19 \cdot 7.64} = 138 mw/cm^3$$

The manufacturers core data lists the thermal resistance of the ETD-34 core set as 19 degrees C per watt, with a core volume of 7.64 cm^3. Several methods of dividing the power losses between core and copper loss can be used. The most common of these suggests an almost equal split between the two, allowing slightly more core than copper loss if possible. An even division of the total losses between the two will be utilized in this design as a first approximation. Later, an evaluation of the minimum number of turns and wire sizes may suggest that the 50/50 ratio be changed to favorably accommodate fewer turns, or less copper.

It has already been established in a previous section that the turns ratio for this design be 5:1, Npri: N sec. Minimization of the leakage inductance is obtained by "sandwiching" the secondaries between the primaries, or using a split primary winding technique.

In this example, one-half of the primary number of turns will be wound first, closest to the core center leg. Then, the corresponding secondary is wound directly above its primary, followed by the other secondary. The final winding is the remaining primary half, with good coupling to its corresponding secondary as shown in the following figure.

WINDING ORIENTATION

Copper strap or foil will be utilized for each winding to minimize "build-up" which increases the distance between windings, hence leakage inductance. The necessary primary and secondary copper areas are calculated using their respective currents divided by 450 amps/cm^2 for a low temperature rise. Other transformer specifics are calculated below.

PRIMARY RMS CURRENT, I pri(rms) = 2.8 AMPS RMS

SECONDARY RMS CURRENT 1sec(rms) - 7.1 AMPS RMS (EACH WINDING)

PRIMARY CONDUCTOR AREA Axp = Ipri(rms)/450 A/cm3 = $6.33*10^{-3}cm^2$

SECONDARY CONDUCTOR AREA Axs = 1sec(rms)/450A/Cm3 = $15.8*10^{-3}cm^2$

PRIMARY INDUCTANCE, Lpri = Al*Np^2 = 190 uH

SECONDARY INDUCTANCE, Lsec = Al*Ns^2 = 7.6 uH (each)

The primary conductor area is approximately equal to that of an AWG #19 wire, while the secondary area is closest to an AWG #14 wire. From Eddy Current calculations is can be seen that the depth of penetration at 500KHZ is $10.6*10^{-13}$ cm, or about the thickness of an umber 37 AWG wire. The most practical technique to minimize the AC loss in a transformer winding is to incoporate copper strip, or foil, as in this design. Its width is determined by the bobbin width and safety spacing requirements of 8 mm per winding as shown.

An 8 millimeter primary to secondary spacing between the winding ends will be subtracted from the bobbin width of 2.1cm, leaving 1.30 cm for the copper strap width. Allowing for tolerances, standard half-inch (0.500") width foil will be utilized in this design.

Standard 2 "mil" (0.002 in) foil will be used for the primary, which is slightly larger than the required thickness of 1.872 thousandths of an inch. The calculated secondary thickness exceeds the depth of penetration, so twin foils each of half the required thickness (0.0085 cm) are mandated. Each of the three "mil" (0.003") foils will be thinly insulated from the other.

The resistance and power loss of each winding is summarized:

R pri = $2.29*10^{-6}$ * 5.99 *10 T/6.18 *10^{-3} = 22.2 milliohms.

R sec = $2.29*10^{-6}$ *5.99*2T/21.91 *10^{-3} = 1.25 milliohms

Winding power loss = 1 rms^2 (winding) * Resistance (winding

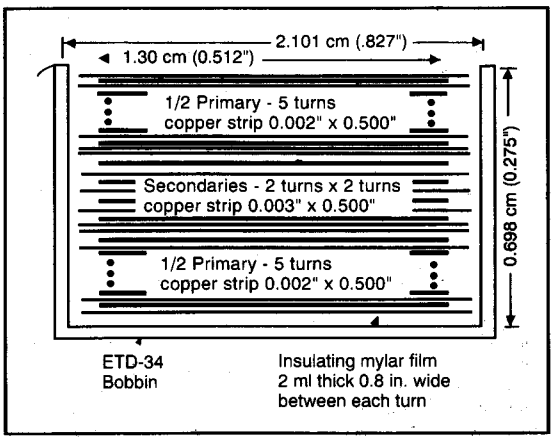
P loss pri = 2.8^2 * 0.0222 = 174 milliwatts (each wdg)

P loss sec = 7.1^2 * .125*1^{-3} = 63 milliwatts (each wdg)

P loss copper = 2*(174 + 126 mW) = 0.60 watts

Transformer power loss = copper + core loss = 1.5 watt total

Temperature rise = R(0) * Ploss total = 19°C/W * 1.5 = 28.5°C



DESIGN PROCEDURE AND SUMMARY

The resonant components can now be transformed to primary side values using the caluclated turns ratio N.

L(r)p = L(r)s * N^2 = 4.4 uH

C(r)p = C(r)s / N^2 = 3.6 nF

Z(r)p - [(L(r)p / C(r)p)$^{0.5}$] = 35 ohms

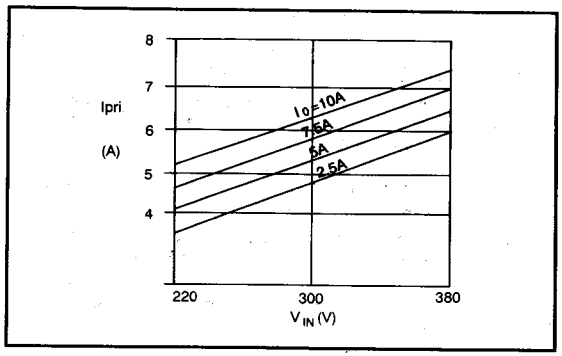
Additionally, the peak primary current and rms currents at the transistor switch, transformer primary and secondary rectifiers are calculated by the following relationships:

I(p)pk = [Io(max)/N] + Vp(max)/(2*X(r)p) = 5.2A @220V, 7.4A @380V

I(p)rms = I(p)pk*[Ton/(2*Tconv()$^{0.5}$ = 2.85 Arms at XFMR primary (assume pulsed sinusoid) = 2.01 Arms at each switch

I(s)rms = I(o)max*[(Ton/Tconv)0.5] = 7.8Arms at XFMR secondary = 5.5Arms per rectifier

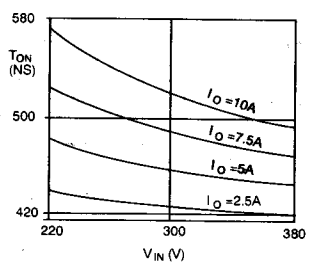
The selection of semiconductors, rectifiers, heatsinking requirements and wire gauges follow standard design practices. For the purpose of this paper, no elaboration is included, however is detailed in references 1 and 2. Using this design equations listed previously and in the Appendix, these parameters can be calculated and plotted over the line and load ranges specified, and are summarized in the following graphs:



TIMING CONSIDERATIONS

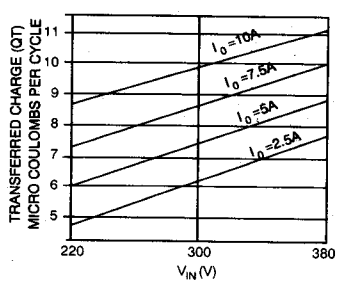
The operation of this quasi-resonant circuit has been described as requiring a variable frequency, FIXED on-time control pulsetrain. In actuality, the on-time must be varied to facilitate zero current switching with changes in input voltage and output current. Using the timing relationships presented in chapter five, the on-time is calculated and plotted for the ranges of Vin and Iout.

ON-TIME vs. Vin AND Iout



The charge transferred from the primary to the secondary per cycle is a function of both Vin and Iout. Using the equations presented previously in section 5, the results are graphically represented in the following figure.

Transferred Charge vs. Vin and Iout

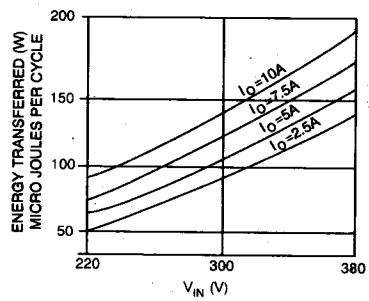


For the selected values of voltage and current shown, the average change required in voltage or output current per micro Coulomb transferred have been calculated.

AVERAGE dV/uC = 5.935 V/uC; and the average dI/uC = 2.086 A/uC

The energy transferred per cycle is obtained by multiplying the results from the charge calculations by Vin / 2 to convert from charge to energy, with the results shown below.

ENERGY TRANSFERRED PER CYCLE



The conversion period is obtained by dividing the energy transferred per cycle by the output power, accounting for an overall efficiency near 85%. Conversion frequency, its inverse, is graphically depicted for various input voltages and output currents below.

CONVERSION FREQUENCY

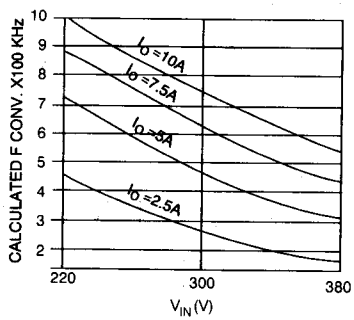
The control circuit adjusts the conversion frequency to maintain a constant output voltage of V out over changing line and load combinations. Maximum conversion frequency will occur at low line and full load, where, by design, the frequency equals the resonant tank frequency divided by K(t). Minimum frequency will occur at high line (Vpri max) and light load (Iout min), and the following equation can be used to estimate the conversion frequency for various line and load possibilities.

$$Tconv = \frac{vpri}{2*N*Io*Vo}\left[\frac{2*N*Lrs*Io^2}{Vpri} + Vpri*\frac{Crs}{N} + \frac{Io}{2*Fr}\right]$$

which can be expanded to account for losses in both the primary switches (Vx) and output rectifiers (Vd) and reduced to:

$$Tconv = \frac{Lrs*Io}{Vo-Vd} + \frac{Crs*(Vp-Vx)^2}{2*N^2*Io*(Vo-Vd)} + \frac{Vp-Vx}{4*N*Fr*(Vo-Vd)}$$

CONVERSION FREQUENCY vs. Vin & Iout



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OUTPUT FILTER DESIGN

The output inductor will be designed for one amp of ripple current at the minimum conversion frequency of approximately 200 KHZ equating to 90 uH. Due to the variable frequency operation, the ripple current will change inversely with operating frequency, as maximum load occurs, the ripple current is at its lowest. A 1.3" o.d. toroidal core of high frequency material was utilized, available as a standard product from Pulse Engineering.

For the output capacitance, two 100 uf electrolytic capacitors were used in parallel to achieve an ESR value of 3 to 15 milliohms — a broad range necessitated by the difficulty in getting specified high frequency data from capacitor manufacturers. A final component added to the output filter is a good high frequency capacitor to bypass the inductive components of the electrolytics and shunt any switching spikes which might get to the output. Unitrode "P" type ceramic monolythic capacitors are used for this application.

THE UC3860 RESONANT MODE CONTROL IC

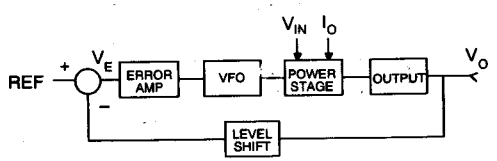
The versitile UC3860 resonant mode controller easily implements fixed on-time, frequency modulated control schemes while providing various user programmable features and unique fault protection. Specifically, this 3 MHz device includes dual 3 amp peak totem pole output drivers and precision clamps on the 5 MHz error amplifier output to accurately control minimum and maximum frequency. In addition, an uncommitted comparator is included for use with zero current switching techniques, and programmable fault thresholds and logic for reduced losses during overload conditions. Preset undervoltage lockout thresholds of 17/10 volts are optimized for off-line designs, but are easily reprogrammed by the user for other applications.

Each of the UC3860 functions are utilized in this design and have been previously highlighted in the references. Zero current detection and switching is performed by connecting the uncommitted comparator's output to the one shot timing network, a technique which allows a programmed maximum on-time that can be modulated as zero current is crossed. Any propagation delays can effectively be "nulled-out" with the addition of anticipator circuit detailed in references 1 and 2. A programmable restart delay following the receipt of a fault condition, often referred to as "hic-cup" has been incorporated in addition to soft start, which gradually increases the conversion frequency in a resonant converter. The UC3860 provides complete regulation and control for this 150 watt design over all line and load combinations.

CLOSING THE LOOP

There are several gain stages in the quasi-resonant control loop, and each will be examined to obtain good closed loop circuit response. The block diagram below displays the various gain stages.

BLOCK DIAGRAM - CONTROL LOOP



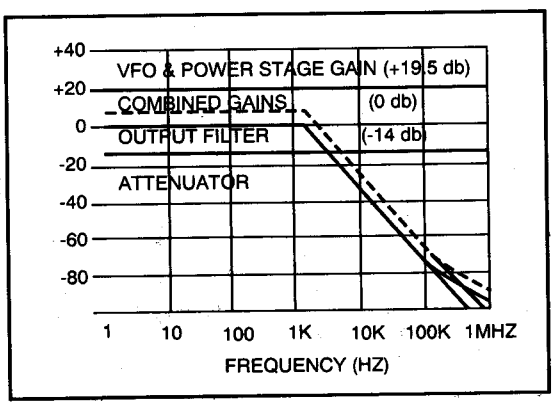
POWER STAGE

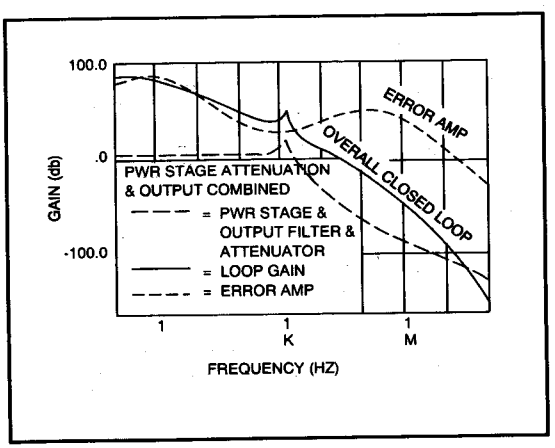
The small signal gain of the power stage will be approximated by analysis of the charge transferred at various line and load combinations. An assumption is made that the power switch on-time is constant, and any changes in frequency directly effect the off-time, or resonant capacitor discharge time. Additionally, both Vin and Iout are assumed to be constant during the interval of interest.

Tabulated below at several points of interest are the values for this gain, obtained from the results of previous sections for work done in the references. The gain of the power stage (in volts per hertz) varies significantly over the input and output ranges, and the highest value will be used to approximate the worst case condition.

V IN sec(V)	I OUT (A)	Win uJ/cyc	F conv KHZ	GAIN Vusec	GAIN (db)
22	2.5	50	450	9.0	19.1
38	2.5	140	180	10.1	20.1
22	5	60	730	8.76	18.9
38	5	160	320	10.7	20.6
22	7.5	78	900	9.65	19.7
38	7.5	185	450	11.3	21.1
22	10	91	1000	9.55	19.6
38	10	205	560	11.8	21.5

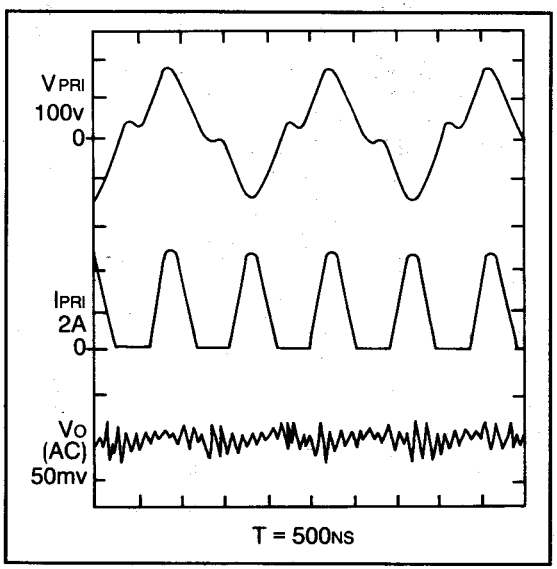
A slightly greater than worst case value of 23 volt-microseconds will be used for the power stage. Multiplying this by the VFO gain of 0.4 Mhz/v results in an combined gain of 9.2 Vout / Vea out.





POWER SUPPLY PERFORMANCE

This 150 watt quasi-resonant supply performed flawlessly over its specified parameters, attaining the overall full load efficiency goal of 80%, however, only at low line. A decrease to 75% was seen as high line was approached, an indication that more attention to high dV/dt losses should be exercised. Nevertheless, low switching noise, quasi-sinusoidal power waveforms and substantially reduced EMI are worthwhile benefits, especially over conventional square wave converters. The relavent primary voltage and current, in addition to secondary voltage waveforms are displayed. These plots were obtained using a 250 MHz bandwidth digitizing scope, UHF measurement techniques and no bandwidth limiting or waveform averaging to distort the high frequency components.



Construction of the power conversion stage was accomplished using the Unitrode UC3860 demonstration kit printed circuit board, with ample facilities to accomodate a variety of quasi-resonant topologies and configurations. The control section was built using the UC3860 evaluation kit p.c. board, and interconnections to the gate drive and current sense transformers made with 75 ohm coaxial cables. An auxiliary winding from the main transformer and opto-coupled feedback were later added to this design for complete primary to secondary isolation.

SUMMARY AND CONCLUSIONS

The ultimate blend of high power density with high efficiency and low noise is realizeable today using quasi-resonant techniques, conventional topologies and existing components. In most applications, the upgrade is quite simple, as many of the devices go unchanged in the process. The control circuit, on the other hand, requires a far more sophisticated controller than for its square wave predecessors. Additionally, as switching frequencies are further pushed towards and beyond a megahertz, the needs for even higher performance and higher speed control logic become increasingly obvious. The UC3860 resonant mode controller exceeds these requirements, simiplifying and condensing the control circuit design process to resistor and capacitor value selections.

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Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460