

Overcoming Challenges in Designing Step-Down Regulator Applications with $\geq 40V$ Input Voltage

— By Robert Bell, Applications Engineer

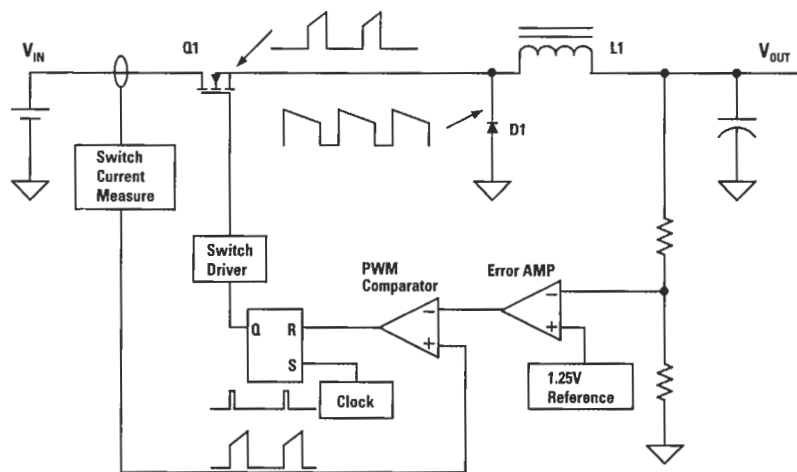


Figure 1. Buck Regulator Using Current Mode Control

Switching regulators are commonly used to step-down a higher level, unregulated input voltage to a regulated output voltage. In applications requiring DC-DC conversion from a relatively high input voltage, a switching regulator will dramatically improve conversion efficiency relative to linear regulator alternatives. Two of the most common transformer based DC-DC converter topologies are the Flyback and Forward. These topologies are very effective for high input to output step-down ratios since the transformer turns ratio can be set to accomplish the majority of the step-down conversion. For example, the conversion equation for a Forward converter is approximately: $V_{OUT} = V_{IN} \times D \times N_s/N_p$

Where D is the duty cycle of the modulating switch, and N_s and N_p are the quantities of the transformer secondary and primary turns. For $V_{IN} = 66V$

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and $V_{OUT} = 3.3$ (20:1 step down) the transformer turns ratio (N_s/N_p) can be set to 1:10, requiring the modulation switch duty cycle to be 50%. For a 500 kHz operation, the 50% duty cycle equates to a switch on-time of 1 μ s. For applications that do not require ground isolation, a Buck regulator is a more desirable topology. The buck topology provides a lower cost solution since it does not require a transformer. The conversion equation for a buck regulator is simply: $V_{OUT} = V_{IN} \times D$

Buck regulator applications with a high input to output step-down ratio require a small duty cycle. Coupled with high-frequency operation, the on-time for the modulating switch becomes very small. The high frequency and high step down ratio imposes significant challenges for the pulse-width modulation (PWM) controller. A buck regulator with $V_{IN} = 66V$ and $V_{OUT} = 3.3V$ operating at 500 kHz will require an on-time of 100 ns.

Common modulation control methods often used in buck regulators include Voltage Mode (VM), Current Mode (CM), and Constant On-Time (COT) control. Current-mode control provides ease of loop compensation and inherent line feed-forward compensation which make this method a favorite among power designers. Voltage-mode control is typically less noise sensitive but under-performs current mode in transient response and ease of stabilization. Constant On-Time control eliminates most of the stability-related issues and responds well to line and load transients. However, COT controlled regulators do not operate at constant switching frequency and cannot be synchronized to an external clock.

Figure 1 shows the block diagram of a buck regulator utilizing the current-mode control method. The output voltage is monitored and

compared to a reference, with the resulting error signal applied to the PWM. The origin of the modulating ramp is where voltage mode and current mode control differ. The modulating ramp used in current mode control is a signal proportional to the buck switch current. The inductor current flows through the buck switch during the switch on-time. During this time, the inductor current waveform has a positive slope of $(V_{IN} - V_{OUT})/L$. An accurate, fast measurement of the buck switch current is necessary to create the modulating ramp signal. The main disadvantage of current-mode control is the difficulties encountered creating the buck switch current signal.

Propagation delays and noise susceptibility make it almost impossible to use conventional current-mode control for high input voltage, large step-down buck regulator applications where very small on-times are required. Measuring the buck switch current is challenging. The measurement techniques commonly used are, make a voltage measurement across a shunt resistor or the buck switch 'on' resistance or use a current mirror circuit coupled to the buck switch. Each method requires a level shift to transpose the measured signal down to the ground reference for application to the PWM comparator. Even with the best design practices, current sense and level shift circuits will add a significant propagation delay. Another challenge is, when the buck switch is turned on, the free-wheel diode (D1) will turn off. A reverse recovery current will flow through the diode and the buck switch, causing a leading edge current spike and an extended ringing period. This spike can cause the PWM comparator to prematurely trip, causing erratic operation. The most common solution is to add filtering or leading edge blanking to the current sense signal. Attempts to filter or

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blank this leading-edge spike increase the minimum controllable on-time of the buck switch.

Creating an Emulated Current Sense Signal

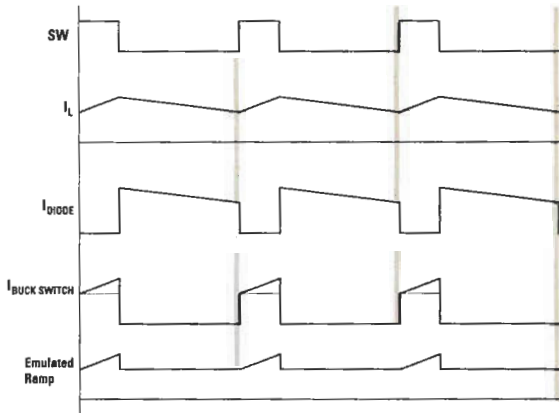


Figure 2. Buck Regulator Waveforms

The challenge of accurate and fast buck switch current measurement can be avoided with a new method that emulates the buck switch current without actually measuring the current. In a buck regulator, the inductor current is the sum of the buck switch current and free-wheel diode current, as shown in *Figure 2*. The buck switch current waveform can be broken down into two parts, a base or pedestal and a ramp. The pedestal represents the minimum inductor current value (or valley) over the switching cycle. The inductor current is at its minimum the instant the free-wheel diode turns off, as the buck switch turns on. The buck switch and the diode have the same minimum current value, occurring at the valley of the inductor current. A sample-and-hold measurement of the free-wheel diode current, sampled just prior to the turn-on of the buck switch can be used to capture the pedestal level information.

The other part of the buck switch current waveform is the ramp portion of the signal. The voltage across the inductor is the difference between the input (V_{IN}) and output (V_{OUT}) voltages when the buck switch is on. This voltage forces a positively ramping current through the inductor and the buck switch. The ramping current slope is equal to: $di/dt = (V_{IN} - V_{OUT}) / L$. An equivalent signal can be created with a voltage controlled current source and a capacitor. The rising voltage slope of a capacitor (C_{RAMP}) driven by a current source (I_{RAMP}) is equal to: $dv/dt = I_{RAMP} / C_{RAMP}$. If the current source is set proportional to the difference between the input and output voltages the capacitor ramp slope is equal to: $dv/dt = K \times (V_{IN} - V_{OUT}) / C_{RAMP}$, where K is a scale factor for the current source and C_{RAMP} is the ramp capacitor. The value of C_{RAMP} can be selected to set the capacitor voltage slope proportional to the inductor current slope.

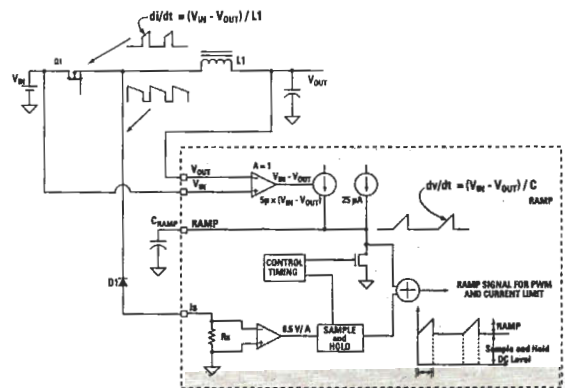


Figure 3. Emulated Current Mode Control Ramp Generator

Figure 3 presents the block diagram of the LM25576, one of six new integrated buck regulators that implement the emulated current mode control scheme described above. The top portion

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of the diagram shows the normal buck regulator power switching components. The free-wheel diode anode is connected to ground through the controller. A small value current sense resistor and amplifier are used to measure the diode current. The sample-and-hold circuit triggers each cycle, just prior to the turn-on of the buck switch, providing the pedestal portion of the emulated current sense signal.

The LM25576 senses the input voltage and the output voltage to generate a current source that charges an external ramp capacitor (C_{RAMP}). Each cycle when the buck switch is turned on, the capacitor voltage rises linearly. When the buck switch is turned off, the ramp capacitor is discharged. For proper operation, the ramp capacitor is set proportional to the value of the output inductor. A good starting point is to select $C_{RAMP} = L \times 10^{-3}$, where the units of L are Henrys and C_{RAMP} are Farads. The last step necessary to complete the generation of the emulated buck switch current signal is to sum the pedestal information (from the sample and hold) to the ramp capacitor voltage signal. The final result is a controller that behaves like peak current mode control but without the delay and transient effects in the current sensing signal.

For applications operating with duty cycles greater than 50 percent, peak current mode controlled regulators are subject to sub-harmonic oscillation. By adding an additional fixed slope voltage ramp signal (slope compensation) to the current sense signal, this oscillation can be avoided. Referring to the ramp generator circuit, an additional fixed 25 μ A offset current provides additional fixed slope to the capacitor voltage ramp signal. For very high duty cycle applications the 25 μ A current source can be supplemented with a pull-up resistor or the ramp capacitor value can be decreased to increase

the ramp slope, preventing sub-harmonic oscillation.

Overload Protection

The LM25576 output overload protection is accomplished with a dedicated current limit comparator that limits the emulated peak current on a cycle-by-cycle basis. The emulated current mode method provides the added benefit of capturing the inductor current information prior to the buck switch turn-on. If the current pedestal exceeds the current limit comparator threshold, the buck switch skips cycles allowing the inductor current additional time to decay, preventing current run-away.

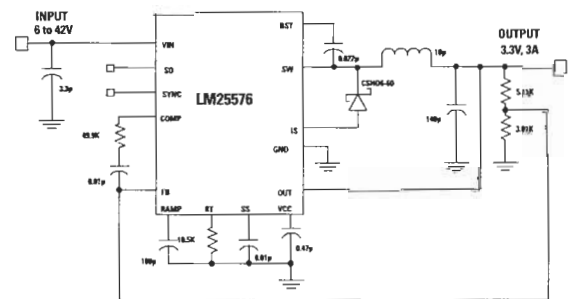


Figure 4. LM25576 Buck Regulator Schematic

Current-mode control offers many benefits. However in buck regulator applications requiring very short on-times the generation of the modulating ramp is very difficult. Through the use of an emulated ramp signal this challenge can be overcome. National has developed a new family of integrated regulators using the emulated current mode control technique.

For more information, visit switcher.national.com