CONTROLLING ZERO VOLTAGE SWITCHED POWER SUPPLIES

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ABSTRACT

Recent advancements in resonant and quasi–resonant power conversion technology propose alternative solutions to a conflicting set of square wave conversion design goals; obtaining high efficiency operation at a high switching frequency from a high voltage source. Today, the conventional approaches are by far, still in the production mainstream, however an increasing challenge can be witnessed by the emerging resonant technologies, primarily due to their lossless switching merits. The intent of this presentation is to unravel the details of zero voltage switching via a comprehensive analysis of the timing intervals awith a specific emphasis on the control IC requirements.

INTRODUCTION

The concept of quasi-resonant, "lossless" switching is not new, most noticeably patented by one individual [1] and publicised by others at various power conferences.[2,3] Numerous efforts focusing on zero current switching ensued, first perceived as the likely candidate for tomorrow's generation of high frequency power converters.[4,5,6,7,8] In theory, the on-off transitions occur at a time in the resonant cycle where the switch current is zero, facilitating zero current, hence zero power switching. And while true, two obvious concerns can impede the quest for high efficiency operation with high voltage inputs.

By nature of the resonant tank and zero current switching limitation, the peak switch current is significantly higher than its square wave counterpart. In fact, the peak of the full load switch current is a minimum of twice that of its squarewave kin. In its off state, the switch returns to a blocking a high voltage every cycle. When activated by the next drive pulse, the mosfet output capacitance (Coss) is discharged by the fet, contributing a significant power loss at high frequencies and high voltages. Instead, both of these losses are avoided by implementing a zero voltage switching technique. [9,10]

ZERO VOLTAGE SWITCHING OVERVIEW

Zero voltage switching can be considered as conventional square wave power conversion during the switch on-time with "resonant" switching transitions. Similar to constant off-time converters, the conversion frequency, or on-time is modulated in order to maintain regulation of the output voltage. For a given unit of time, this method is analagous to fixed frequency conversion which using an adjustable duty cycle. The foundation of this conversion is the volt-second product balancing of the input and output. It is virtually identical to that of square wave power conversion, and vastly unlike the energy transfer system of its electrical dual, the zero current switched converter.

During the OFF-TIME of the ZVS converter's switch, the L-C tank circuit resonates. The voltage across the switch initially traverses linearly from "zero" to Vin, then resonantly to its peak, and back down again to zero. At this instant the switch can be reactivated, and lossless, zero voltage switching facilitated. Since the output capacitance of the mosfet switch (Coss) has been discharged by the resonant tank, it does not contribute as power lossin the switch. Therefore, the mosfet transition losses go to zero - regardless of operating frequency and

input voltage. This represents a significant savings in power, and results in a sustantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Furthermore, the technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback and boost converters, to name a few.

ZVS SWITCH WAVEFORMS

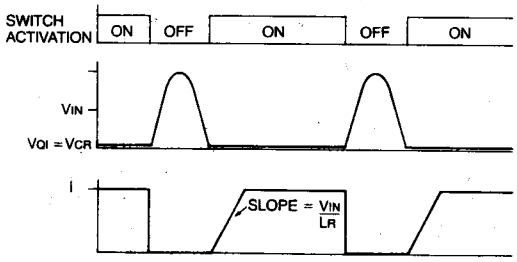

Figure 1.

ZVS BENEFITS

** Zero power "Lossless" switching transitions
** Reduced EMI / RFI at transitions
** No power loss due to discharging Coss
** No higher peak currents than square wave systems - unlike Zero Current Switching
** High efficiency with high voltage inputs - independant of conversion frequency
** Can incorporate parasitic circuit and component inductance and capacitance
** Reduced gate drive , no "Miller" effects
** Short circuit tolerant

ZVS DIFFERENCES

** Variable frequency operation (in general)
** Higher off-state voltages in single switch, unclamped topologies
** Relatively new technology (learning curve)
** Conversion frequency is inversely proportional to load current
** A more sophisticated control IC may be required

CONTROL CIRCUIT FUNDAMENTALS

Requirements for the Zero Voltage Switching generation of control ICs differ immensely from that of the more traditional pulse-width modulator. In fact, the two are direct opposites regarding the control circuit implementation in many respects, with similarities existing only amongst the housekeeping and gate drive attributes.

ERROR AMPLIFIER

The core of variable frequency operation focuses upon the error amplifier (E/A). The power supply output voltage (Vout) is sensed, compared to a reference input and the difference is amplified by the gain of the error amplifier. The resulting error voltage (Ve) signifys the need for the control circuit to respond to a change in the power supply's output voltage, typically caused by a line or load variation. This error voltage drives a voltage controlled oscillator (VCO) which decreases the conversion frequency with increasing error voltages, as required. An ideal amplifier should feature a high slew rate for fast transient response in addition to high gain-bandwidth for high frequency applications.

VOLTAGE CONTROLLED OSCILLATOR

The voltage controlled oscillator needs to incorporate three programmable functions to satisfy the ZVS control circuit requirements; minimum conversion frequency, maximum conversion frequency and the voltage-to-frequency gain of the VCO. Programmability should request a minimal amount of external components for typical ranges in operating frequencies extenting into the megaHertz sector.

ONE-SHOT TIMER

The VCO output clocks the one-shot circuitry which generates the off-time for the ZVS switch. While a fixed off-time is generally associated with these ZVS converters, the "real" off-time can vary significantly. In most applications, a three-to-one variation in off-time is not uncommon, and necessary to accommodate the resonant components initial accuracies, temperature effects, line and load range combinations. A preferred approach is to program the maximum off-time at the one-shot and modulate it with a true zero voltage detection circuit. To state it quite simply, a fixed off-time control technique can NOT guarantee optimal zero voltage switching over all operating conditions.

ZERO VOLTAGE DETECTION

A zero crossing detection circuit is incorporated in the UC 1861/64 family of devices to implement "true" zero voltage switching. A precision threshold of 0.5 volts is compared to the ICs ZERO input, a representation of the switch drain-to-source voltage. When the falling edge of this waveform crosses the threshold, the ZERO detection comparator forces a change in the one-shot status, terminating its output. Numerous arrangements of external components provide the flexibility to adapt this feature to a wide range of ZVS switch topologies and applications. The drain-to-source voltage can be resistively scaled to the proper levels in high voltage applications, and offset above ground in low power usages.

PROTECTION CIRCUITRY

SOFT-START

Upon power-up the ZVS switch should start operation at the maximum conversion frequency, corresponding to the maximum switch off-time for an effective zero "duty" cycle. As the soft start circuitry lowers the conversion frequency the switch on-time starts at zero and gradually widens, increasing the effective duty cycle hence output power.

RESTART DELAY

Once a short circuit or overload on the power supply output has been detected, the IC controller needs to perform several functions. First, turn the output(s) off as quickly as possible (nanoseconds) to prevent a catastrophic failure of the supply. Second, the outputs should remain off for a programmed restart delay interval, one designed long enough to allow operation into a short circuit for extended periods of time (forever) without failing. Often called "Hiccup", this mode will subsequently restart the controller's output(s) in soft start under full fault protection once the restart delay period has concluded.

CLOSED LOOP START-UP

A preferred method to start or restart a power system is under full closed-loop control. The soft-ref feature of the UC1861/64 controllers is intened to be used as the reference input to the error amplifier to facilitate closed loop start-up. Rather than simply clamping the output of the error amplifier as in a converntional PWM, this soft reference configuration controls the increasing power supply output voltage until regulation is attained. Additionally, only a single IC pin and one capacitor is used to provide both soft start and restart delay with user programmable fault management options.

UC 1861 / UC 1864 BLOCK DIAGRAM

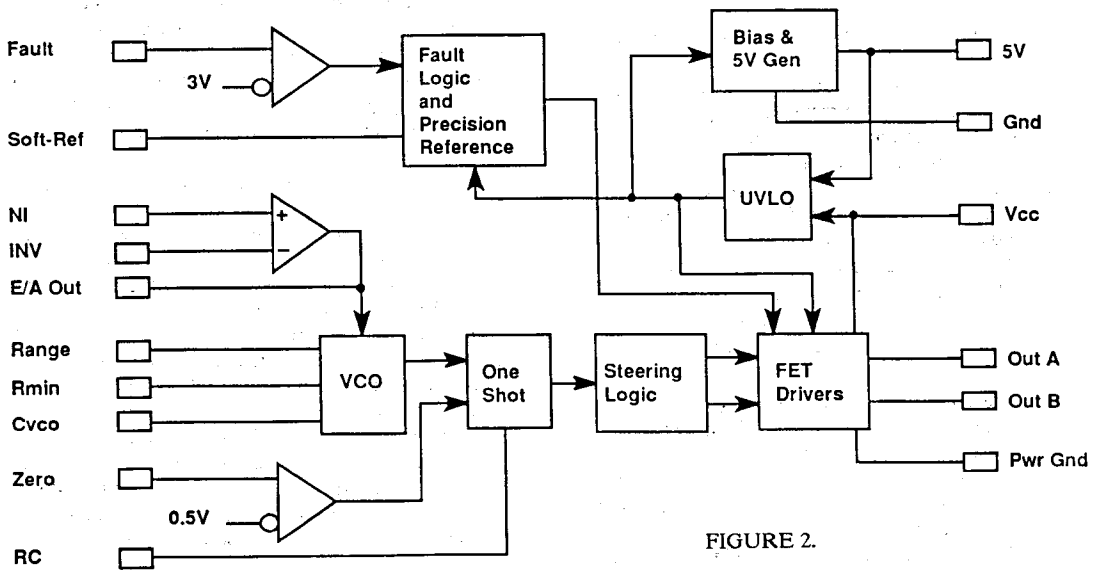

FIGURE 2.

ZVS - QRC FORWARD CONVERTER : DESIGN EXAMPLE AND PROCEDURE

TIMING INTERVALS AND DESIGN EQUATIONS

A zero voltage switched Forward converter will be used to develop the design equations for the various voltages, currents and time intervals associated with each of the conversion periods which occur during one complete switching cycle. The circuit schematic, component references, and relevent polarities are shown in figure 3.

A valid assumption is that the output filter section consisting of output inductor (Lo) and capacitor (Co) has a time constant of several orders of magnitude larger than any power conversion period. The filter inductance is large in comparison to that of the resonant inductor's value (Lr) and the magnetizing current (delta ILo) as well as the inductor's DC resistance is negligible. In addition, both the input voltage (Vin) and output voltage (Vo) are purely DC, and do not vary during a given conversion cycle. Additionally, the transformer is also ideal with a turns ratio of 1:1, thus allowing the simplification of this circuit to that of a Buck regulator. Last, the converter is operating in a stable, closed loop configuration which varies the conversion frequency in order to regulate the output voltage (Vo).

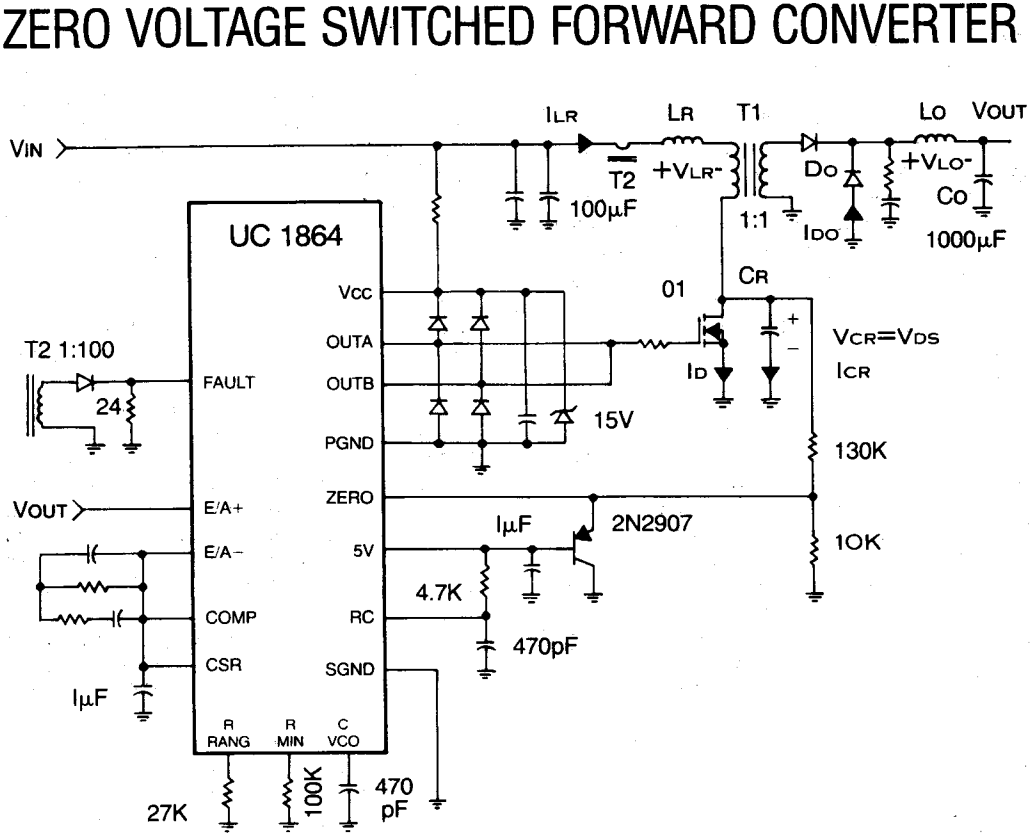

FIGURE 3. SCHEMATIC DIAGRAM

INITIAL CONDITIONS: t < t0

The analysis will begin with the switch (Q1) ON, conducting a drain current (Id) equal to the output current (Io), and Vds = VCr = 0 (ideal). In series with the switch (Q1) is the resonant inductor and the output inductor, also conducting the output current (Io). The voltage across the output inductor equals the input to output voltage differential; VLo = Vin - Vo. The output filter section catch diode is not conducting and sees a reverse voltage equal to the input voltage; VDo=Vi, observing the polarity shown in figure 3.

Q1 is ON , Vds = VCr = 0 ;
Id = ILr = ILo = Io
Do is OFF, VDo = Vin ; IDo = 0
ILr = Io ; VLr = 0
VLo = Vin - Vo; ILo = Io

CAPACITOR CHARGING STATE
Time interval: t0 < t < t1

The conversion period is initiated at time t0 when the switch is turned OFF. Since the current through the resonant inductor and output inductor cannot change instantaneously, and no drain current flows in Q1 while it is off, the current is diverted around the switch through the resonant capacitor. This constant output current of Io will linearly increase the voltage across the resonant capacitor until it reaches the input voltage (VCr = Vin). Since the current is not changing, neither is the voltage across the resonant inductor.

At time t0 the switch current "instantly" drops from Io to zero. Simultaneously, the resonant capacitor current snaps from zero to Io, while the resonant inductor current and output inductor current remains constant and equal also to Io over the duration of this span from t0 to t1. Voltage across the output inductor and output catch diode is linearly decreasing from time t0 to t1 due to the linearly increasing voltage across the resonant capacitor, Cr. This interval ends at time t1 when VCr equals Vin, and the output catch diode starts to conduct.

Q1 is OFF; Id=0; Vds(t)=VCr(t)
ICr(t)=Io; VCr(t)=[Io * t] / Cr
ILr(t)=Io; VLr=0
VDo(t) = Vin - [Io * t]/Cr
VLo(t0) = VDo - Vo

RESONANT STATE
Time interval: t1 < t < t2

The resonant portion of the conversion cycle begins at time t1 when the voltage across the resonant capacitor equals the input voltage, and the output catch diode begins conducting. Current through the resonant components at time t1 equals the output current.

The stimulus for this series resonant L-C circuit is output current flowing through the resonant inductor prior to time t1. The ensueing resonant tank current follows a cosine fuction beginning at time t1, and ending at time t2. At the natural resonant frequency (Wr), each of the L-C tank components exhibit an impedance equal to the tank impedance, Zr. Therefore, the peak capacitor voltage and peak OFF switch voltage is a function of the tank impedance and the load current.

Of great importance is the ability to solve the equations for the precise switch off-time which varies with line and load changes. While some allowance does exist for a fixed off time technique, the degree of latitude is insufficient to accommodate typical input and output variations.

The absolute maximum duration for this interval occurs when 270 degrees [(3/2) * Pi * Wr] of resonance is required to intersect the zero voltage axis. This corresponds to the limit of resonance as minimum load and maximum line are approached.

Prior to time t1, the catch diode was not conducting. Its voltage was linearly decreasing from Vin at time t0 to zero at t1 while the input source was supplying full output current. At time t1, however, this situation changes as resonance is initiated, diverting the resonant inductor current away from the output filter section. Instantly, the output diode voltage changes polarity as it conducts, supplementing the decreasing resonant inductor current with a diode current, extracted from stored energy in the output inductor. The diode current waveshape follows a cosine function during this interval, equalling Io minus ICr(t).

Vds(t)=VCr(t)=Vin+{Io*Zr*SIN[Wr(t-t1)]}
ILr(t)=ICr(t)=Io*COS[Wr(t-t1)]
VLr(t)=[Io*Zr*SIN[Wr(t-t1)]
IDo(t)=Io-ILr(t)

ZVS FORWARD WAVEFORMS

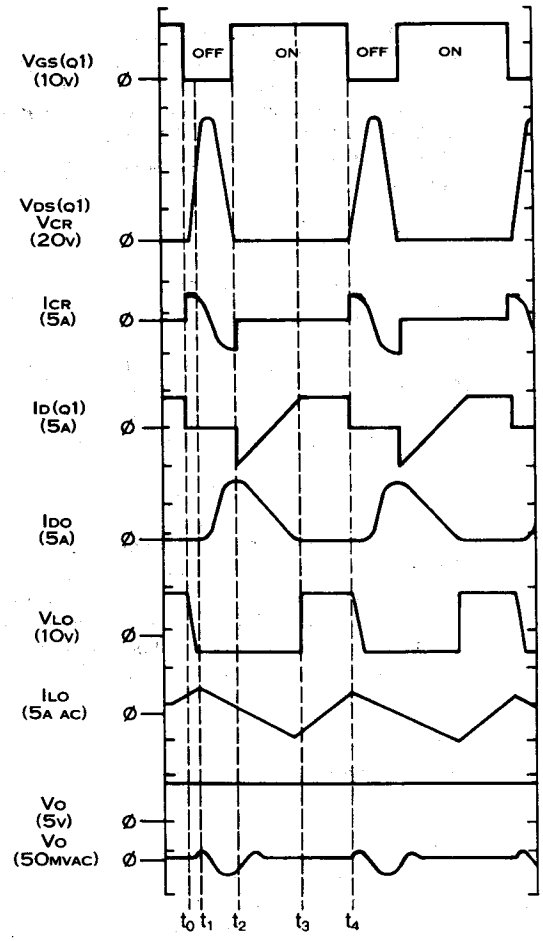

FIGURE 4 .

INDUCTOR CHARGING STATE
Time interval: t2 < t < t3

To facilitate zero voltage switching, the switch is activated once the voltage across the switching device and the resonant capacitor has reached zero, occurring at time t2. During the interval from t2 to t3, the resonant inductor current is linearly returned from its negative peak of minus Io to its positive level of plus Io.

The output filter section catch diode conducts during this interval, continuing to freewheel the full output current, and clamping one end of the resonant inductor to ground through the output diode. The voltage across the resonant inductor is equal to Vin - VDo resulting in a linearly rising resonant inductor current along with a linearly decreasing catch diode current. Energy stored in the output inductor is providing the output power to the load during this interval.

A noteworthy peculiarity during this timespan can be seen in the switch drain current waveform. At time t2, when the switch is turned on, current is actually returning from the resonant tank to the input source, Vin. An interesting diversion is that the switch can virtually be turned on at leisure during the first half of the t2 to t3 interval at any time without interfering with normal operation. A seperate time interval could be used to identify this region if necessary.

$ILr(t)=ID(t)= -Io+[(Vin+VDo)/Lr]*t \quad t2<t<t3$
$VLr=Vin+VDo$
$IDo(t)=Io-ILr(t) \quad t2<t<t3$
$ILo=Io \; ; \quad VLo= - Vo+VDo$

POWER TRANSFER STATE
Time interval : t3 < t <t4

Once the resonant inductor current has reached the output current at time t3, the zero voltage switched converter resembles that of a conventional square wave power processor. During the remainder of the conversion period, most of the pertinant waveforms approach DC conditions.

With switch Q1 closed, the input source is supplying the output current, and the output filter inductor voltage equals Vin minus Vout. Both the switch current and resonant inductor currents are equal to the output current.The output catch diode voltage equals Vin, and no current flows.

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In closed loop operation where the output voltage is in regulation, the control circuit essentially varies the on-time of the switch during the timing interval between t3 and t4. Variable frequency operation is the result of modulating the on-time as dictated by line and load conditions. Increasing the ON time duration, or lowering the conversion frequency has the same effect as widening the duty cycle in a traditional square wave converter.The conversion frequency is inversely proportional to output load.

Vds=Io*Rds(on) ; Id=Io
VLo=Vin-Vo ; ILo=Io
VDo = Vin

TIMING INTERVAL SUMMARY

dt10 = (Cr * Vin) /Io
dt21 = (Pi/Wr) + (1/Wr)ARCSIN[Vin/(Io*Zr)]
dt32 = (2*Io*Lr) / Vin
dt43 = (Vo*dt30) / (Vin-Vo)
where dt30=dt10+dt21+dt32

and the conversion period (tconv)=
dt40=dt10+dt21+dt32+dt43

CONTROL CIRCUIT PROGRAMMING

Determination of the range of required ON and OFF durations of the control circuit is necessary to program the UC3864s VCO and one-shot timer. Equally as important is the need to analyze these variations to accommodate changes in line voltages, load currents, component initial tolerances and temperature effects. Once obtained, the minimum and maximum operating frequencies define the VCO timing component values. Additionally, the one shot timer is programmed for the maximum on-time, and modulated by the ZERO detect circuitry to facilitate true zero voltage switching. [9]

OFF - TIME

The OFF-TIME of the switch and controller includes the linear charge and resonant intervals which begin at time t0 and end at time t2.

t off = t10 + t21

MAXIMUM OFF - TIME

The maximum off-time is used to program the one-shot timer which corresponds to :
t off max = dt10 max + dt21 max

t off max = [1 + (1.5 * Pi)] / Wr
= 0.909 / Fres

MAXIMUM CONVERSION FREQUENCY

The maximum conversion frequency occurs as both the switch ON-TIME and OFF-TIME go to their minimum value. For the circuit to remain resonant, the inductor charging interval limitations must be satisfied, therefore dt32 cannot go to zero. However, the power transfer interval, dt43, can, although the output will be out of regulation. [10]

MINIMUM ON - TIME

t on MIN = dT32 MIN + dT43 MIN
= 1/(Pi * Fres) = 0.318 / Fres

The conversion period (t40) is the sum of the four timing intervals and equal to the ON plus OFF times of the switch. The conversion frequency, Fconv, is the reciprocal of the conversion period.

f conv = 1/ tconv = 1 / t40

Both minimum and maximum conversion frequency need to be calculated to program the UC3864 VCO, a task best performed by a personal computer. The program should accommodate component initial tolerances, diode and switch voltage drops versus output currents, in addition to the temperature effects on all.

ZVS FORWARD CONVERTER DESIGN SPECIFICATIONS

A low voltage DC/DC converter design has been selected for the purposes of generalization and simplicity. Each of the previously listed equations will be utilized to determine the circuit specifics and can be altered by the user to accommodate circuit and device losses. A resonant tank frequency of 500 KiloHertz will be incorporated as a compromise between high frequency operation and minimal circuit and device parasitic interference. The maximum conversion frequency of this design will approach that of the resonant tank , but never exceed it in normal operation.

SPECIFICATIONS

Vin = 18 to 26 VDC
Vout = 5.0
Iout = 2.5 to 10 ADC
Fres = 500KHz

INTERVAL DURATIONS : t10 - t43

VARIATIONS WITH LINE & LOAD

	VIN=18		VIN=26	
	IO=2.5	IO=10	IO=2.5	IO=10
(uSec)				
dT10	0.217	0.055	0.314	0.078
dT21	1.29	1,06	1.49	1.08
dT32	0.93	3.72	0.64	2.58
dT43	1.39	6.68	0.78	1.78
Tconv	3.83	11.51	3.23	5.52
Fcon	261K	87K	310K	181K

SWITCH DURATIONS (uSec)

Toff	1.51	1.11	1.80	1.16
Ton	2.32	10.4	1.42	4.36

The ZVS Forward converter gain in kiloHertz per volt of Vin (KHz/V) and amp of Iout (KHz/A) can be evaluatated over the specified ranges. As summary of these follows.

AVERAGE d(Fconv) / d(Vin) vs Iout

Io =	2.5A	5A	7.5A	10A
dF/dV =	11.25	11.8	11.75	10.25

Average d(Fconv) / d(Vin) = 11.26 KHz/V

The highest gain of 11.87 KHz/V occurs near full load.

AVERAGE d(Fconv) / d(Io) vs Vin

Vin =	18	20	22	24	26
dF/dI =	23.3	22.1	20.5	18.8	17.3

AVERAGE dF/dI (KHz/A) = 20.4

The highest gain of 23.3 KHz/A occurs at Vin min.

It may be required to use the highest gain figures to compensate the control loop for stability over all operating conditions. While this may not optimize the loop transient response for all operating loadlines, it will guarantee stability over the the input and ouput variations.

PROGRAMMING THE CONTROL CIRCUIT

ONE - SHOT : ACCOMMODATING OFF - TIME VARIATIONS

The switch off-time varies with line and load by approximately +/- 35% in this design example using ideal components. Accounting for initial tolerances and temperature effects will result in an much wider excursion. For all practical purposes, a true fixed off-time technique will NOT work as previously mentioned. Incorporated into the UC3861 family of ZVS controllers is the ability to modulate this off-time. Initially, the one-shot is programmed for the maximum off-time, and modulated via the ZERO detection circuitry. The switch drain-source voltage is sensed and scaled to initiate turn-on when the precision 0.5V threshold is crossed. This offset was selected to accommodate propogation delays between the instant the threshold is sensed and the instant that the switch is actually turned on. Although brief, these delays can become significant in high frequency applications, and if left unaccounted, can cause NONZERO switching transitions.

In this design, the off-time varies between 1.11 and 1.80 microseconds, using ideal components and neglecting any temperature effects on the resonant components. Since the ZERO detect logic will facilitate "true" zero voltage switching, the off-time can be set for a much greater period. The one-shot has a minimum of 5:1 (minimum to maximum) range of duration, and will programmed for 3.0 uS (max), controllable down to 0.60 uS. Programming of the one-shot requires a single R-C time constant and is straighforward using the design information and equations from the datasheet. Implementation of this feature is shown in figure 3.

PROGRAMMING THE VCO

The calculated range of conversion frequencies spans between 87 KHz and 310 KHz which will be used for this "first cut" draft of the control circuit programming. Due to the numerous circuit specifics omitted from the computer program for simplicity, the actual range of conversion frequencies will probably be somewhat wider than planned. Later, the actual timing component values can be adjusted to accommodate these differences. First, a minimum conversion frequency of 75 KHz has been selected

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and programmed according to the following equation:
Fvco min = 3.6 / (Rmin * Cvco)

The maximum conversion frequency of 350 KHZ is programmed by:
Fvco max = 3.6 / [(Rmin || Rrange) *Cvco]

Numerous values of Rmin and Cvco will satisfy the equations which can be simplified by letting Rmin equal 100K.

Cvco (uF) = 0.036 / Fmin(KHz)
Rrange(K)= 100 / [(Fconv max/Fconv min) - 1]
where Rmin= 100 K , Cvco= 480 pF (use470pF)
Rrange= 27.2 K

The VCO gain in frequency per volt in from the error amplifier output is approximated by :
dF/dV = 1 / (Rrange * Cvco) = 78.2 KHz / V
with an approximate 3.6 volt delta from the error amplifier.

ZERO DETECTION CIRCUIT

True zero voltage switching occurs every cycle as the ZERO detection circuitry modulates the width of the one-shot output. The falling edge of the resonant capacitor waveform is sensed, resistively scaled and fed to one input of the the ZERO comparator. Its other input is a precision 0.5 volt reference and the output is tied to the one-shot. Once the half-volt threshold is crossed, the one-shot output is clocked, thus terminating the output and initiating the next VCO timing pulse. Typical operation is show in figure 5.

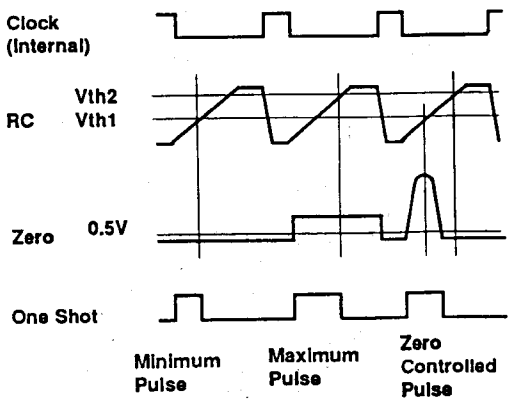


Figure 5.

FAULT PROTECTION- SOFTSTART & RESTART DELAY

One of the many unique features of the UC 3861 family of resonant mode controllers can be found in its fault management circuitry. A single pin connection interfaces with the soft start, restart delay and programmable fault mode protection circuits. In most applications, one capacitor to ground will provide full protection upon power-up and during overload conditions. Users can reprogram the timing relationships or add control features (latchoff following fault, etc) with a single resistor to ground or Vcc.

Selected for this application is a 1 uF soft-restart capacitor value, resulting in a soft-start duration of 10 milliseconds and a restart delay of approximately 200 milliseconds. The pre-programmed ratio of 19:1 (restart delay to softstart) will be utilized. Primary current will be utilized as the fault trip mechanism, indicative of an overload or short cirucit current condition. A current transformer is incorporated to maximize efficiency when interfacing to the three volt fault threshold. Core reset is accomplished by the bidirectional resonant current in this transformers primary.

TIMING EQUATIONS:

SOFT START (Tss)
Tss = Csr * 10K ohms

RESTART DELAY Trd
Trd = Csr * 190 K ohms

TIMING RATIO (Trd:Tss)
APPROX 19:1

GATE DRIVE

Another unique feature of the UC 3861-64 family of devices is the optimal utilization of the silicon devoted to output totem pole drivers. Each controller uses two pins for the A and B outputs which are internally configured to operate in either unison or in an alternating configuration. Typical performance for these 1 Amp peak totem poles shows 30 nanosecond rise and fall times into 1nF. One significant advantage of zero voltage switching is the reduced "miller" effects at the fet gates - the switch is only transitioned while Vds has reached zero, substantially reducing the gate drive requirements.

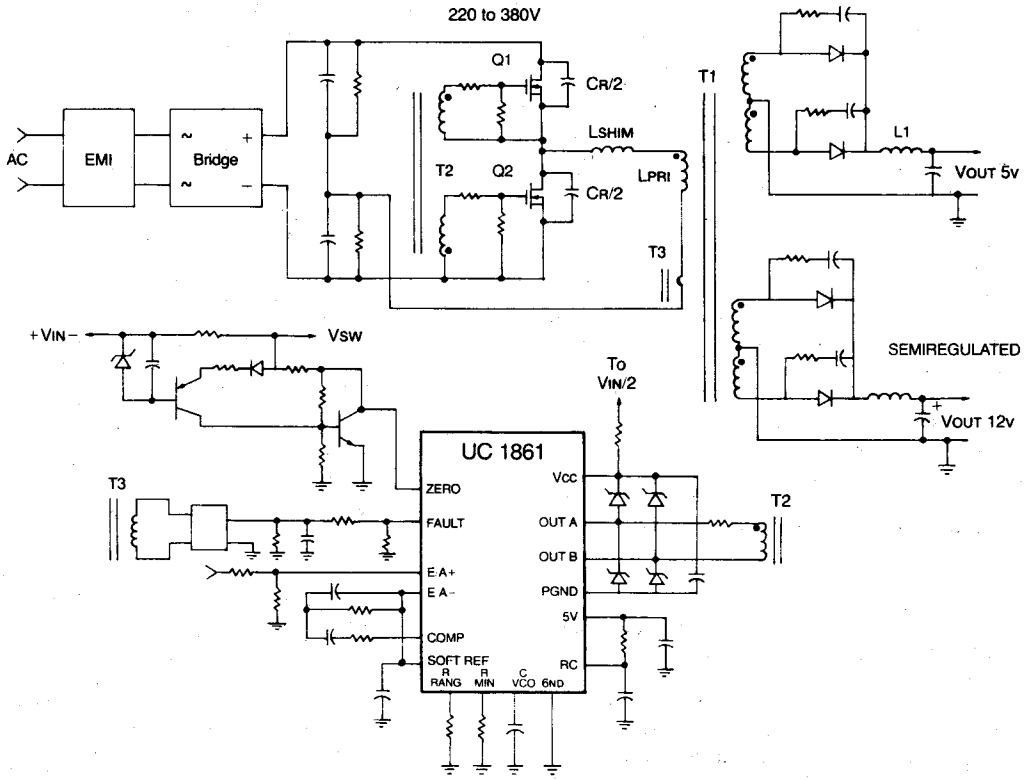
LOOP COMPENSATION GENERAL INFORMATION

The ZVS technique is similar to that of conventional voltage mode square wave conversion which utilizes a single voltage feedback loop. Unike the dual loop system of current mode control, the ZVS output filter section exhibits a two pole-zero pair and is compensated accordingly. Generally, the overall loop is designed to cross zero dB at a frequency below one-tenth that of the switching frequency. In this variable frequency converter, the lowest conversion frequency will apply, corresponding to approximately 85 KHz, for a zero crossing of 8.5 KHz. Compensation should be optimized for high low frequency gain in addition to ample phase margin at crossover. Typical examples utilize two zeros in the error amplifier compensation at a frequency equal to that of the output filters two pole break. An additional high frequency pole is placed in the loop to combat the zero due to the output capacitance ESR, assuming adequate error amplifier gain-bandwidth.

ZVS HALF - BRIDGE

The foundation of zero voltage switching can be extended to multiple switch topologies for higher power levels, specifically the half and full bridge configurations. While the basic operation of each time interval remains quite similar, ther is a difference in the resonant interval, t1-t2.

ZERO VOLTAGE SWITCHED HALF-BRIDGE CONVERTER



Unlike the single switch converter's high off-state voltage, the bridge circuits clamp the voltage excursions to the DC input rails, thereby reducing the switch voltage stress and requirements. This alters the duration of the off segment of the resonant interval since the opposite switch(es) must be activated long before the resonant cycle were to have been completed. In fact, the opposite switch(es) should turn on immediately ofter their voltage is clamped to the rails while their drain-to-source voltage equals zero. If not, the resonant tank will continue its resonance and return the switch voltage to its starting point, the opposite rail. Additionally, this off period varies with line and load changes. To guarantee true zero voltage switching, it is necessary to incorporate a zero voltage detection circuit, and modulate the controller's programmed off-time. The circuitry shown connected to the UC1861 ZERO input performs the attenuation and sensing to interface to the switch voltage in this half-bridge design.

THE UC1861 CONTROLLER

The UC1861 controller is similar to the UC1864, and incorporates a toggle flip-flop to generate the alternating A and B outputs for half and full bridge applications. All other programmable features and connections remain identical to the UC1864 IC. Each device is optimized for controlling zero voltage switched converters at frequencies into the megahertz with minimal parts count and interface logic.

SUMMARY

The zero voltage switched quasi-resonant technique is applicable to most power conversion designs, but is most advantageous to those operating from a high voltage input. In these applications, losses associated with discharging of the mosfet output capacitance can be significant at high switching frequencies, imparing efficiency. Zero voltage switching avoids this penalty by negating the drain-to-source, "off-state" voltage via the resonant tank.

A high peak voltage stress occurs across the switch during resonance in the buck regulator and single switch forward converters. Limiting this excursion demands limiting the useful load range of the converter as well, an unacceptable solution in certain applications. For these situations, the zero voltage switched multi-resonant approach [11,12] could prove more beneficial than the quasi-resonant ZVS variety.

Significant improvements in efficiency can be obtained in high voltage, half and full bridge ZVS applications when compared to their square wave design complements. Clamping of the peak resonant voltage to the input rails avoids the high voltage overshoot concerns of the single switch converters, while transformer reset is accomplished by the bidirectional switching. Additionally, the series transformer primary and circuit inductances can beneficial, additives in the formation of the total resonant inductor value. This not only reduces size, but incorporates the detremental parasitics generally snubbed in square wave designs, further enhancing efficiency.

A new series of control ICs has been developed specifically for the zero voltage switching techniques with a list of features to facilitate lossless switching transitions with complete fault protection. The multitude of functions and ease of programmability greatly simplify the interface to this new generation of power conversion techniques; those developed in response to the demands for increased power density and efficiency.

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