Circuit limits dV/dt and capacitor inrush at regulator turn-on

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Unusual design constraints sometimes reveal the unfriendly side of everyday components and circuits. A case in point is the design of power-supply-regulation circuitry in which the primary power source has an absolute current-limit specification, such as spacecraft photovoltaic, or "solar," panels and radioisotope-thermoelectric generators. Such applications require that you pay scrupulous attention to strict control of current consumption, including transient-current consumption, and infrequent consumption spikes, such as those that typically occur on power-up. The problem is that current-limited primary-power sources can suffer catastrophic voltage droop and shutdown in response to momentary overcurrent faults, even when the fault is brief. Common causes of such faults are the current spikes that charge the regulator output's decoupling capacitor.

Unless the current limit of the regulator clips the resulting spikes, the spikes are equal to the regulator's output-voltage rate of rise multiplied by the sum of the parallel output capacitances: $I_{MAX}=dV/dt\times C_{OUT}$, where I_{MAX} is the maximum current, dV/dt is a differential in voltage with respect to a differential in time, and C_{OUT} is the output capacitance. The math suggests that the best strategy for limiting the regulator's turn-on maximum current is

to limit dV/dt. The circuit in **Figure 1** relies on this trick and works with industry-standard adjustable linear regulators, such as the popular low-dropout LM2941.

The basis of the dV/dt-limiting technique comprises the six added components: R_3, R_4, C_T, D_1, D_2, and Q_1. On power-up, the control current through R_3, C_T, and D_2 delays the rise of the output voltage and thus prevents excessive maximum-current transients.

Here's how it works. When V_{IN} is on and Q_1 is off, current through R_3, C_T, and D_2 pulls the adjust pin of the regulator to the reference. This action limits V_{OUT}'s dV/dt to the rate of C_T charging through the series resistance, $(R_3+R_1R_2/(R_1+R_2))$, and thereby limits I_{MAX} to any desired value using the design **equations** $R_3=(V_{IN}-V_{REF}-1)/V_{OUT}$, $R_4=<20R_3$, and $C_T=C_{OUT}V_{OUT}/(I_{MAX}(R_3+R_1R_2/(R_1+R_2)))$. For example, given the circuit constants in the **figure** and assuming $C_{OUT}=100$ µF, dV/dt=2500V/s, and $I_{MAX}=0.25$A. At the end of the modified power-up sequence, D_1 and D_2 decouple the dV/dt circuit from the regulator's feedback network, preventing the coupling of ripple voltages from the input voltage into the output voltage. EDN

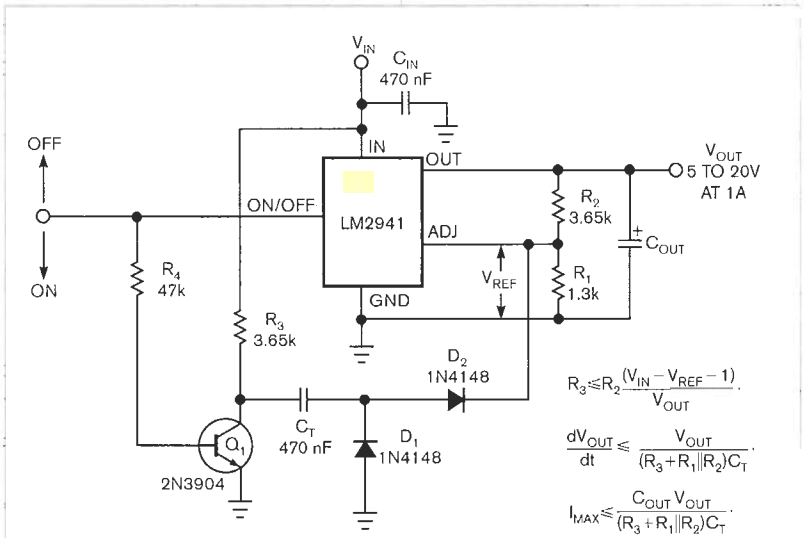

Figure 1 On power-up, the control current through R_3, C_T, and D_2 delays the rise of V_{OUT} and thus prevents excessive I_{MAX} transients.