Application Note 56
Total Power Conversion Solution for Pentium® II Motherboards

Abstract

This application note provides detailed design procedures for the development of Core, GTL+ and Clock supplies for Intel Pentium® II motherboards using Fairchild Semiconductor's RC5055 triple controller.

Introduction

As the demand for increased integration grows, the RC5055 combination PWM controller and Low Dropout Regulators (LDOs) constitute a simple and cost effective solution. The PWM controller implements robust yet flexible voltage-mode control architecture combined with 1% accurate reference, over voltage protection and over current protection employing MOSFET $R_{DS(ON)}$. The step down DC-DC converter can deliver up to18A of continuous load current at voltages ranging from 1.3V to 3.5V. A specific application circuit, design considerations, component selection, PCB layout guidelines, and performance evaluations are covered in detail.

Intel Pentium II Processor Power Requirements

Refer to Intel's AP-587 Application Note, Slot 1 Processor Power Distribution Guidelines, May 1997 (order number 243332-001), as a basic reference.

Available inputs are +12V±5% and +5V±5%. The input voltage requirements for Fairchild's RC5055 DC-DC converter are listed in Table 1.
See below for detailed information on how to apply these.

Table 1. Input Voltage Requirements

Part #	Vcc for IC	MOSFET Drain
RC5055	+12V ±5%	+5V ±5% or 12V ±5% For switching Converter
		3.3V ±5% For Clock and Vtt

DC Voltage Regulation

The voltage level supplied to the CPU must be within ±3% of its nominal setting. Voltage regulation limits must include:

- Output load range
- Output ripple/noise
- DC output initial voltage set point
- Temperature and warm up drift (Ambient +0°C to +70°C at full load with a maximum rate of change of 5°C per 10 minutes but no more than 10°C per hour)
- Output load transient with:
- Slew rate >30A/µs at converter pins
  Range: 0.3A - I_{CCP} Max.

Output Ripple and Noise

Ripple and noise are defined as periodic or random signals over the frequency band of 0 - 20MHz at the output pins. Output ripple and noise must be consistent with voltage requirements throughout the full load range and under all specified input voltage conditions.

Efficiency

The efficiency of the DC-DC converter must be greater than 80% at maximum output current and greater than 40% at low current draw.

Processor Voltage Identification

There are five Voltage Identification Pins, VID0-VID4, on the Pentium II processor package which can be used to support automatic selection of the power supply voltage. These pins are either internally unconnected or are shorted to ground (VSS). The logic status of the VID pins defines the voltage required by the processor.

I/O Controls

In addition to the Voltage Identification, there is a signal that provides feedback from the DC-DC converter to the CPU. This is the Power-Good (PWRGD) signal, which will be discussed later.

RC5055 Description

Simple Step-Down Converter

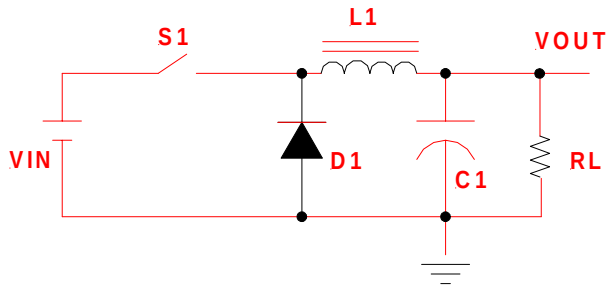

Figure 1. Simple Buck DC-DC Converter

For the purpose of understanding a buck converter, Figure 1 illustrates a step-down DC-DC converter with no feedback control. The operation of the basic step-down converter is the basis for the design equations for the Pulse Width Modulation (PWM) controller in the RC5055. Referring to Figure 1, the basic operation begins by closing the switch S1. When S1 is closed, the input voltage V_{IN} is applied to inductor L1. The current flowing in this inductor increases, and the increase is given by the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})T_{ON}}{L1}$$

where T_{ON} is the time S1 is closed (the duty cycle is T_{ON} / T_S, with T_S the switching period). When S1 opens, the diode D1 conducts the inductor current and the output current is delivered to the load; the inductor current decrease is given by:

$$\Delta I_L = \frac{V_{OUT}(T_S - T_{ON})}{L1}$$

where (TS - TON) is the time during which S1 is open.

By solving these two equations, we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_{OUT} = V_{IN}\frac{T_{ON}}{T_S}$$

In order to obtain a more accurate approximation for V_{OUT} , we must also include the forward voltage V_D across diode D1 and the voltage across the switch , V_{SW} . After taking into account these factors, the new relationship becomes:

$$V_{OUT} = (V_{IN} + V_D - V_{SW})\frac{T_{ON}}{T_S} - V_D$$

Where V_{SW} is the voltage across the MOSFET in the on state and is equal to $\approx I_L * R_{DS(ON)}$.

The RC5055 PWM Controller

The RC5055 has a programmable synchronous DC-DC controller. When designed around the appropriate external components, it can be configured to deliver more than 18A of output current. The RC5055 utilizes voltage-mode PWM control.

Main Control Loop

Refer to the RC5055 Block Diagram illustrated in Figure 2. The control loop of the regulator contains two main sections: the analog control section and the Gate Control Logic block. The analog section consists of signal conditioning error amplifier feeding into a comparator, which provide the inputs to the Gate Control Logic block. The error amplifier amplifies the difference between the feedback signal and the voltage reference (DACOUT) and presents the output to the comparator, which provides the main PWM control signal to the Gate Control Logic block.

The monitor and protection section comprises the soft start section, short circuit protection section and the over-voltage protection section.

The Gate Control Logic block takes the comparator output and the main clock signal from the oscillator to provide the appropriate pulses to the Upper Gate (UGATE) and Lower Gate (LGATE) output pins. These pins control the external power MOSFETs. The Gate Control Logic block utilizes high speed Schottky transistor logic, allowing the RC5055 to operate at clock speeds as high as 1MHz.

High Current Output Drivers

The RC5055 contains two identical high current output drivers that utilize high-speed bipolar transistors in a push-pull configuration. Each driver is capable of delivering 0.5A of current in less than 100ns. The driver's power and ground (BOOT & PGND) are separated from the chip's power and ground (VCC & GNDA) for additional switching noise immunity. A dead time of a few nano seconds guard against the upper and lower MOSFETs conducting simultaneously during turn on and turn off.

Internal Voltage Reference

The reference included in the RC5055 is a precision band-gap voltage reference. The internal resistors are precisely trimmed to provide a near zero temperature coefficient

(TC). Added to the reference input is the resulting output from an integrated 5-bit DAC—provided in accordance with the Pentium II specification guidelines. These guidelines require the DC-DC converter output to be directly programmable via a 5-bit voltage identification (VID) code. This code scales the reference voltage from 2.0V (no CPU) to 3.5V in 100mV increments, and between 1.3V and 2.05V in 50mV increments.

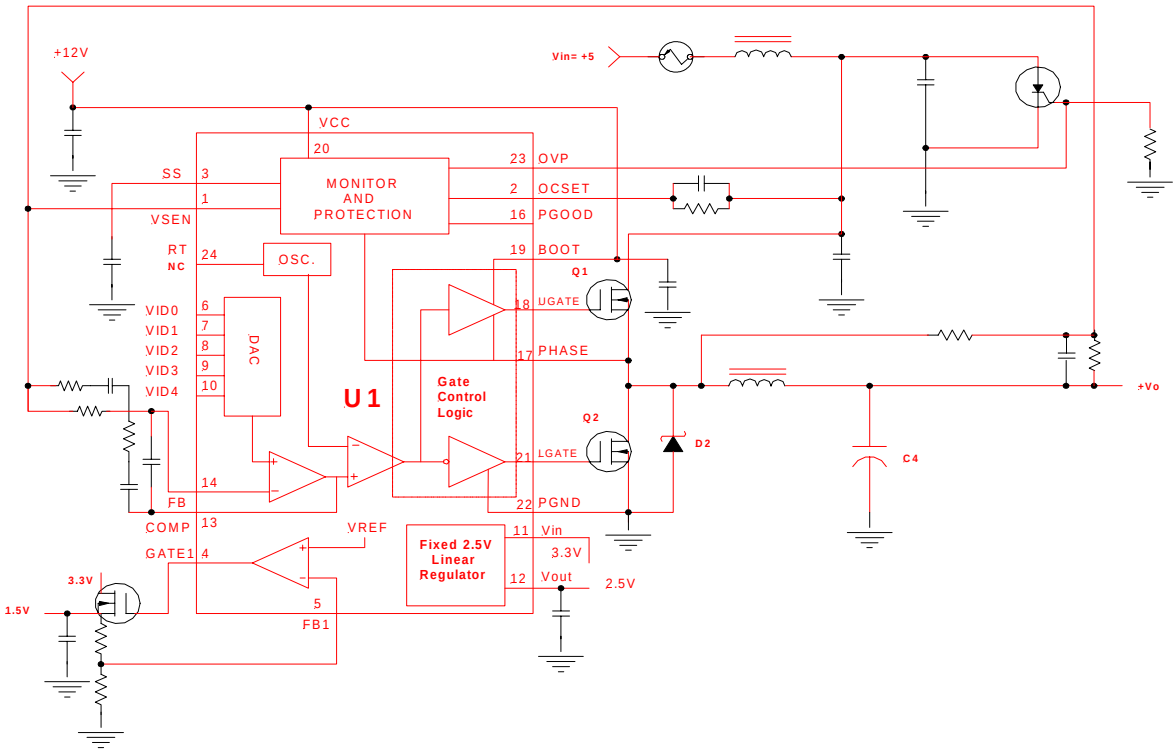

Figure 2 RC5055 Block Diagram

Power Good (PGOOD)

The RC5055 Power Good function is designed to provide a constant voltage monitor on VSEN and LVOUT (V_{clock}) . The circuit compares the VSEN signal to the DACOUT voltage and outputs an active-low interrupt signal to the CPU when the power supply voltage differs more than ±10% from nominal. In the case of V_{clock} the Power Good flag is pulled down if the 2.5Volt clock supply is less than 60% of its design value. The Power Good flag provides no other control function to the RC5055.

Over-Voltage Protection

The RC5055 constantly monitors the PWM output voltage for protection against over voltage conditions. If the voltage at the VSEN pin exceeds 15% of the selected program voltage, an over-voltage condition is assumed and the chip provides a high voltage at OVP pin to drive an external SCR to short out the input supply causing a fuse to blow and hence disconnects power to the microprocessor.

Over-current Protection

The RC5055 uses the $R_{DS(ON)}$ of the upper switching MOSFET as the current sense resistor. A current sense methodology is implemented to cause the IC to go into a hick-up mode when over-current is detected. During the hick-up mode, the controller goes through soft start where the duty cycle drops to zero and then increases gradually to the required duty cycle dictated by the VID pins. This hick-up action will continue until the over-current condition is removed. The soft start will cause much less stresse to the MOSFETs.
The DC-DC converter returns to normal operation after the fault has been removed.

Oscillator

The RC5055 utilizes a 200kHz free running internal oscillator that can be programmed from 50kHz to 1MHz. An external resistor (R_T) is used to program the oscillator frequency to the desired frequency value. This scheme allows maximum flexibility in choosing external components. In general, a higher operating frequency

decreases the peak ripple current flowing in the output inductor, thus allowing the use of a smaller inductor value. Operation at higher frequencies also decreases the amount of energy storage that must be provided by the bulk output capacitors during load transients.

Unfortunately, the efficiency losses due to switching of the MOSFETs increase as the operating frequency is increased. Thus, efficiency is optimized at lower operating frequencies. A typical operating frequency of 300 kHz was chosen in this Application Note to optimize efficiency while maintaining excellent regulation and transient performance under all operating conditions.

Design Considerations and Component Selection

Figure 3 illustrates a synchronous application using the RC5055 and two linear regulators, 2.5V for the clock and 1.5V for GTL+ termination.

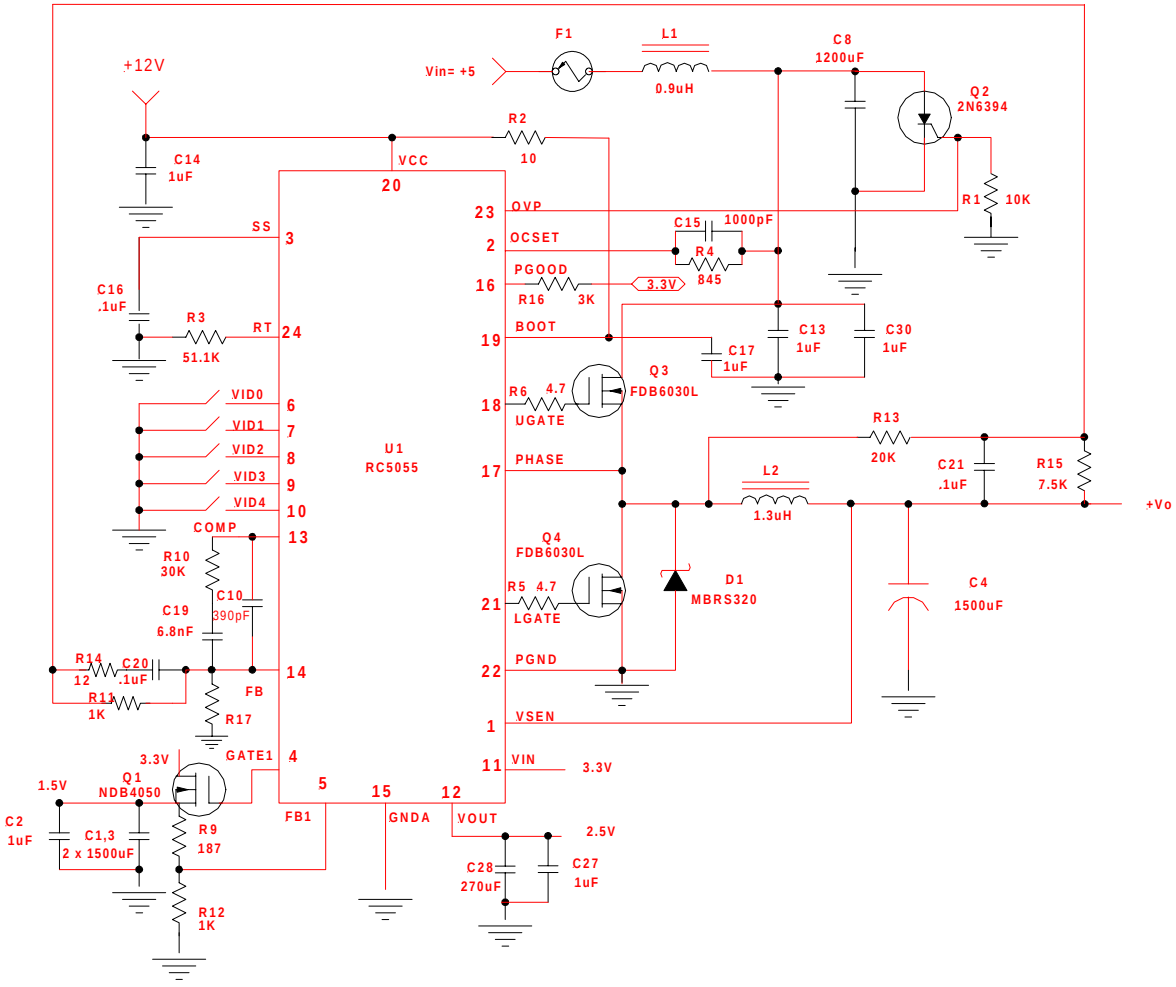

Figure 3. Synchronous DC-DC Converter Application Schematic Using the RC5055

Table 2. RC5055 Application Bill of Materials for Intel Pentium II Processors

Qty.	Reference	Manufacturer	Part Number	Package	Description
1	R1	Various	10KΩ	0805	Resistor, 1%, 0.1W
1	R2	Various	10Ω	0805	Resistor, 1%, 0.1W
1	R3	Various	51.1K	0805	Resistor, 1%, 0.1W
1	R4	Various	1K	0805	Resistor, 1%, 0.1W
1	R5	Various	4.7Ω	0805	Resistor, 1%, 0.1W
1	R6	Various	4.7Ω	0805	Resistor, 1%, 0.1W
1	R8????	Various	845Ω	0805	Resistor, 1%, 0.1W
1	R9	Various	187Ω	0805	Resistor, 1%, 0.1W
1	R10	Various	30.1KΩ	0805	Resistor, 1%, 0.1W
1	R11	Various	1KΩ	0805	Resistor, 1%, 0.1W
1	R12	Various	1KΩ	0805	Resistor, 1%, 0.1W
1	R13	Various	20KΩ	0805	Resistor, 1%, 0.1W
1	R14	Various	12Ω	0805	Resistor, 1%, 0.1W
1	R15	Various	7.5KΩ	0805	Resistor, 1%, 0.1W
3	C8	Sony	10MV1200GX	Radial 10mmx20mm	Aluminum Electrolytic Capacitor, 1200µF, 10V
2	C2,C27	Various	1.0µF Ceramic	1206	Ceramic capacitor, X7R, 16V, 1.0µF
6	C6, C13, C14,C16, C17,C21	Various	0.1µF Ceramic	0805	Ceramic capacitor, X7R, 16V, 0.1µF
7	C4	Sanyo	6MV1500GX	Radial 10mmx20mm	Aluminum Electrolytic Capacitor, 1500µF, 6.3V
1	C15	Various	3.3nF Ceramic	0805	Ceramic capacitor, X7R, 16V, 1000pF
1	C28	Sanyo	6MV330GX	Radial 6.3mmx11mm	Aluminum Electrolytic Capacitor, 330µF, 6.3V
1	C10	Various	3.7nF Ceramic	0805	Ceramic capacitor, X7R, 16V, 6.8nF
1	C19	Various	5.6nF Ceramic	0805	Ceramic capacitor, X7R, 16V, 390pF
1	C20	Various	.1uF Ceramic	0805	Ceramic capacitor, X7R, 16V, 390pF
1	L1			Wound Toroid 18mmx18mmx 9mm	Inductor, 12 Turns, of 16AWG on Micrometals T60-2 Core, 0.9µH
1	L2			Wound Toroid 20mmx20mmx 10mm	Inductor, 9 Turns, of16AWG on Micrometals T50-8/90 Core, 1.3µH
1	D1	Fairchild	MBRS320	DO-214AB	Schottky Rectifier, 3A, 20V
2	Q1, Q2	Fairchild	FDB6030L	TO-263AB	N-Channel MOSFET
1	Q4	Fairchild	NDB4050	TO-263AB	N-Channel MOSFET
1	Q5	Various	2N6394	TO-220	SCR
1	F1	Various			12A, 32Volt , Fast acting subminiature Fuse

MOSFET Selection Considerations

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS(ON)} < 40\ m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} \leq 4.5V$
- Power package with low Thermal Resistance
- Drain current rating of 20A minimum
- Drain-Source voltage > 15V.

The on-resistance $R_{DS(ON)}$ is the primary parameter for MOSFET selection. It determines the power dissipation within the MOSFET and, therefore, significantly affects the efficiency of the DC-DC converter. Table 3 is a selection table for MOSFETs.

Table 3. MOSFET Selection Table

Manufacturer and Part #	Conditions		RDS(ON) Max (mΩ)	Package	Thermal Resistance (°C/W)
Fairchild FDP6030L	V_{GS}=4.5V I_D=21Amp	Tj=25 °C	20	TO-220	θ_{JA}=62.5
Fairchild FDB6030L	V_{GS}=4.5V I_D=21Amp	Tj=25 °C	20	D^2 PAK	θ_{JA}=62.5
Fairchild FDP7030BL	V_{GS}=4.5V I_D=21Amp	Tj=25 °C	12	TO-220	θ_{JA}=62.5
Fairchild FDB7030BL	V_{GS}=4.5V I_D=21Amp	Tj=25 °C	12	D^2 PAK	θ_{JA}=62.5
Fairchild FDP7030L	V_{GS}=5V I_D=40Amp	Tj=25 °C	10	TO-220	θ_{JA}=62.5
Fairchild FDB7030L	V_{GS}=5V I_D=40Amp	Tj=25 °C	10	D^2 PAK	θ_{JA}=62.5
IR IRL2203N	V_{GS}=4.5V I_D=50Amp	Tj=25 °C	10	TO-220	θ_{JA}=62
IR IRL2203S	V_{GS}=4.5V I_D=50Amp	Tj=25 °C	10	D^2 PAK	θ_{JA}=40

+5V

Two MOSFETs in parallel

If output current is high, we recommend two MOSFETs used in parallel instead of one single MOSFET. The following significant advantages are realized using two MOSFETs in parallel:

• **Significant reduction of power dissipation**
Example: RC5055 with maximum output current of 18A at 2.0V with one MOSFET on the high side:

$P_{MOSFET} = (I^2 R_{DS(ON)})*(\text{Duty Cycle}) = (18A)^2 (0.010\Omega)(2.0V / 5V) = 1.296W$

With two MOSFETs in parallel:

$P_{MOSFET} = (I^2 R_{DS(ON)})*(\text{Duty Cycle}) = (18A/2)^2 (0.01\Omega) (2.0V / 5V) = 0.32W/FET$

* **Note:** $R_{DS(ON)}$ increases with temperature. Assume $R_{DS(ON)}$ = 25mΩat 25°C. $R_{DS,ON}$ can easily increase to 50mΩ at high temperature when using a single MOSFET. When using two MOSFETs in parallel, the temperature effects should not cause the $R_{DS(ON)}$ to rise as much.

• **Smaller heat sink required**
With power dissipation down to around one watt, considerably smaller or no heat sink is required.

• **Better Over-Current trip point**
Since RC5055 uses $R_{DS(ON)}$ as the current sense resistor and since power dissipation per MOSFET is much lower, the $R_{DS(ON)}$ will not change much with temperature; the over-current trip point should remain fairly constant with temperature

• **Reliability**
With thermal management under control, this DC-DC converter is able to deliver load currents up to 16A with no performance or reliability concerns.

MOSFET Gate Bias
The MOSFET can be biased by one of two methods: Charge Pump or 12V Gate Bias.

• **Method 1: Charge pump (or Bootstrap) method.**
Figure 4 displays the use of a charge pump to provide gate bias to the high-side MOSFET with the RC5055. Capacitor CP is the charge pump deployed to boost the voltage of the RC5055 output driver. When the MOSFET switches off, the source of the MOSFET is at approximately 0V. CP is charged through the Schottky diode D1 to approximately 4.5V. When the MOSFET turns on, the source of the MOSFET voltage is equal to 5V. The capacitor voltage follows, and hence provides a voltage at BOOT equal to approximately 10V. The Schottky diode D1 is required to provide the charge path when the MOSFET is off, and reverses bias when the BOOT goes to 10V. The charge pump capacitor, CP, needs to be a high Q, high frequency capacitor. A 1µF ceramic capacitor is recommended here.

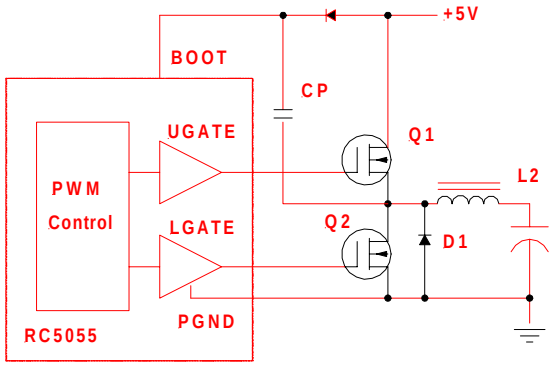

Figure 4. Charge Pump Configuration

• **Method 2: 12V Gate Bias.**
Figure 5 illustrates how a 12V source can be used to bias The BOOT pin. A 47Ω resistor is used to limit the transient current into the BOOT pin in and a 1µF capacitor filter is used to filter the BOOT supply. This method provides a higher gate bias voltage (VGS) to the MOSFET than the charge-pump method does, and therefore reduces the $R_{DS(ON)}$ of the MOSFETs and thus reduces the power loss due to the MOSFET.

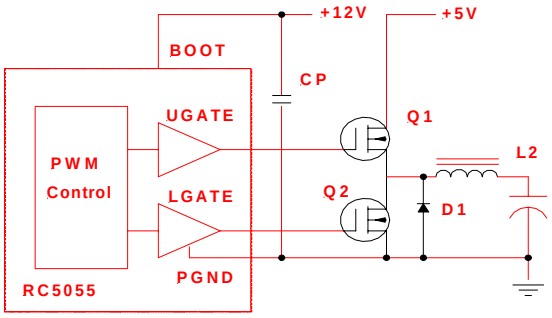

Figure 5. 12V Gate Bias Configuration

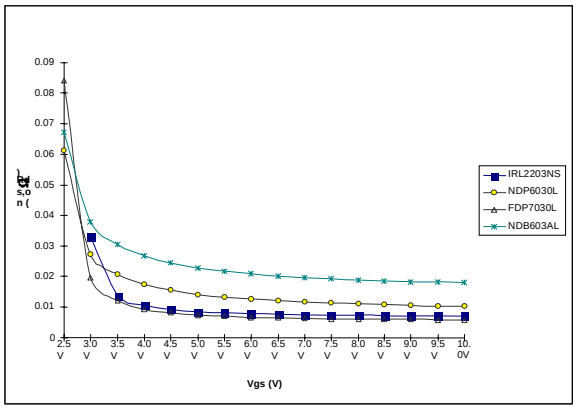

Figure 6. $R_{DS(ON)}$ vs. V_{GS} for Selected MOSFETs

Figure 6 shows how $R_{DS(ON)}$ reduces dramatically with VGS increases.

Converter Efficiency

Losses due to parasitic resistance in the switches, coil, and sense resistor dominate at high load-current level. The major loss mechanisms under heavy loads, in typical order of importance, are:

- MOSFET I^2R losses
- MOSFET Transition losses
- Input Capacitor losses
- Coil losses
- Losses due to the operating supply current of the IC.
- Diode-conduction losses
- Gate-charge losses

Formulae for Calculation of Converter Efficiency

$$\text{Efficiency} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} I_{OUT}}{V_{OUT} I_{OUT} + P_{LOSS}}$$

$$P_{LOSS} = P_{Rds} + (P_{rise} + P_{fall}) + P_{Inductor} + P_{gate} + P_{diode} + P_{caps} + P_{IC}$$

$$P_{Rds} = I_{OUT}^2 R_{ds,on} DC \quad \text{for the high - side MOSFET}$$

$$P_{Rds} = I_{OUT}^2 R_{ds,on} (1 - DC) \quad \text{for the low - side MOSFET}$$

$$P_{rise} + P_{fall} = \frac{V_{IN} I_{OUT} t_{rise} F_s}{2} + \frac{V_{IN} I_{OUT} t_{fall} F_s}{2} \quad \text{for the high - side MOSFET}$$

$$P_{rise} + P_{fall} = \frac{V_f I_{OUT} t_{rise} F_s}{2} + \frac{V_f I_{OUT} t_{fall} F_s}{2} \quad \text{for the low - side MOSFET}$$

$$P_{inductor} = I_{OUT}^2 R_{inductor}$$

$$P_{gate} = CV^2 F_s \quad \text{for each MOSFET}$$

$$P_{diode} = I_{OUT} V_f T_{dt} F_s, \text{ with } T_{dt} \text{ the deadtime}$$

$$P_{caps} = ESR * I_{OUT}^2 * DC * (1 - DC)$$

$$P_{IC} = 25mA * V_{CC}$$

Example Efficiency Calculation

As an example, the efficiency of a synchronous 14A converter based on the RC5055 will be calculated. The converter produces 2.8V output from a 5V input, switches at 300kHz, has MOSFETs with a 4nF gate capacitance, $R_{DS(ON)}$ = 10mΩ for both MOSFETs and a rise and fall time of 50nsec. The inductor has a winding resistance of 3mΩ and the sense resistor used is 5.2mΩ. The schottky paralleled with the synchronous rectifier has a forward voltage of 400mV at 14A. The input capacitors have a total ESR of 15mΩ.

$$P_{Rds} = (18A)^2 10m\Omega = 3.24W$$

$$P_{rise} + P_{fall} = \frac{5V * 18A(50nsec + 50nsec)300kHz}{2} = 1.35W$$

$$P_{rise} + P_{fall} = \frac{400mV * 18A(50nsec + 50nsec)300kHz}{2} = 108mW$$

$$P_{inductor} = (18A)^2 3m\Omega = 972mW$$

$$P_{gate} = 4nF(5V)^2 300kHz * 2 = 60mW$$

$$P_{diode} = 18A * 400mV * 50nsec * 300kHz = 108mW$$

$$P_{caps} = 15m\Omega * (18A)^2 * 0.56 * (1 - 0.56) = 1.20W$$

$$P_{IC} = 25mA * 5V = 125mW$$

$$P_{LOSS} = 3.24W + 1.35W + 0.108W + 0.97W + 0.06W + 0.108W + 1.20W + 0.125W = 7.16W$$

$$\text{Efficiency} = \frac{2.0V * 18A}{2.0V * 18A + 7.16W} = 83\%$$

When using these formulae, special care must be taken regarding the MOSFETs' transition times: the rise and fall refer to the MOSFETs' drain-source voltage, NOT the gate-source. Using the datasheet values (rather than measured values) can also result in serious overestimation of the losses, since the transition is being driven by an inductive source, not a resistor.

Selecting the Inductor

The inductor is one of the most critical components to be selected for a DC-DC converter application. The critical parameters of the inductor are its inductance (L), maximum DC current (I_O), and DC coil resistance (R_l).

The inductor's inductance helps determine two key parameters of a converter, its ripple current and its transient response. On the one hand, making the inductance large reduces the ripple current, and thus the output ripples voltage. On the other hand, a large inductance provides a slow response to load transients. For Pentium II supplies, the transient response is paramount, and thus the inductance is typically chosen to be in the 1-5µH range.

Most inductors' inductance also depends on current, that is, increasing the current through the inductor decreases the inductance. It is thus vital to specify the DC current when procuring an inductor. The one type of inductor, which does not change inductance with current, is the rod-core inductor, but this type may have significant EMI (noise) problems. For further information, refer to Applications Bulletin AB-12.

The resistance of the winding of the inductor is also important, as it is directly responsible for much of the losses in the inductor. Minimizing the resistance will help improve the converter's efficiency.

Implementing Over-current Protection

Intel currently requires all power supply manufacturers to provide continuous protection against short circuit conditions that may damage the CPU. To address this requirement, Fairchild Semiconductor has implemented a current sense methodology to limit the power delivered to the load in the event of over-current. The voltage drop created by the output current across the upper switching MOSFET is compared to the voltage drop across the over-current programming resistor R_{OCSET}. When calculating R_{OCSET}, pay careful attention to the output limitations during normal operation and during a fault condition. If the over-current protection threshold is set too low, the DC-DC converter may not be able to continuously deliver the maximum CPU load current. If the threshold level is too high, the output driver may not be disabled at a safe limit and the resulting power dissipation within the MOSFETs may rise to destructive levels. The following is the design equation used to determine the over-current threshold limit:

$$I_{pk} = I_{load,max} + \frac{I_{ripple}}{2}$$

Where I_{pk} is defined as in Figure 7, and $I_{load,\ max}$ = maximum output load current. Figure 7 illustrates the inductor current waveform for the RC5055 DC-DC converter at maximum load.

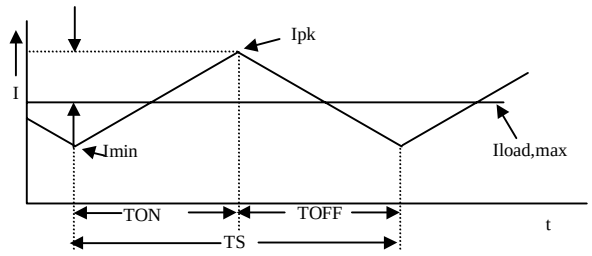

Figure 7. Typical DC-DC Converter Inductor Current Waveform

The calculation of the ripple current is as follows:

$$\frac{I_{ripple}}{2} = \frac{V_{IN} - V_{OUT}}{2L} T_S \frac{V_{OUT}}{V_{IN}}$$

where:

V_{IN} = input voltage to converter,

T_S = the switching period of the converter = $1/f_S$, and

f_s = switching frequency.

As an example, for an input voltage of 5V, output voltage of 2.8V @ 14A, L equal to 1.3µH and a switching frequency of 285KHz (using CEXT = 100pF), the peak inductor current can be calculated as :

$$I_{pk} = 14A + \frac{5V - 2.8V}{2 * 1.3\mu H} \frac{1}{285kHz} \frac{2.8V}{5V} = 15.7A$$

Therefore, the over-current detection threshold must be at least 16A. The next step is to determine the value of the over current programming resistor. The R_{OCSET} resistor value can be determined as

$$I_{Peak} := \frac{I_{OCS} \cdot R_{OCSET}}{R_{DS(ON)}}$$

RC5055 Over-current Characteristics

The over-current function protects the converter from a shorted output by using the upper MOSFET's on-resistance, RDS(ON) to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor. The over-current function cycles the soft-start function in a hiccup mode to provide fault protection.

A resistor (ROCSET) programs the over-current trip level. An internal 200mA current sink develops a voltage across ROCSET that is referenced to VIN. When the voltage across the upper MOSFET (also referenced to VIN) exceeds the voltage across ROCSET, the over-current function initiates a soft-start sequence. The soft-start function discharges CSS with a 10mA current sink and inhibits PWM operation. The soft-start function recharges

CSS, and PWM operation resumes with the error amplifier clamped to the SS voltage. Should an overload occur while recharging CSS, the soft start function inhibits PWM operation while fully charging CSS to 4V to complete its cycle. Note that the inductor current increases to over 15A during the CSS charging interval and causes an over-current trip. The converter dissipates very little power with this method. For an equation for the ripple current see the section under component guidelines titled 'Output Inductor Selection.' A small ceramic capacitor should be placed in parallel with ROCSET to smooth the voltage across ROCSET in the presence of switching noise on the input voltage.

Power dissipation in the low-side MOSFET during an over-current condition must also be considered. The low-side MOSFET dissipates power while the high-side MOSFET is off. The power dissipated in the low-side MOSFET during normal operation, is given by:

$$P_D = I^2 * R_{DS(ON)} * (1 - DC)$$

$$= (14.2)^2 * .01 * .36 = 0.73W$$

During an over-current , the duty cycle reduces to around 47%. The power dissipated in the low-side MOSFET during short circuit condition, is given by:

$$P_D = (20)^2 * .01 * .53 = 2.1W$$

Thus, for the low-side MOSFET, the thermal dissipation during over-current is greatly magnified. This requires that the thermal dissipation of the low-side MOSFET be properly managed by an appropriate heat sink. To protect the low-side MOSFET from being destroyed in the event of an over-current, you should limit the junction temperature to less than 130°C. You can find the required thermal resistance using the equation for maximum junction temperature:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\Theta JA}}$$

Assuming that the ambient temperature is 50°C,

$$R_{\Theta JA} = \frac{T_{J(max)} - T_A}{P_D} = \frac{130 - 50}{2.1} = 38^\circ C/W$$

Thus, you need to provide a heat sink that gives the low-side MOSFET a thermal resistance of 38°C/W or lower to protect the device during an indefinite short.

In summary, with proper heat sink, the low-side MOSFET is not over-stressed during an over-current condition.

Schottky Diode Selection

The application circuit diagram of Figure 3 shows a Schottky diode, D1. D1 is used as a flyback diode to provide a current path for the inductor current during the dead-time when both the high-side and low-side MOSFETs are briefly both turned off. Table 11 shows the characteristics of several Schottky diodes. Note that MBRB2515L has a very low forward voltage drop even at high current. Although it is not necessary to use a high-current diode for this application, selecting a higher current schottky will provide improved efficiency at slightly higher cost.

Table 4. Schottky Diode Selection Table

Manufacturer Model #	Conditions	Forward Voltage VF
Motorola 1N5817	I_F = 1A; T_j = 25°C	<.45v
Motorola 1N5820	I_F = 3A; T_j = 25°C	<.475v
Motorola MBR2015CTL	I_F = 20A; T_j = 25°C I_F = 20A;T_j =150°C	< 0.58v < 0.48v
Motorola MBRB2515L	I_F = 19A; T_j = 70°C	< 0.28v

Output Filter Capacitors

Correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and, most importantly, load transient response. Because the control loop response of the controller is not instantaneous, the initial load transient must be supplied entirely by the output capacitors. The initial voltage deviation is determined by the total ESR of the capacitors used and the parasitic resistance of the output traces. For a detailed analysis of capacitor requirements in a high-end microprocessor system, please refer to Application Bulletin 14.

Input Filter

The DC-DC converter may include an input inductor between the system +5V supply and the converter input as described below. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is typical; details on selection of an input inductor may be found in Applications Bulletin AB-16.

The number of input capacitors required for a converter is determined by the capacitors' ripple current rating. The ripple current is given by:

$$I_{rms} = I_{out} \sqrt{DC - DC^2}$$

Thus, for example, a Deschutes processor running at 2.0V out from 5.0V in has a DC = 2.0/5.0 = .4; if it pulls 14.2A, its I_{rms} = 7A.

Table 5 shows some typical input capacitors' current ratings the current rating increases as temperature decreases. Although exceeding these ratings will not cause capacitor damage, it will reduce their life, and thus the converter's MTBF.

Manufacturer	Part #	I_{rms}
Sanyo	10MV1200GX	2.0A @ 65°C
United Chemicon	LXZ10VB122M10X20	1.2A @ 105°C
Panasonic	EEUFA10122	1.2A @ 105°C

Table 5. Input Capacitor Selection Guide

General

The RC5055 has two Low Dropout Linear Regulators (LDO). One is optimized for GTL+ VTT termination applications and the other is a fixed 2.5V optimized for the clock supply application. The fixed 2.5V LDO is short-circuit protected with foldback. The RC5055 provides fast transient response. The output filter capacitors with low ESR is a part of the frequency compensation circuit.

Stability

The LDO's in RC5055 require output capacitors as a part of the frequency compensation. It is recommended to use a 22µF solid tantalum or a 100µF aluminum electrolytic on the output to ensure stability. The frequency compensation of this device optimizes the frequency response with low ESR capacitors. In general, it is suggested to use capacitors with an ESR of <0.1Ω.

Load Regulation

It is not possible to provide true remote load sensing because the LDO's in RC5055 are three-terminal devices. The load regulation is limited by the resistance of the wire connecting the regulator to the load. Load regulation per the data sheet specification is measured at the package.

Thermal Considerations

The RC5055 does not have over-temperature protection under overload conditions. However, for normal continuous load conditions, do not exceed maximum junction temperature ratings. The electrical characteristics section provides a separate thermal resistance and maximum junction temperature for controller.

PCB Layout Guidelines

Refer Appendix 1 regarding guidelines for component selection and layout using the RC5055 DC-DC controller

Appendix 1: **Layout Guidelines**:

1. Placement of the MOSFETs relative to the RC5055 is critical. The MOSFETs (Q1 & Q2) should be placed such that the trace length of the UGATE & LGATE (pins 18 and 21) from the RC5055 to the MOSFET gates is minimized. A long lead length on this pin will cause high amounts of ringing due to the inductance of the trace combined with the large gate capacitance of the MOSFET. This noise will radiate all over the board, and because it is switching at such a high voltage and frequency, it will be very difficult to suppress.

   The following drawing depicts an example of good placement for the MOSFETs in relation to the RC5055 and also an example of problematic placement for the MOSFETs:

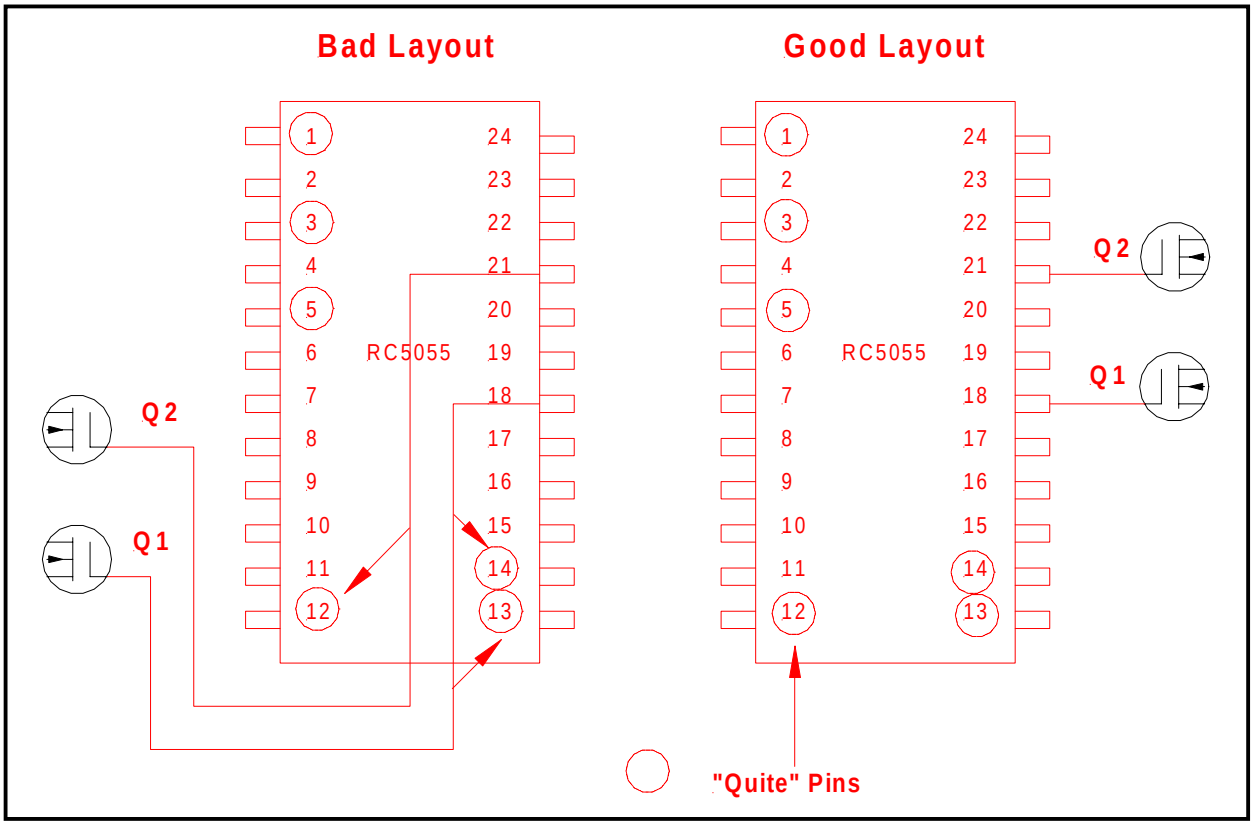

Fig. 1 Layout Consideration

In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5055. That is to say, traces that connects to pins 17, 18, 19 and 21(PHASE, UGATE, BOOT AND LGATE) should be kept far away from the traces that connect to pins 5, 12, and pin 14.

2. Place decoupling capacitors (.1uF) as close to the RC5055 pins as possible. Extra lead length on these will negate their ability to suppress noise.

3. Each VCC and GND pin should have its own via down to the appropriate plane underneath. This will help give isolation between pins.

3. Place MOSFETs, inductor and Schottky as close together as possible for the same reasons as #1 above. Also place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a 1uF decoupling cap right on the drain of each MOSFET will help to suppress some of the high frequency switching noise on the input of the DC-DC converter.

4. A 1µF capacitor is physically as close as possible to the V_{CC} (pin 20). This ensures that the +12V power running the IC is noise-free.
5. A 1µF capacitor is physically as close as possible to the BOOT (pin 19) This capacitor together with R2 provide bypass for the high currents used in driving the MOSFETs.
6. A 1µF capacitor is physically close to the drain pin of the high-side MOSFET. This reduces the impedance presented by the input bulk capacitance at high switching speeds.
7. The input bulk capacitance is physically located less than 1" from the drain of the power MOSFET(s). This reduces the impedance presented to the high-side MOSFET.
8. The output bulk capacitors are located physically as close to the CPU socket as possible. This minimizes the impedance seen by the CPU, optimizing transient performance.
9. The controller IC and the power FET are oriented in such a way as to make the length of the gate drive trace < 1". This minimizes trace inductance, reducing gate ringing. If the trace is > 1", a 4.7Ω resistor must be used in series from the controller to the gate, one resistor for each MOSFET.
10. The gate drive trace is routed on one layer only. This prevents gate noise from propagating to other layers.
11. The gate drive trace routing stays away from the quiet analog sections of the RC5055 controller IC. (I.e., away from FB1, FB and COMP). This prevents switching noise from upsetting the analog functions of the controller.
12. Each V_{CC} pin on the IC is connected to the 5V power plane through its own via. This helps prevent crosstalk.
13. The controller IC receives its V_{CC} power from the system side of the input inductor and not the "noisy" side of the inductor (i.e., V_{CC} is NOT connected to the side that is connected to the power MOSFET drains). This keeps the switching noise from upsetting the analog functions of the controller.
14. High currents are located on planes, not traces. This minimizes losses.
15. An internal power plane connects the source of the high-side MOSFET, the inductor, and the flyback schottky diode and the drain of the low-side MOSFET together. This minimizes losses.
16. All of the signal ground connections are attached together, and connect to the power ground plane at only one place, preferably the input capacitor ground. Separating signal and power ground avoids noise pickup into the analog functions of the controller.
17. The controller IC has a continuous ground plane running underneath the entire chip area. This helps minimize noise pickup into the analog functions of the controller.
18. Each of the IC's power ground pins has a separate via connection down into the ground plane. This minimizes ground bounce.
19. Ground connections are short, and go directly to the ground plane. This minimizes ground bounce.
20. Sensitive low-level signals are away from the active switching components. They use the ground plane as a shield. This helps minimize noise pickup into the analog functions of the controller. These signals are FB, FB1, Comp, Vsen and SS
21. Connect a 0.1uF across the electrolytic filter capacitor of each of the LDO regulators for high frequency noise suppression
22. As much as practically possible the two LDO regulators are located physically away from the PWM supply.
23. As much as practically possible the two LDO do not share common traces with each other or the PWM supply except in the ground plane
24. Try as much as possible to run the noisy switching signals (PHASE, UGATE, BOOT AND LGATE) on one layer; and use the inner layers for only power and ground. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VSEN