A Universal 100kHz Power Supply Using a Single HEXFET®

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Summary

Power MOSFETs are attractive candidates for use in switching power supplies. In order to take full advantage of their unique characteristics, one cannot simply substitute a MOSFET for a bipolar transistor in an existing circuit. More fundamentally, it is necessary to rethink basic concepts, and to shape the circuit around the operating features of the device.

This application note describes a 100kHz, 100W off-line power supply providing a regulated 5V DC output. The circuit is "universal" in the sense that it operates both from 115V and 240V line inputs, without any alteration of circuitry or switching of components. The circuit uses a single 500V-rated power HEXFET in a modification of the classical "forward converter" circuit.

Introduction

DC power supplies are employed today wherever electrical or electronic equipment is in use. Traditional designs that operate from AC input power are based upon the use of a line frequency transformer, a secondary rectifier, an output filter and a dissipative series regulating element; typical overall efficiency is 40% to 50%.

Newer designs are based upon fundamentally more efficient high frequency switching techniques. The line frequency is first rectified to DC, then inverted to high frequency AC, by a transistor switching circuit. The high frequency voltage is fed through an output transformer, rectified and filtered to produce the required DC. Regulation of the output is accomplished by controlling the pulse width of the high frequency voltage wave. This circuit technique gives much better efficiency — typically 75% to 85% — and a dramatic reduction in size — typically 4 or 5 to 1 — because of the much smaller magnetic and filter components associated with the use of high frequency.

Today, most switching power supplies use power bipolar transistors. Switching frequencies are in the range of 20kHz to 40kHz. Although a few designs operate at higher frequency, this undoubtedly means "pushing" the bipolar to the limits of its performance.

Higher operating frequency than the usual 20kHz to 40kHz range is in principle advantageous, because it offers the possibility for further reductions in size of magnetic and filter components, as well as faster response. With the availability of power MOSFETs, the switching component is no longer the frequency limiting element in the system. This new situation has generated considerable interest in where the optimum switching frequency of a power supply now lies, having due regard to the technology of the associated magnetic and filter components. Presently, there is no clear consensus. It is safe to say, however, that the optimum switching frequency is certainly greater than the 20kHz to 40kHz range of the bipolar transistor. Most probably it is 100kHz, and perhaps considerably higher.

It would be erroneous, however, to assume that the potential advantage of the power MOSFET is simply one of faster switching speed and higher frequency. In order to utilize all of the characteristics of the power MOSFET to best advantage, the design task is not simply one of pursuing well trodden bipolar transistor circuit techniques, albeit with higher operating frequency. Basic circuit concepts should be rethought; only then can all the potential advantages of the MOSFET be realized.

By the same token, it can be quite erroneous to labor under the notion that because power MOSFETs still are more expensive than bipolars, therefore they are not yet economically competitive. This overlooks the fact that performance advantages, or cost reductions, or both, are achieveable at the system level with these devices, that can more than compensate for their higher costs.

In this application note, we present a switching power supply using a HEXFET that operates at 100kHz — a considerably higher frequency than normally used with bipolar transistors. Attainment of this frequency actually is no particular feat for a power HEXFET, since frequencies much higher are within easy reach. A more vital objective of this application note is to demonstrate that by rethinking basic circuit concepts, results are achievable which, to many circuit designers at first sight, might seem to be unattainable. Specifically, we will show that just a single 500V-rated HEXFET can be used in a circuit that operates from a 220V line input; this compares with the usual 800V minimum rating requirement of a bipolar transistor in a single-ended circuit. We will moreover demonstrate a circuit which has the surprising capability of maintaining a constant DC output voltage over a very wide range of line input voltage — a "universal" power supply — that can operate both from the 115V line

common in the United States, and from a 220V/240V line common in Europe, without any modification of circuitry or switching of components.

Specific Design Goals

The discussion that follows is addressed to the general circuit concepts involved in using a single power HEXFET in a wide input voltage range switching power supply. A specific implementation of the concepts described is presented; this is a circuit for a 100kHz, 100W, 5V DC power supply that employs a single 500V/3.5A-rated power HEXFET in a TO-220 package.

The stated purpose of this application note is not to supply a "worked-out design" but to provide some basic guidelines on how to rethink a power supply along MOSFET lines. Because of this we will overlook several subjects that are of vital importance in the design of a power supply like the bias supply, EMI and stability considerations and isolation requirements. Although the design has been tested at 265V input, as the oscillograms show, it is questionable whether the voltage margin on the device is adequate for operation under those conditions, particularly if the dynamic performance of the supply is underdamped.

The performance of this power supply is summarized in Table 1. Variations from these specifications — different output power, different output voltage, different operating frequency, and so on — are obviously possible, without departing from the basic concepts.

Table 1. Performance Characteristics of 100kHz "Universal" Power Supply

Minimum Input Voltage	85V RMS, 50-400 Hz
Maximum Input Voltage	230V RMS, 50-400 Hz
Output Voltage	5V DC
Maximum Output Current	20A DC
DC Output Voltage Regulation, For All Conditions of Output Current & Input Voltage	± 0.5%
Maximum Output Ripple Voltage	50mV P-P
Transient Response for a Step Change of 10A Load Current	500mV, settling within 250μs
Full Load Efficiency	74%

Basic Concepts

The Conventional Forward Converter Circuit

The basic single-transistor forward converter circuit is shown in Figure 1. Idealized voltage and current waveforms that describe the operation are shown in Figure 2. During the conduction period of the transistor, current is transferred from the primary DC power source through the output transformer to the output circuit. During the OFF period of the transistor, the magnetizing current in the transformer is returned via the clamping winding to the primary DC source, resetting the flux in the transformer core, prior to the next cycle of operation.

The clamping winding usually has the same number of turns as the primary, which means that the peak voltage developed across the transistor during the OFF period is twice the primary DC supply voltage. For a nominal line input voltage of say 220V, this peak voltage would be about 660V; this is why a transistor voltage rating of at least 800V is required.

The maximum permissible conduction period of the transistor is 50% of the total cycle time. It cannot be longer than this, because there would then be insufficient time for the transformer flux to be reset during the transistor OFF period, and the transformer would be driven into saturation. A 50% duty cycle is approached for the condition of low input voltage and full load; the transistor conduction time automatically decreases from this point as the line input voltage increases or as the output load decreases, under the action of a

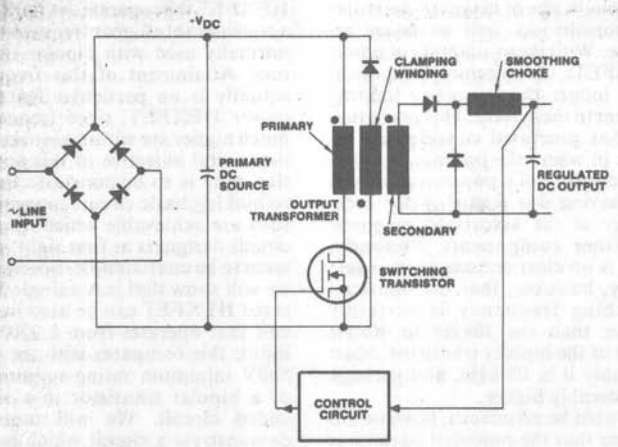


Figure 1. Basic Single-Transistor Forward Converter Circuit

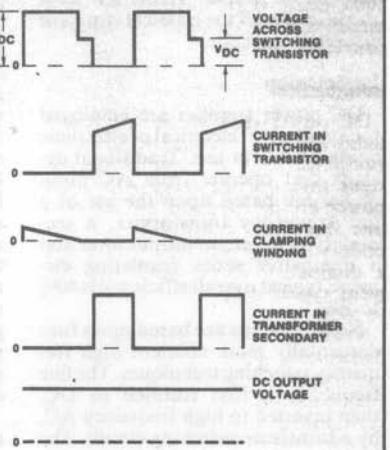


Figure 2. Idealized Waveforms for the Circuit of Figure 1

closed-loop regulator circuit, which acts so as to maintain an essentially constant output voltage.

Modified Circuit

There is no fundamental need to clamp the peak transistor voltage to twice the supply voltage. The device voltage could be clamped to any level that is higher than the DC supply voltage, so long as the voltage-time integral developed across the transformer during the OFF period of the transistor is equal and opposite to the voltage-time integral during the conduction period, thereby fully resetting the flux by the end of each cycle.

It is therefore possible, in principle, to reduce the peak transistor voltage, at the expense of reducing the conduction time of the transistor. The penalty is that the peak device current necessarily increases as the conduction time decreases, for a given power output and input voltage level. The idealized waveforms in Figure 3(a) illustrate operation with a 20% duty cycle; for comparison, Figure 3(b) represents operation with a 50% duty cycle, for the same power output and input voltage. The peak transistor current is greater by a factor of 2.5 for the shorter conduction period; the peak transistor voltage, on the other hand, is lower, by a factor of 1.6. This means that for a 240V input, the peak transistor voltage is reduced from the usual 720V to around 450V, permitting a 500V-rated HEXFET to be used, albeit with limited margin.

With a bipolar transistor, operation with a duty cycle substantially less than 50% is undesirable. The gain of a bipolar decreases, and the device becomes increasingly difficult to use as the peak current increases. The transconductance of the power HEXFET, on the other hand, does not decrease with increasing drain current, and it is quite practical to operate a HEXFET with a short duty cycle at relatively high peak current. Higher peak current will, of course, produce greater conduction power dissipation than would be obtained in a circuit operating with a longer conduction time at correspondingly lower current. This is of little concern, however, because the HEXFET is well able to handle the "extra" dissipation; in any event, the dissipation in the switching device is substantially less than that in the output rectifiers. It is an unfortunate fact that the conduction voltage drop in these rectifiers is quite significant for a 5V output, and the circuit losses tend to be dominated by the rectifier losses.

Clamping the Drain Voltage

The drain voltage must be clamped at a level that ensures the output transformer is completely reset during the OFF period of the HEXFET. There are various ways of doing this.

A clamping winding on the output transformer — used in the conventional forward converter with a 50% duty cycle — can, in principle, still be used. The ratio of clamping turns to primary turns would, of course, no longer be 1 to 1. Taking the example considered, for a conduction duty cycle of 0.2, the peak transistor voltage must be at least 1.25X the primary DC source voltage. The clamping winding should therefore have four times the number of primary turns, as shown in Figure 4(a).

This fixes the peak transistor voltage at 1.25X the primary DC source voltage, as illustrated in Figure 4(b). A duty cycle of 0.2 would be set to occur when the line input voltage is lowest, and the output load current is highest. As the line input voltage increases, or the load current decreases, the conduction time of the transistor would decrease, under the action of a closed-loop regulator, so as to keep the DC output voltage at a constant value. The transistor clamping voltage would always be 1.25X the primary DC source voltage, regardless of what that voltage might be. The flux in the transformer is therefore reset before the end of the cycle, except at the condition of minimum line input voltage, and the peak transistor voltage is therefore generally higher than the level that is just sufficient to reset the transformer by the end of the cycle.

A transformer clamping winding, though realizable, creates some practical problems. In the example considered, the peak voltage developed between the primary and clamping windings would be five times the DC

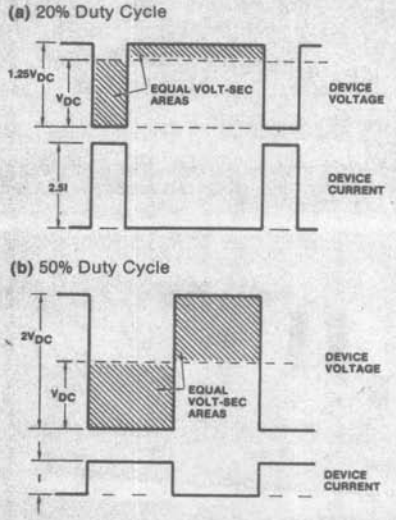


Figure 3. Idealized Waveforms of Device Voltage and Current

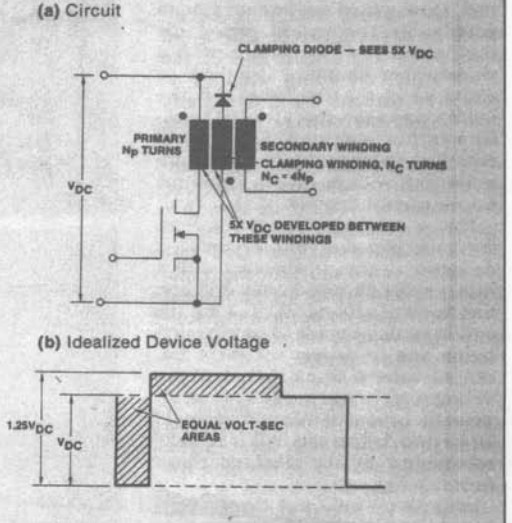


Figure 4. Use of a Transformer Clamping Winding

source voltage; the insulation between these windings must be sufficient to withstand this voltage. The clamping rectifier also sees a total of five times the DC source voltage and must be rated accordingly. Perhaps the biggest practical difficulty is that substantial leakage inductance and self-capacitance inevitably appears between the primary and clamping windings, and this gives rise to superimposed high frequency oscillations on the current and voltage waves, as shown in Figure 4(c). These oscillations are difficult to eliminate.

A Different Approach

A much more satisfactory approach arises from the basic fact that for minimum voltage stress on the HEXFET, the voltage that appears across the transformer during the device OFF period should have the right amplitude to reset the flux just by the end of this period, independent of the conduction duty cycle. This principle is illustrated by the idealized waveforms in Figure 5. In this example, it is assumed that the minimum duty cycle, which occurs at maximum input voltage, is 0.15.

If this principle is followed, the voltage that appears across the transformer during the reset period by no means bears a fixed relationship to the primary DC source voltage; it increases as the DC source voltage decreases and is inversely proportional to (1-D), where D is the duty cycle. Thus, a transformer clamping winding, in principle, will not do the job.

If the required clamping circuit could be devised, two benefits — in addition to the elimination of the transformer clamping winding — would be realized. First, as already mentioned, the voltage across the HEXFET would be minimized. Second, there would not be a maximum permissible conduction period for the transistor — as there is with a transformer clamping winding — above which the transistor OFF period becomes too short for the transformer flux to be reset. There would therefore no longer be the same minimum line voltage below which the circuit cannot operate.

This is very interesting; it means, for example, that if the circuit is designed so that it operates with a rather short duty cycle, say 0.15 at a line voltage around 265V, then the circuit could be made to stay in regulation and to deliver the same DC output voltage when the line input voltage is as low as say 80V, at which point the conduction duty cycle would be about 0.5. This example is actually represented by the idealized waveforms in Figure 5.

Even this would not theoretically be the limiting range of operation; as a practical matter, however, most integrated circuits that are intended for controlling power supplies of this type have a maximum duty cycle of 0.5. At all events, if we design the circuit according to these principles, we will have a "universal" power supply, capable of delivering the same regulated DC output voltage both from 115V and 220V/240V line inputs, with no modification of circuitry, or switching of components.

A Capacitor-Resistor-Diode Clamp

The desired clamping circuit can be realized in a surprisingly simple manner. The circuit is illustrated in Figure 6. The capacitor C is a "reservoir" capacitor which charges to an essentially steady level of voltage — the necessary transformer resetting voltage. The resistor R dissipates the energy delivered to the clamping circuit from the transformer. Unlike the transformer winding, which returns

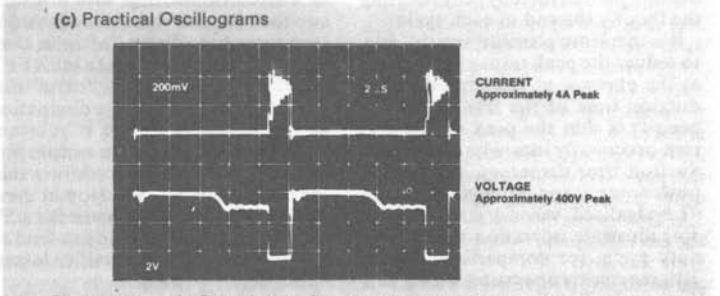


Figure 4. Use of a Transformer Clamping Winding (continued)

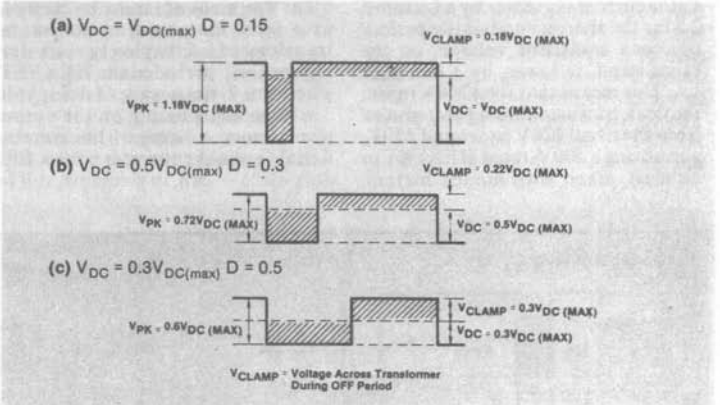


Figure 5. Idealized Waveforms Illustrating Operation when Device Voltage During OFF Period Always has just Correct Amplitude to Reset Transformer by End of this Period.

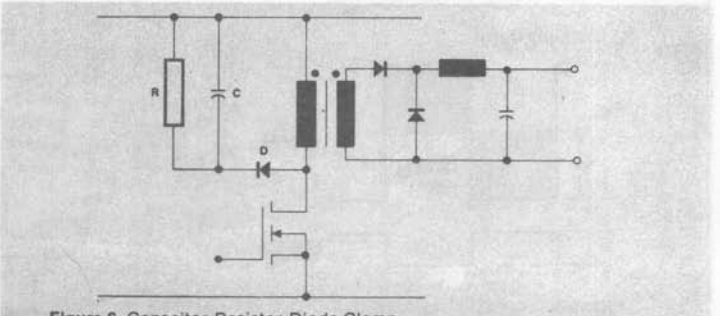


Figure 6. Capacitor-Resistor-Diode Clamp

the energy stored in the transformer to the primary DC source, this is a dissipative clamp.

From a practical point of view, because of the possibility for operating at high frequency, the transformer can be designed so that the power dissipation in the clamp is kept to a quite acceptable level. In the specific circuit described, the power dissipation in the clamping circuit is quite minimal, and ranges between 2% and 3% of the output power.

The inherent action of this simple clamp can be arranged to be such as to adjust the steady-state voltage across the capacitor to the level required to reset the transformer just by the end of the OFF period, regardless of the level of input voltage. This can be seen by assuming for the moment that the voltage across the capacitor is insufficient to reset the transformer. In this event, the magnetizing current, and the voltage across the capacitor, "ratchet up" during succeeding cycles, until the voltage does become sufficient, at which point an equilibrium condition is attained. This action is illustrated by the idealized waveforms in Figure 7.

This clamp thus provides the required voltage to keep the transformer voltage-time integral within balance, independent (within limits) of the value of the capacitor C or the resistor R. Care must be taken, however, to size the resistor so that minimum energy is stored in the transformer — that is, so that the magnetizing current does not "ratchet up" more than is necessary — otherwise, the losses will be excessive. Assuming that the magnetizing current will always be continuous, and thus that the HEXFET voltage will always be minimized, the "best" design will result from sizing the resistor so that the magnetizing current is just continuous at the highest input voltage level.

The general relationship between the voltage across the clamping resistor, V_R, and the primary DC source voltage, V_{DC}, for a given conduction duty cycle, D, with continuous transformer magnetizing current is:

$$V_R = \frac{D\,V_{DC}}{(1-D)}$$

The required value of the resistor R is therefore given by:

$$R = \frac{\left[\frac{D_{(min)}\,V_{DC(max)}}{1-D_{(min)}}\right]^2}{\left[\tfrac{1}{2}\,L_{(mag)}\,I^2_{(mag)PK} + \tfrac{1}{2}\,L_S\,I^2_{LPK}\right] f}$$

Where $D_{(min)}$ is the minimum full load duty cycle, (obtained when $V_{DC} = V_{DC(max)}$).

$L_{(mag)}$ is the transformer magnetizing inductance.

$I_{(mag)PK}$ is the peak magnetizing current for just-continuous magnetizing current.

L_S is the leakage inductance of the transformer, referred to the primary.

I_{LPK} is the peak full load current in the transformer primary.

f is the frequency.

The ratio of the voltage V_R across R at any other lower value of primary DC voltage V_{DC} is:

$$\frac{V_R}{V_{R(min)}} = \frac{1 - D_{(min)}}{1-\left[\frac{V_{DC(max)}}{V_{DC}} \cdot D_{(min)}\right]}$$

Considering a specific example, if $D_{(min)} = 0.15$ and $\frac{V_{DC(max)}}{V_{DC}} = 0.3$, then:

$$\frac{V_R}{V_{R(min)}} = \frac{1 - 0.15}{1 - [(0.15)3]} = 1.55$$

The losses in the clamping resistor at 1/3 of the maximum input voltage would then be $1.55^2 = 2.4X$ the losses at maximum input voltage.

The maximum power dissipation in the clamp — obtained at the lowest input voltage — can be reduced, at the expense of a small increase in the maximum voltage developed across the HEXFET — obtained at the highest input voltage — by sizing the resistor R so that the magnetizing current becomes discontinuous at some intermediate value of line input voltage. As the input voltage increases above this level, the peak magnetizing current stays constant, while the magnetizing current waveform becomes progressively more discontinuous, and the voltage across the clamp circuit stays constant, because (for a given load current) the energy stored in the transformer is constant. Below the critical intermediate level of line voltage, the transformer magnetizing current becomes continuous, and the clamping voltage rises as the input voltage decreases.

As an example of this design approach, assume that the clamp resistor is sized to give just-continuous conduction at 45% of maximum line voltage. If the minimum duty cycle at maximum input voltage is 0.15, then at maximum input voltage, the peak voltage developed across the transistor will be 1.23, instead of 1.18 times the primary DC source voltage. For a total range of input voltage variation of 3 to 1, the maximum duty cycle would be 0.45, and the ratio of the maximum to minimum voltage across

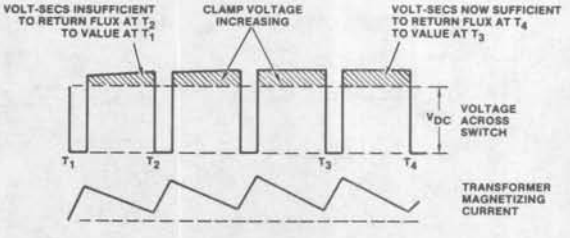


Figure 7. Idealized Waveforms Showing Transformer Magnetizing Current "Ratcheting Up" to Create Sufficient Clamp Voltage to Maintain Equilibrium

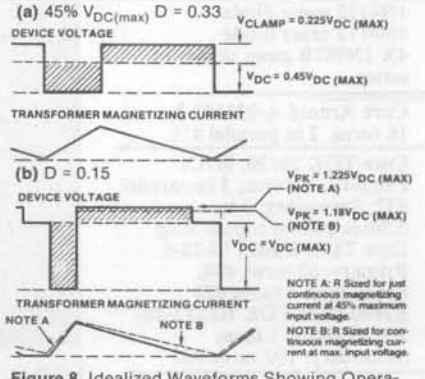


Figure 8. Idealized Waveforms Showing Operation when Clamp Resistor is Sized to Give just Continuous Magnetizing Current at 45% Maximum Input Voltage

the clamp resistor would be:

$$\frac{V_{R(max)}}{V_{R(min)}} = \frac{1 - (0.15/0.45)}{1 - 0.45} = 1.22$$

The range of maximum to minimum power loss in the clamp resistor at full output power would then be $1.22^2 = 1.49$. Figure 8 illustrates this specific design example.

Practical Circuit

Figure 9 shows a complete diagram for a 100W, 100kHz, 5V DC output circuit, which conforms with the performance specifications shown in Table 1. Component details are listed in Table 2.

Table 2. List of Components for Figure 9

Q1	IRF830 HEXFET
IC	Silicon General 3526
B1	IR KBPC 106
C1	500μF, 450V wkg.
C2	0.68μF, 100V
C3	4X 150μF, 6V
C4	22μF, 16V
C5	0.5μF, 25V wkg.
C6	10nF
C7	910pF
C8	0.0068 mfd.
C9	0.005μF
C10	0.1μF
C11	22μF, 25V
R1	1.5K (3X500Ω, 5W)
R2	12Ω 1/4W
R3	6.8kΩ 1/4W
R4	10Ω
R5	12kΩ 1/4W
R6	100Ω potentiometer
R7	33Ω 1/4W
R8	560Ω 1/4W
D1	20FQ030
D2	BYV 79-100
D3	IR 40SL6
Z1	1N4112 zener diode
Z2	1N4112 zener diode
Z3	4X 1N987B zener diodes in series
L1	Core Arnold A-930157-2, 16 turns, 2 in parallel #14
T1	Core TDK 26/20, H7C1 Primary: 20 turns, 3 in parallel #32; Secondary: 3 turns, 0.3mm x 8mm copper strip
T2	Core TDK H5B2T10-20-5, Primary: 60 turns #24; Secondary: 6 turns #24
T3	E2480 Core TDK H52T5-10-2.5. Primary: 1 turn; Secondary: 100 turns #32

Performance Measurements

Oscillograms for various operating conditions are shown in Figures 10 through 20. Figure 10(a) and (b) shows oscillograms of drain voltage and drain current for output currents of 20A and 5A, respectively, with a 85V input. Figure 11(a) and (b) shows corresponding waveforms with 265V input.

It will be noticed that at this input voltage the drain voltage is dangerously close to the max. rated value. When the output voltage is switched, low frequency damped oscillation occur across the input filter capacitors. The voltage rating of the device can be easily exceeded during these oscillations.

Figure 12(a) and (b) shows oscillograms of HEXFET voltage and current during turn-ON for output currents of 20A and 5A, respectively, with 85V input. Note that although the voltage across the HEXFET falls in about 75ns, the rise time of the HEXFET current with a 20A output is over 300ns. This rather long rise time is due to leakage inductance, primarily of the transformer, and does not reflect the switching speed of the HEXFET. Figure 13(a) and (b) shows corresponding oscillograms for the turn-on interval, with 265V input. The rise time of the current is faster, because the higher voltage produces an increased rate-of-rise of current in the circuit inductance.

Figure 14(a) and (b) shows oscillograms of HEXFET voltage and current during turn-OFF for output currents of 20A and 5A, respectively, with 85V input. Transformer leakage inductance does not significantly effect the fall time of the current, because the current in the leakage inductance when switching OFF is diverted into the clamping circuit, and the slow fall time is not "seen" by

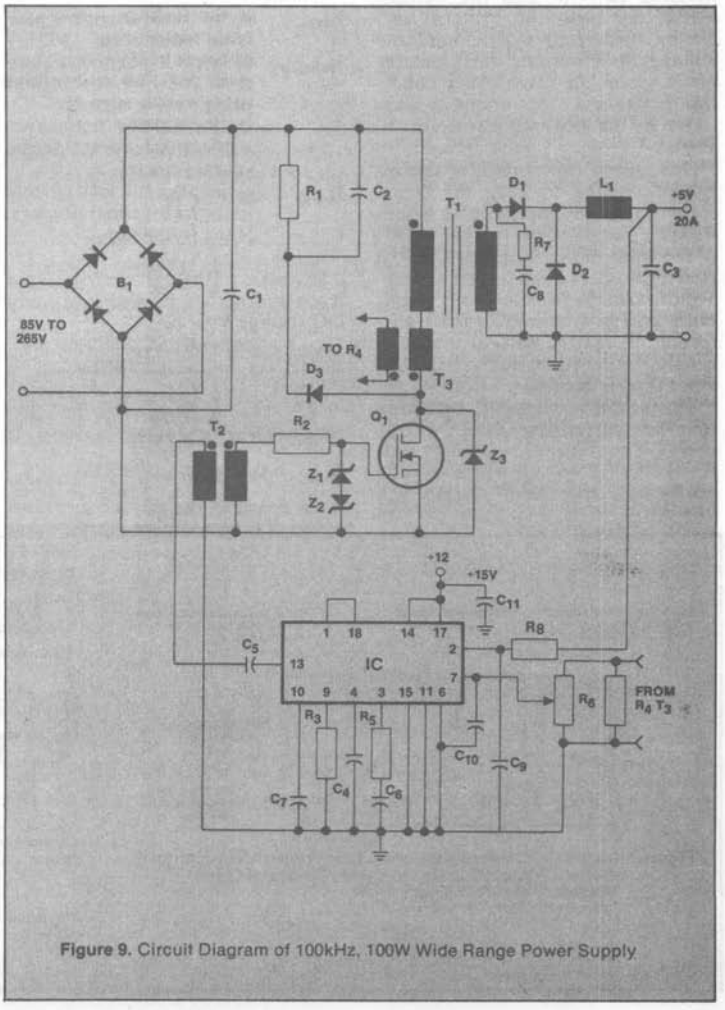
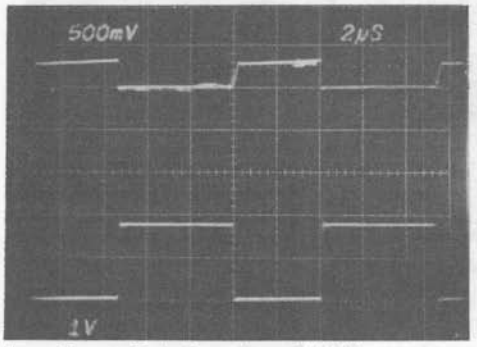
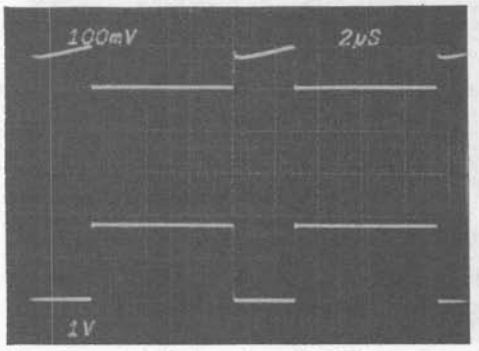


Figure 9. Circuit Diagram of 100kHz, 100W Wide Range Power Supply



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

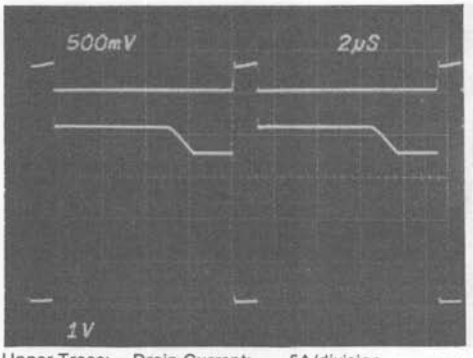
(a)



Upper Trace: Drain Current: 1A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

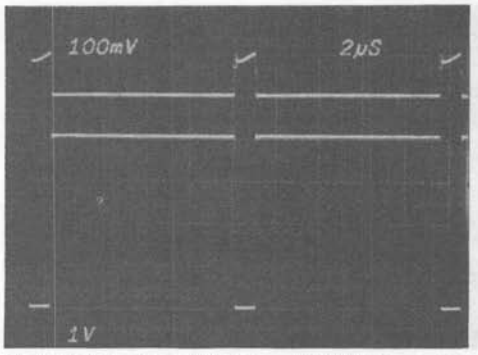
(b)

Figure 10. Oscillograms of Drain Voltage and Current, 85V Line Input



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

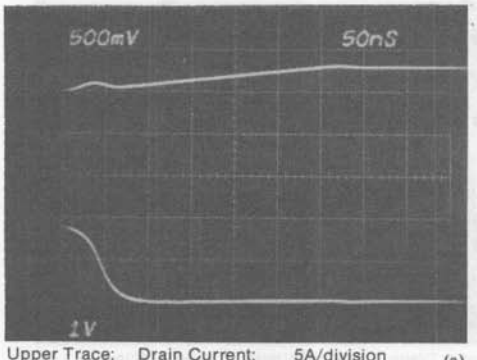
(a)



Upper Trace: Drain Current: 1A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

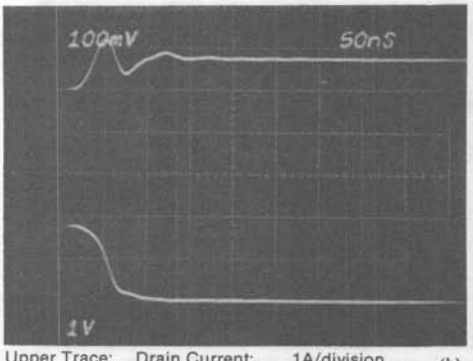
(b)

Figure 11. Oscillograms of Drain Voltage and Current, 265V Line Input



Upper Trace: Drain Current: 5A/division
50ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

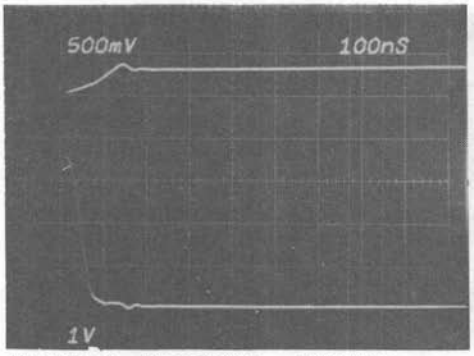
(a)



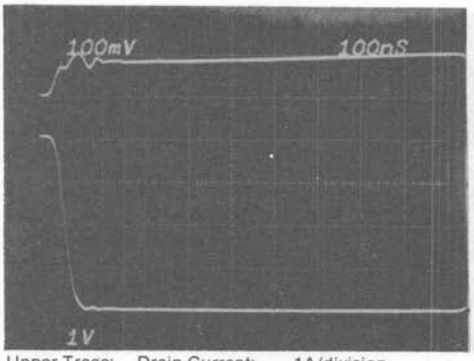
Upper Trace: Drain Current: 1A/division
50ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

(b)

Figure 12. Oscillograms of Drain Voltage and Current During Turn-On, 85V Line Input

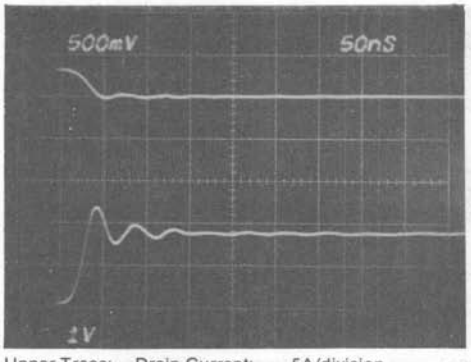


Upper Trace: Drain Current: 5A/division, 100ns/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 20A
(a)

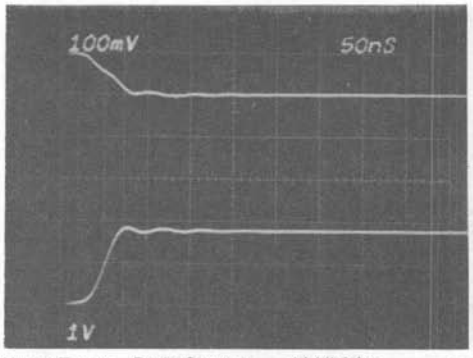


Upper Trace: Drain Current: 1A/division, 100ns/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 5A
(b)

Figure 13. Oscillograms of Drain Voltage and Current During Turn-On, 265V Line Input

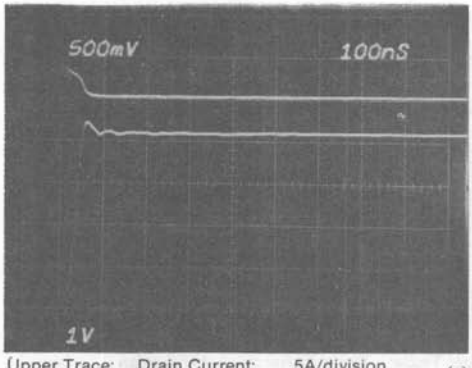


Upper Trace: Drain Current: 5A/division, 50ns/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 20A
(a)

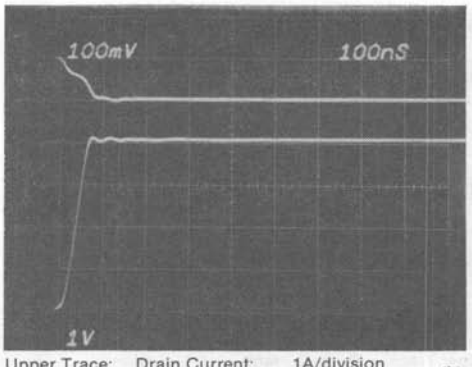


Upper Trace: Drain Current: 1A/division, 50ns/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 5A
(b)

Figure 14. Oscillograms of Drain Current and Voltage During Turn-Off, 85V Line Input



Upper Trace: Drain Current: 5A/division, 100ns/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 20A
(a)



Upper Trace: Drain Current: 1A/division, 100ns/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 5A
(b)

Figure 15. Oscillograms of Drain Current and Voltage During Turn-Off, 265V Line Input

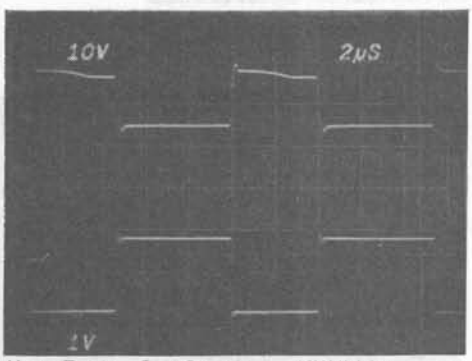
the HEXFET. Figure 15(a) and (b) show corresponding oscillograms during turn-OFF, with 165V input.

In Figures 11 and 15, it can be seen that with the maximum line input voltage of 265V, the peak voltage developed across the HEXFET at full load, including the voltage "spike" when switching OFF, is about 440V. This is comfortably within the 500V rating of the device.

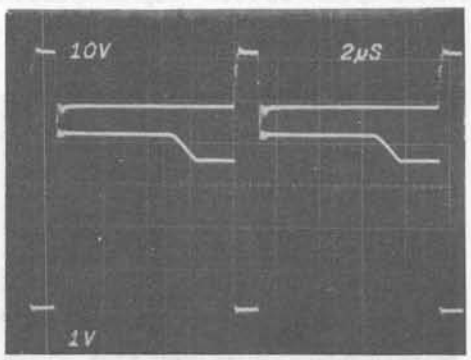
Figure 16(a) and (b) shows oscillograms of the gate-to-source and drain-to-source voltages at line input voltages of 85V and 265V, respectively, with the full load output current of 20A, while Figure 17 shows oscillograms of voltage across the output rectifiers, D_1 and D_2, with 5A output current, for input voltages of 85V and 265V. Note that with 265V input, the voltage across the output freewheeling rectifier, D_2, including the transient commutation spike, is about 75V. Note that the peak voltage across rectifier D_1, including the commutation "spike", is less than 20V, which means that a 30V-rated Schottky is adequate.

Figure 18(a) and (b) shows the transient response to the output voltage to a step change in output current from 10A to 20A, and vice versa, with 85V input, while Figure 19(a) and (b) shows corresponding oscillograms for 265V input.

Figure 20(a) and (b) shows oscillograms of drain current and drain voltage with a short circuit applied at the output, at input voltages of 85V and 265V, respectively. With 85V input, the peak HEXFET current is regulated to about 3A, by the automatic current limiting facility built into the control circuit, and the corresponding DC output current is just over 20A. With 265V input, however, the peak HEXFET current is about 7A, the short circuit DC output current is about 55A, and the peak HEXFET voltage is almost 500V. The lack of effective current limiting under this condition is due to the fact that the control circuit has a minimum ON conduction time of about 0.8 microseconds, and this is not short enough to keep the current under control under short circuit conditions.

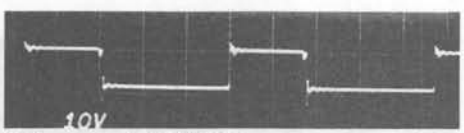


Upper Trace: Gate-Source Voltage: 10V/division, 2μs/division
Lower Trace: Drain Voltage: 100V/division, Line Input: 85V (a)

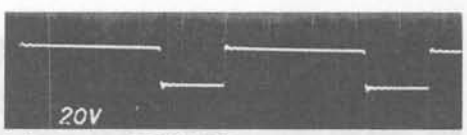


Upper Trace: Gate-Source Voltage: 10V/division, 2μs/division
Lower Trace: Drain Voltage: 100V/division, Line Input: 265V (b)

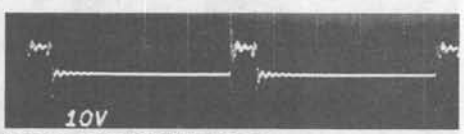
Figure 16. Oscillograms of Gate-Source Voltage and Drain Voltage, 20A Output



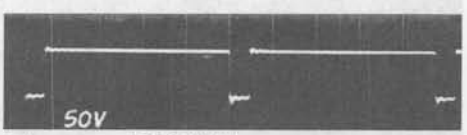
Voltage across D1: 10V/division, 2μs/division
Input: 85V (a)



Voltage across D2: 20V/division, 2μs/division
Input: 85V (b)

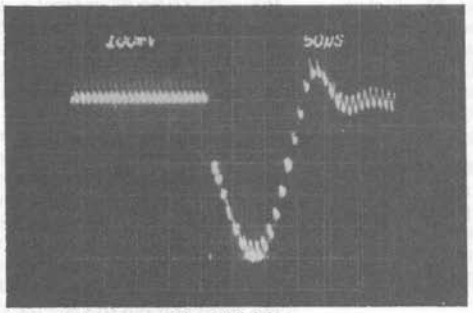


Voltage across D1: 10V/division, 2μs/division
Input: 265V (c)



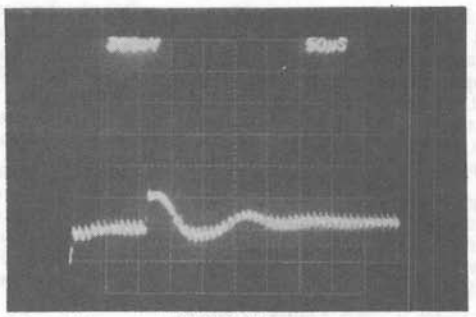
Voltage across D2: 50V/division, 2μs/division
Input: 265V (d)

Figure 17. Oscillograms of Voltage Across Output Rectifiers D1 and D2, 5A Output Current



Output Voltage: 100mV/division
50μs/division
Step Load Change: 10A to 20A

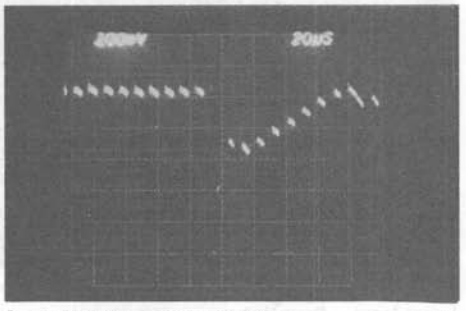
(a)



Output Voltage: 100mV/division
50μs/division
Step Load Change: 20A to 10A

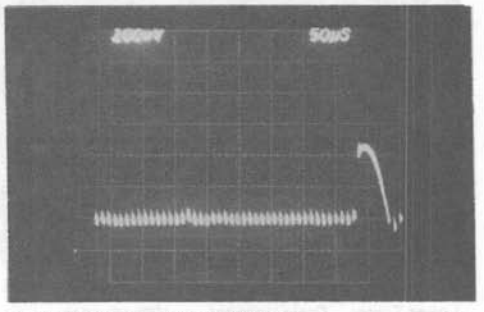
(b)

Figure 18. Oscillograms of DC Output Voltage During Step Change of Output Load Current, 85V Line Input



Output Voltage: 100mV/division
50μs/division
Step Load Change: 10A to 20A

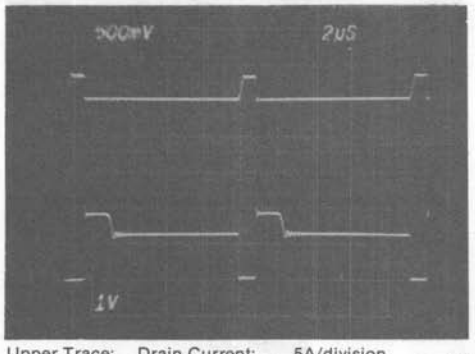
(a)



Output Voltage: 100mV/division
50μs/division
Step Load Change: 20A to 10A

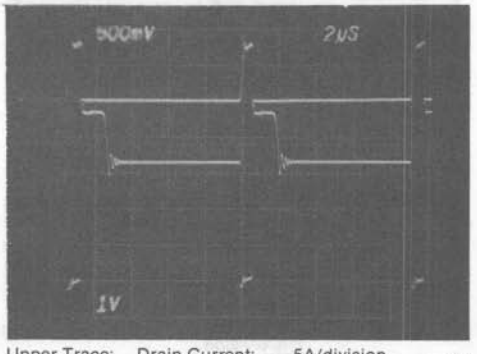
(b)

Figure 19. Oscillograms of DC Output Voltage During Step Change of Output Load Current, 265V Line Input



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 85V

(a)



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 265V

(b)

Figure 20. Oscillograms of Drain Voltage and Current with Short Circuit at Output

Attention should be paid to this point in a production design. A solution could be to add a circuit that clamps the "soft start" terminal of the control circuit to ground when the output current exceeds a predetermined level, thereby switching OFF the power supply. Resetting would be done manually once the fault condition has cleared. While this design aspect certainly needs consideration, it is of interest to see that the circuit continues to operate satisfactorily, albeit under high stress, with a short circuit output current close to 3X the rated value.

Generally, our objective has been to demonstrate the feasibility of the basic circuit concepts described, and we have not paid particular attention to design details that can be handled in a rather routine manner, according to the particular requirements of the designer. In this vein, we have taken for granted that 15V DC is available to supply the control circuit. This auxiliary DC supply could be derived from a small line frequency transformer with a rectifier and a relatively coarse voltage regulator. A 12V to 16V range of regulation would be quite satisfactory. Current consumption of the control circuit is 50mA maximum, which equates to a total power dissipation in this auxiliary power supply circuit of a little over 2W at maximum input voltage, and less than 1W at minimum input voltage.

Power Losses and Overall Efficiency

Table 3 shows the power dissipation in the various individual components of the circuit, as well as the overall efficiency, for various levels of output power, at input voltages of 90V and 260V. This data has been obtained through a combination of measurement and estimation.

The DC power delivered from the input bridge rectifier, and the DC output power, are measured directly, and the overall loss in the intervening circuitry is derived from the difference of these two measurements. The loss in the input rectifier, the HEXFET, the output rectifier, and an assumed auxiliary DC control power supply, fed from the input line through a transformer (as discussed above), are estimated individually from a knowledge of the operating voltage and currents for these components. The loss in the clamp circuit is calculated from the measured voltage across the clamp resistor; and the power loss in the output transformer and filter choke is taken as the difference between the total power dissipation, and the sum of the losses in the other components.

The overall full load efficiency arrived at in this way is 76% at 265V input, and 74% at 85V input. It should be added that an EMI filter, required in a practical system, but not included here, would reduce the overall efficiency slightly from the values shown here.

"Wide Range" Versus "Dual Range"

A point of contention may have arisen in the mind of the astute reader. This is that it is a usual design requirement to maintain rated DC output voltage during loss of the input line voltage for one cycle. In order to do this, the input reservoir capacitor, C_I in Figure 9, must be sized to supply the required energy to the output, while its voltage must not deplete below a level at which control of the output voltage can be maintained. If this capacitor is sized to supply the required energy when operating from a 115V input, as it should be, it will then be grossly oversized for operation from a 240V input, and most likely will be larger and more expensive than the capacitance required by a conventional power supply.

A conventional "dual voltage" power supply can operate either from 115V or 240V input, by means of switching from a voltage doubler circuit when operating at 115V, to a full rectifier bridge circuit when operating at 240V, with the two "doubler" capacitors then connected directly in series across the output of the bridge. Substantially the same primary DC source voltage is thereby maintained for both AC input voltage levels.

Taking the specific case of a 100W supply, the choice would then typically be between the single 500μF 450V capacitor, shown in Figure 21(a), for the wide range power supply, versus two 600μF 200V capacitors, shown in Figure 21(b), for the "dual voltage" supply. The single capacitor in Figure 21(a) has approximately 30% more volume than the combined volume of the two capacitors shown in Figure 20(b); the cost differential is about 11%, or $0.60 extra for the capacitor for the wide range power supply. This could be more than compensated for by the fact that the additional complication of switching from a doubler to a bridge configuration is eliminated, to say nothing of the functional convenience of not having to make any adjustments when operating from 115V or 240V input.

A quite different aspect is that if the wide regulation capability of the circuit is utilized only under the short-term condition of loss of input line voltage for one cycle, then a drastic reduction in the size of the input reservoir capacitance can be made. This is because the voltage across this capacitor can then be allowed to "drift" all the way from, say, 310V down to 120V, during the one-cycle "outage" period.

Table 3. Power Losses and Overall Efficiency Under Various Operating Conditions

Line Input Voltage V	DC Output Voltage V	Power Output W	Total Power Loss W	Estimated Power Loss in Input Rectifier W	Estimated Power Loss in HEXFET W	Power Loss in Clamp Circuit W	Estimated Power Loss in Transformer and Filter Choke W	Estimated Power Loss in Output Rectifier W	Estimated Power Loss in Control Circuit W	Overall Efficiency %
90	5.0	97.26	34.09	4	8.0	2.99	2.7	15.5	0.9	74
	5.0	73.11	24.4	3	4.6	2.60	2.4	10.9	0.9	75
	5.0	48.81	15.94	2	2.3	2.24	1.5	7.0	0.9	75
	5.0	24.40	9.3	1	0.8	2.02	1.28	3.3	0.9	72
260	5.0	96.96	30.22	1.3	5.4	2.02	3.3	15.5	2.7	76
	5.0	72.81	22.74	1.0	3.7	1.54	2.9	10.9	2.7	76
	5.0	48.66	16.69	0.7	2.3	1.29	2.7	7.0	2.7	74
	5.0	24.35	10.98	0.4	1.1	1.18	2.3	3.3	2.7	69

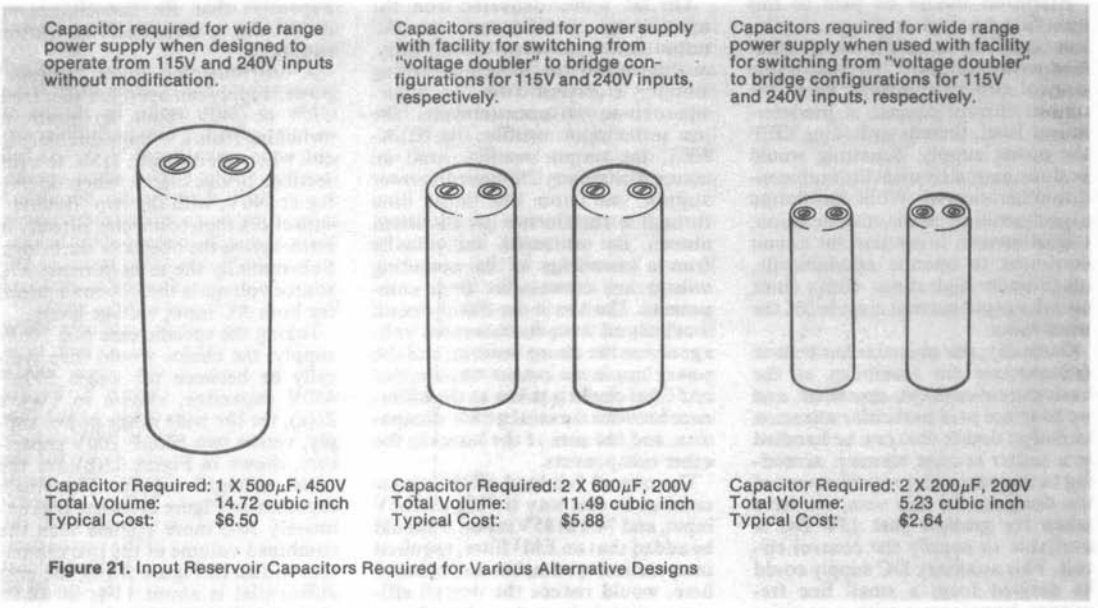


Figure 21. Input Reservoir Capacitors Required for Various Alternative Designs

With this design approach, it would be necessary to switch from a voltage doubler circuit to a bridge circuit when operating from 115V and 240V inputs, respectively, but the size of the required input capacitors would be reduced as shown in Figure 21(c). The volume of these capacitors is just under 50% of the volume of the capacitors required for a conventional "dual voltage" power supply, and the cost is approximately 45% — an absolute saving in the region of $3.00.

Conclusions

In order to get the most out of a power HEXFET, it is necessary to rethink basic concepts, and to design the circuitry to take maximum advantage of the special operating features of the device. An illustration of this basic precept is the 100kHz, 100W "universal" switching power supply described in this article. The circuit uses a single 500V-rated HEXFET to provide a regulated 5V DC output, over the entire range of line input voltage from 85V to 265V. □