KURK MATHEWS, LINEAR TECHNOLOGY CORP, MILPITAS, CA

It is often desirable to synchronize a switching power supply to a system clock or to a second supply. If the power-supply controller has no synchronization pin, you can add a low-value resistor in series with the oscillator capacitor, thereby developing a synchronization pulse to sum into the oscillator ramp. Depending on the controller, this method may have drawbacks. Primarily, the wider the synchronization range, the higher the sync-pulse amplitude required (without exceeding the controller's internal reference voltage). Further problems arise if the controller IC uses the oscillator ramp for voltage-mode control, slope compensation, or timing. Under these circumstances, modifying the amplitude of the oscillator ramp may not be an option. Such is the case with IC_1 in **Figure 1**, an LT1509 PWM and power-factor controller, which depends on ramp amplitude for determining the phase relationship between the power-factor and PWM sections and for determining duty cycles.

The circuit in **Figure 1** uses a PLL to adjust the oscillator-ramp charge current, providing a wide synchronization range without changing oscillator voltage levels. Q_1 to Q_3 form a comparator that supplies a square wave (at the oscillator frequency) to IC_2. IC_2's phase comparator II output adjusts the oscillator-ramp charge current until the oscillator frequency equals the input frequency. The method provides synchronization and preserves the oscillator waveform and the IC's function. With the values shown, the frequency-lock range is 90 to 150 kHz. The circuit requires less than 1 mA from a 12V supply. (DI #2233) EDN

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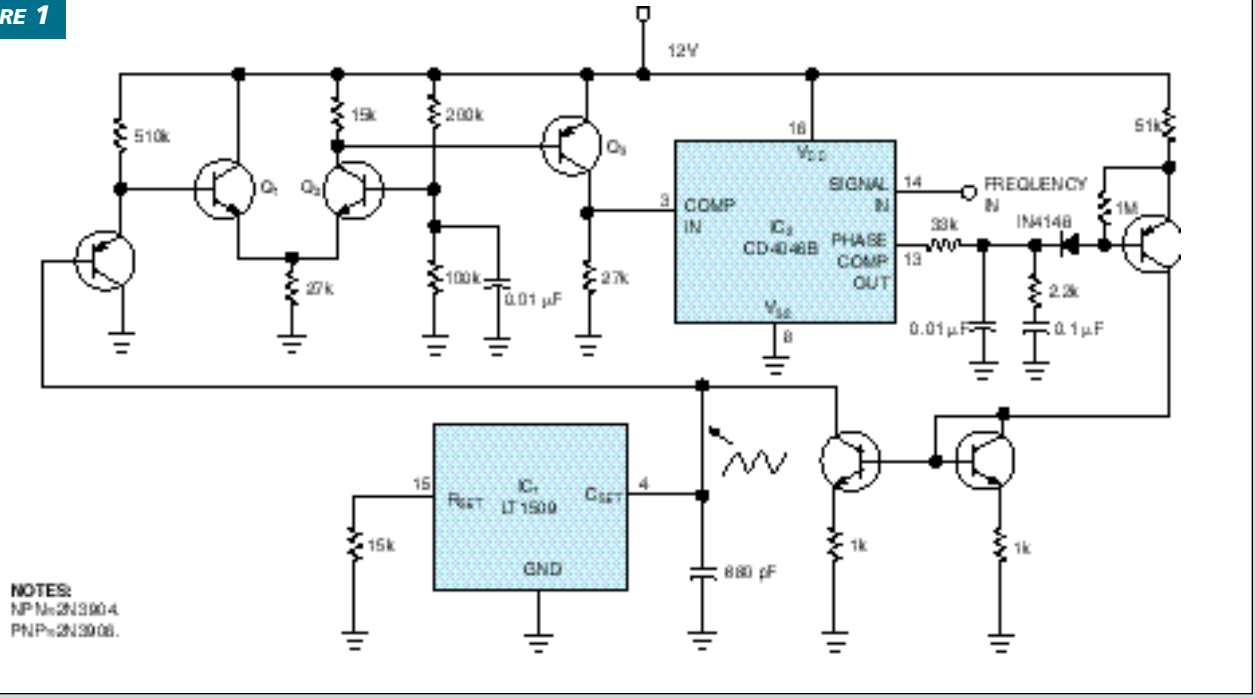
FIGURE 1



A PLL provides frequency synchronization for a PWM and power-factor-controller IC.