ED ONLINE 20893

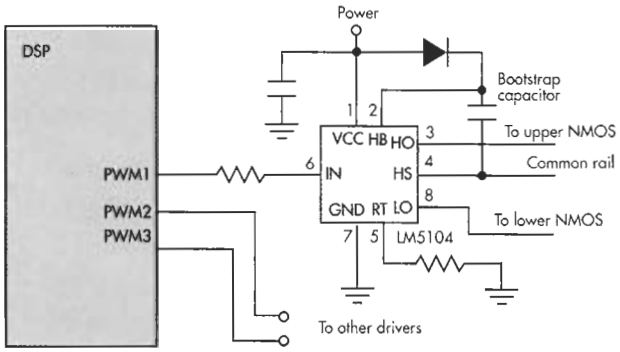
ANTONIO MUÑOZ AND ARTURO MEDIANO
P.T. WALQA, HUESCA, SPAIN, AND 13A-UNIV. OF ZARAGOZA, ZARAGOZA, SPAIN
anmunoz@unizar.es; amediano@unizar.es

Simple Solution Provides PWM Signal Fault Protection

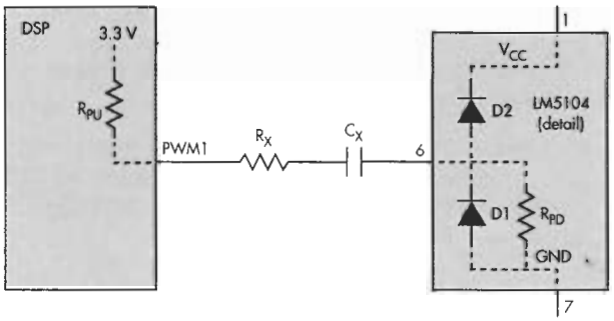
This idea was created to solve a design problem we faced a few months ago. The circuit we were working on was used to steer an H-bridge that was controlled by a TMS320F2810 digital signal processor (DSP).

During the final phase of the design, we discovered by chance that everything worked fine when the circuit was initially powered. However, if it was powered off for 5 to 15 seconds and then powered on again, the circuit started draining a lot of current through the H-bridge/load. This destabilized the power supply, and the DSP was kept in reset.

After some hardware and software debugging, we found that the problem was a steady high level on the pulse-width modulation (PWM) control lines when the TMS320F2810 was held in reset (power up). This DSP has internal pull-ups (20 to 80 kΩ) enabled on the uninitialized PWM outputs in order to maintain the pins at a known, defined level. Because the DSP-PWM pins are current limited to ±4 mA, they were interfaced to a MOSFET driver (LM5104) through a bootstrap capacitor to drive the H-bridge *(Fig. 1)*.



1. In this (simplified) schematic of a DSP-to-MOSFET driver interface, problems arose when the circuit was powered off for 5 to 15 s and powered on again.



2. The solution to the problems of the circuit in Figure 1 ensures that the level is high only for a defined period, without affecting the PWM signal and with only a small increase in the power drain.

This type of driver works very well, but the bootstrap capacitor should not be discharged completely (as in the case of a steady high level in pin 6). Although the MOSFET driver has an internal pull-down resistor attached to pin 6, its value is around 200 kΩ, which is much higher than the DSP pull-up. Because of that, the input level is held high when the system is in reset.

An additional pull-down resistor on pin 6 would have solved the problem, but at the cost of a higher current drain (the resistor value must be lower than the DSP pull-up) and longer low-to-high transitions. But the proposed solution *(Fig. 2)* guarantees that the output is high only for a defined period (depending on the values of R_X, R_{PD}, and C_X) without affecting the PWM signal and with only a small increase in the power drain.

In this solution, C_X defines the maximum high period and R_X limits the transient current when the PWM signal is switching. R_X and C_X are determined by:

$$R_X = \frac{V_{DSP}}{I_{IO-LIM}}$$

$$V_{TH} = V_{DSP}\left(e^{\frac{-T_{MAX}}{R_T C_X}}\right) \Rightarrow C_X = \frac{-T_{MAX}}{R_T \times \ln\left(\frac{V_{TH}}{V_{DSP}}\right)}$$

where:
V_{DSP} is the DSP I/O supply,
I_{IO-LIM} is the current limit for a DSP I/O pin,
T_{MAX} is the maximum allowed pin 6 high time,
V_{TH} is the threshold voltage of pin 6, and
$R_T = R_{PU} + R_X + R_{PD}$.

Assuming that C_X is initially discharged and pin 6 is high, C_X will be progressively charged through R_{PU}, R_X, and R_{PD}. If PWM1 toggles to low in a time shorter than T_{MAX}, C_X will discharge fast through R_X and D1 and the cycle starts again. But if PWM1 stays high longer than T_{MAX}, the voltage on pin 6 will go under V_{TH} and the LM5104 will switch the output to low.

Because of component tolerances, the calculation of T_{MAX} is approximate. In practice, that poses no problem since controlled system evolution is far slower than the PWM control signal. One final tip: To limit the circuit EMI and prevent latch-up, the value of R_X should be higher than that calculated by the formula.

ANTONIO MUNOZ, R&D engineer, Advanced Laboratories, University of Zaragoza, holds an MSc in telecommunications engineering from the University of Zaragoza.
ARTURO MEDIANO, professor and senior member of the IEEE, holds an MSc and PhD in electrical engineering from the University of Zaragoza.