YUMING BAI, Senior Staff Engineer • **JIM BROILES**, Senior Manager Strategic Marketing,
Vishay Intertechnology Inc., Santa Clara, Calif.

Measuring Power Losses of Heat Sources in Switch-Mode Converters

A new methodology obtains power losses using dc power measurements and a thermal camera to measure the surface temperature of each heat source on a printed circuit board.

The efficiency and power losses of dc-dc converters are important characteristics of many electronic systems. These characteristics can be measured and expressed in a straightforward manner as follows:

Efficiency = output power / input power (Eq. 1)

Power loss = input power – output power. (Eq. 2)

But such results provide no information on the contribution of each component as an individual heat source. A new methodology addresses this problem, allowing designers to better choose the best dc-dc implementation for their application.

The major sources of heat in a buck converter are the high-side MOSFET, the low-side MOSFET and the inductor. If we use an electrical method to determine the power losses on high-side and low-side MOSFETs, then we must measure the instantaneous drain current, drain-to-source voltage, gate current and gate-to-source voltage. Unfortunately, these measurements are difficult to obtain in high-frequency dc-dc converters without introducing extra inductance in the current path and disturbing the circuit's normal operation. With the help of a thermal camera, however, we have developed a new method to extract the power loss of each heat source without affecting circuit operation.

MEASUREMENT PRINCIPLES

In an electrical circuit, a heat source converts electrical energy into thermal energy. Energy converted to heat increases the temperature of the source and the area surrounding it. The amount of energy converted to heat is the component's power loss. All temperature rises (ΔT) depend on the power loss (P) and the environment. For a certain PCB on a fixed test bench, ΔT is only a function of power loss. Therefore, if we can measure ΔT, then we can derive a method for calculating the power loss of each heat source.

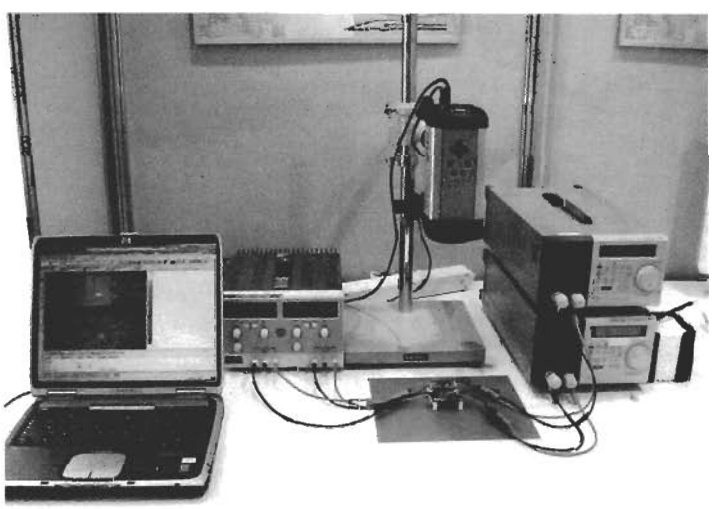

Fig. 1. Integrated power stage has four heat sources: inductor, driver IC, high-side MOSFET and low-side MOSFET.

For the simplicity, assume there are two heat sources, HS1 and HS2, on the PCB. The operation of HS1 not only makes its own surface temperature higher, but also increases the surface temperature of HS2, and vice versa. Hence, the final ΔT of each heat source could be expressed as:

$$\begin{pmatrix}\Delta T_1\\ \Delta T_2\end{pmatrix}=\begin{pmatrix}S_{11} & S_{12}\\ S_{21} & S_{22}\end{pmatrix}\begin{pmatrix}P_1\\ P_2\end{pmatrix}, \quad \text{(Eq.3)}$$

where:

$S_{ij\ (i,j\ =\ 1,2)}$ = Coefficients of thermal sensitivity with the same dimensions as thermal resistance

Pi = Power loss of each heat source.

Eq. 3 could be extended to N heat sources. In this case, the temperature rise of each heat source is:

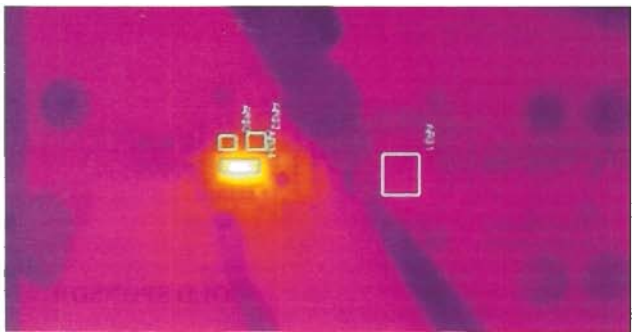

Fig. 2. This thermal image of SiC739EVB shows the temperature of the four heat sources when the body diode of the low-side MOSFET is forward-biased.

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ . \\ \Delta T_N \end{pmatrix} = S \cdot \begin{pmatrix} P_1 \\ P_2 \\ . \\ P_N \end{pmatrix}, \quad \text{(Eq.4)}$$

where S is an N × N matrix.

If we know the value of S, then the power loss of each heat source can be found by:

$$\begin{pmatrix} P_1 \\ P_2 \\ . \\ P_N \end{pmatrix} = S^{-1} \cdot \begin{pmatrix} \Delta T \\ \Delta T_2 \\ . \\ \Delta T_N \end{pmatrix}. \quad \text{(Eq.5)}$$

Assuming S_{ij} doesn't depend on temperature or operation of the circuit, then each S_{ij} could be determined by:

$$S_{ij} = \frac{P_j}{\Delta T_i}, \quad \text{(Eq.6)}$$

where:

ΔT_i = Temperature rise on the ith heat source

P_j = Power consumed by the jth heat source

All other components are disabled.

We used simple dc techniques to energize one heat source at a time, such that the coefficients of thermal sensitivity can be measured in a non-invasive manner. We applied dc voltage and current to force the components under test (the IC, MOSFET and inductor) to begin consuming power, which was then measured for P_j. Then we used the thermal camera to measure the surface temperature ΔT_i. S_{ij} can then be calculated using Eq. 6.

We used the new methodology to calculate the power loss of the major heat sources of two buck topologies: an integrated power stage using the SiC739D8 DrMOS IC, and a discrete power stage using two MOSFETs — Si7382DP on the high side and Si7192DP on the low side.

INTEGRATED BUCK CONVERTER

Fig. 1 shows the front side of the EVB for integrated buck converter. There are four heat sources: the inductor (HS1), the driver IC (HS2), the high-side MOSFET (HS3) and the low-side MOSFET (HS4). The SiC739 DrMOS is a single IC solution that contains HS2, HS3 and HS4 in very close proximity. Because there are four heat sources, S is a 4 × 4 matrix. The components of S are obtained by forcing current through each heat source one at a time.

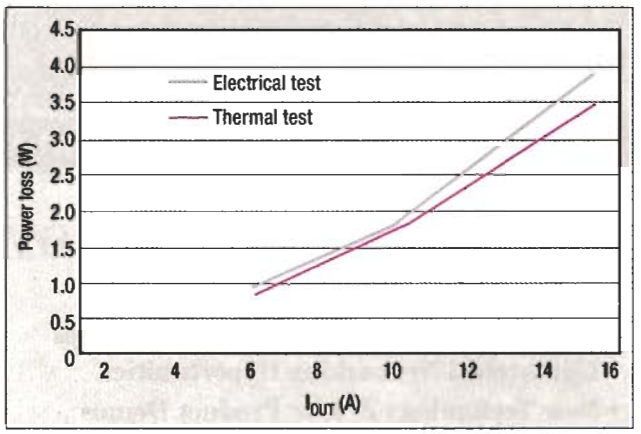

Fig. 3. A comparison of the thermal and electrical methods, whose difference is due to minor heat sources such as PCB traces and ESR in the capacitors.

Fig. 2 shows the temperature of the four heat sources when the body diode of the low-side MOSFET is forward-biased (AR0x Avg. => HSx).

If T_A is 23.3°C, then:

ΔT_{14} = 8.2°C

ΔT_{24} = 13.1°C

ΔT_{34} = 13.4°C

ΔT_{44} = 22.8°C.

Measured current I_4 and voltage V_4 are 2.14 A and 0.6589 V, respectively. Therefore:

$P_4 = I_4 \times V_4$ = 1.41 W.

Using the temperature information of TA, we have S_{i4}, (i=1, 2, 3, 4)

S_{14} = 5.82

S_{24} = 9.29

S_{34} = 9.5

S_{44} = 16.2

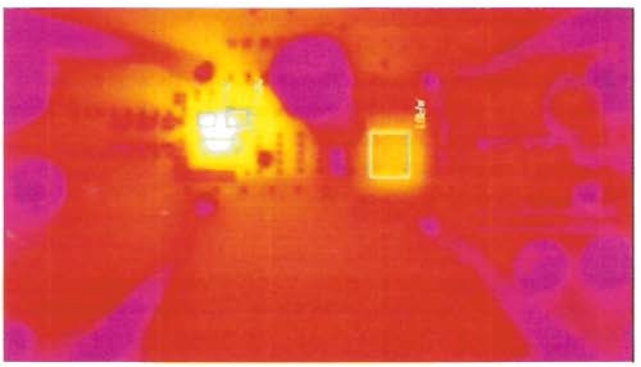

Fig. 4. Integrated EVB, V_{IN} = 12 V, V_O = 1.3 V, F_S = 1 MHz, I_O = 8 A for the S matrix of the discrete implementation simply by not considering the power in the driver IC.

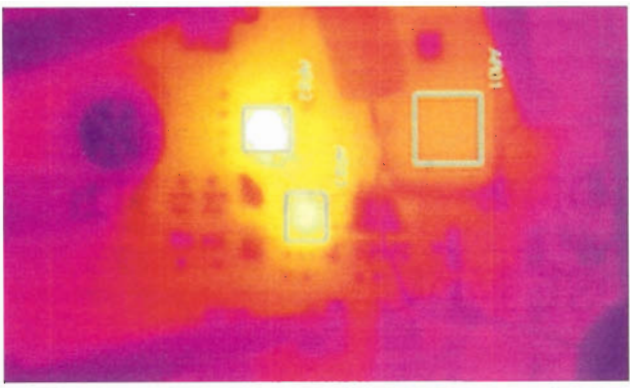

Fig. 5. Discrete buck EVB, power losses for V_{IN} = 12 V, V_0 = 1.3 V, F_S = 1 MHz, I_0 = 8 A.

By repeating this procedure, the S matrix is found to be:

$$S = \begin{pmatrix} 29.6 & 5.9 & 5 & 5.82 \\ 12.4 & 18.3 & 9.7 & 9.29 \\ 10.9 & 10.5 & 15.4 & 9.5 \\ 12.1 & 10.2 & 9.6 & 16.2 \end{pmatrix} \quad \text{(Eq.7)}$$

and

$$S^{-1} = \begin{pmatrix} 0.042 & -5.994\times10^{-3} & -4.015\times10^{-3} & -9.118\times10^{-3} \\ -0.015 & 0.097 & -0.039 & -0.027 \\ -9.17\times10^{-3} & -0.043 & 0.122 & -0.044 \\ -0.016 & -0.032 & -0.045 & 0.112 \end{pmatrix} \text{(Eq.8)}$$

EXPERIMENTAL RESULTS: INTEGRATED BUCK CONVERTER

Now, we can power up the SiC739 EVB and use Eqs. 5 and 8 to calculate the power loss of each heat source:

P_1 = 0.224 W, inductor
P_2 = 0.431 W, driver IC
P_3 = 0.771 W, high-side MOSFET
P_4 = 0.512 W, low-side MOSFET.

By measurement and Eq. 2:

$P_1 + P_3 + P_4$ = 1.538 W.

The new method gives:

$P_1 + P_3 + P_4$ = 1.507 W.

Fig. 3 shows the difference between the thermal and electrical methods can be attributed to minor heat sources such as PCB traces and ESR in the capacitors.

DISCRETE BUCK CONVERTER

Using the above procedure and Fig. 4 we obtain the S matrix for the discrete implementation simply by not considering the power in the driver IC.

ΔT_{13} = 10.5°C, inductor
ΔT_{23} = 13.8°C, high side
ΔT_{33} = 24.7°C, low side, then:

$S_{13} = 7.5$
$S_{23} = 9.86$
$S_{33} = 17.6$

$$S = \begin{pmatrix} 28.4 & 6.22 & 7.5 \\ 12.8 & 17.5 & 9.86 \\ 13.9 & 8.85 & 17.6 \end{pmatrix}. \quad \text{(Eq.9)}$$

Using the information in Fig. 5, we find the power losses at $V_{IN} = 12$ V, $V_O = 1.3$ V, $I_O = 8$ A, $F_S = 1$ MHz.

$P_1 = 0.228$ W, inductor

$P_2 = 0.996$ W, high-side MOSFET

$P_3 = 0.789$ W, low-side MOSFET

Comparing the power for P_1, P_2, P_3 and P_4 of the discrete and integrated buck converter, we find that the two circuits have the same inductor loss as would be expected because they use the same inductor. The power losses of the integrated buck solution are less than the discrete buck even though the $R_{DS_{ON}}$ of the discrete MOSFETs is 23% (low side) and 28% (high side) lower than the integrated MOSFET. Therefore, we can conclude that the integrated solution leads to less frequency related power loss.