INTERLEAVED FORWARD CONVERTERS LOWER CAPACITOR RIPPLE CURRENTS, CUT COMPONENT COST AND SIZE, AND INCREASE RELIABILITY IN LOW-VOLTAGE, HIGH-CURRENT-OUTPUT VOLTAGE-REGULATION MODELS.

Interleaved forward converters transform voltage-regulation models

VRMs (voltage-regulation modules) that power the latest generations of computer CPUs have historically used multiphase, interleaved buck converters. These VRMs must meet the tight Pentium 4 and Athlon CPU voltage-regulation and -transient requirements. Because of their reduced input-capacitor rms current, reduced output-capacitor ripple current, and smaller output-capacitor bank as compared with those of standard buck converters, interleaved step-down converters are ideal for these low-voltage, high-current applications. By interleaving two forward converters, IFCs (interleaved forward converters) provide benefits similar to those that designers might obtain by interleaving a pair of buck converters. In high-current applications, such as intermediate bus or merchant power, an IFC can be more beneficial than a standard forward converter.

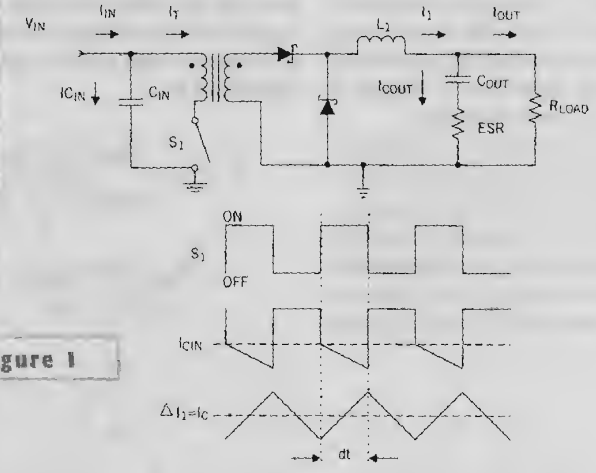

Figure 1

A traditional forward converter exhibits discontinuous input current.

TRADITIONAL FORWARD CONVERTER

A traditional forward converter exhibits discontinuous input current, which the input capacitor (C_{IN}) must filter (**Figure 1**). Using the input capacitor for this purpose causes the capacitor to carry a high input ripple current (I_{CIN}).

To meet output-ripple-voltage (V_{RIPPLE}) requirements, the output filter inductor (L_1) is sized to have an inductor ripple current (I_{L1}) that is roughly 25 to 30% of the output current (I_{OUT}):

$$L_1 = \frac{V_{OUT} \times dt}{0.30 \times I_{OUT}}.$$

The output capacitor (C_{OUT}) is sized to suppress the inductor ripple current. To meet output-voltage-ripple requirements, the following equations estimate the maximum ESR (equivalent series resistance) and minimum output capacitance. In normal practice, the ESR requirement dominates

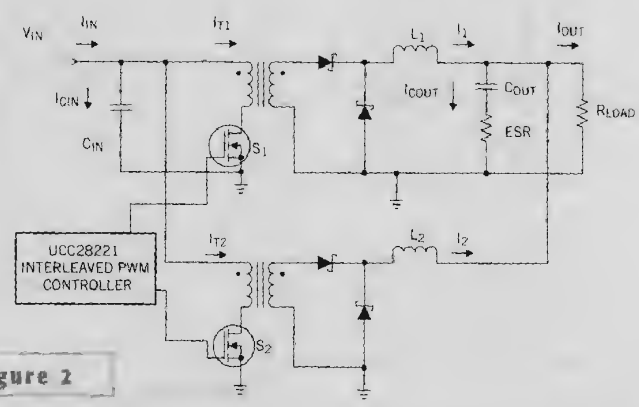

Figure 2

An interleaved dual forward converter comprises two forward converters operating 180° out of phase.

the capacitor selection, resulting in more capacitance than is needed to suppress the inductor ripple current:

$$ESR \le \frac{V_{RIPPLE}}{\Delta I_{L1}},\ C_{OUT} \ge \frac{\Delta I_{L1}}{8 \times f_S \times V_{RIPPLE}}.$$

BENEFITS OF A DUAL IFC

An interleaved dual forward converter comprises two forward converters operating 180° out of phase, providing the benefits of reduced input-capacitor rms current and reduced output-capacitor ripple current (**Figure 2**).

Each forward converter exhibits discontinuous input current (for example, I_{T1} and I_{T2}). The converter's input current is the sum of these two discontinuous currents, and, because they are 180° out of phase, the input current becomes more continuous and approaches dc. The input capacitor (C_{IN}) must filter only the ac portion of the input current. Interleaving the two converters drastically reduces the required input capacitance. **Figure 3** shows the rms current reduction.

The output current (I_{OUT}) in this interleaved converter is the sum of the inductor currents (I_1+I_2) minus the capacitor current (I_{COUT}). The output capacitor in this application must also suppress the ac portion of the current through the output filter inductors. However, because the two converters operate 180° out of phase, the inductor ripple currents cancel each other, providing a more continuous output current. This effect reduces the amount of ripple current that C_{OUT} must suppress. The output capacitance is sized similarly to the single phase-forward converter for output-voltage-ripple requirements, except that the interleaved converter's output capacitor need not suppress the entire inductor ripple current. The IFC's output capacitor can thus have a greater ESR than is permissible in the traditional converter:

$$ESR \le \frac{V_{RIPPLE}}{\Delta I_{COUT}},\ C_{OUT} \ge \frac{\Delta I_{COUT}}{8 \times f_S \times V_{RIPPLE}}.$$

Theoretically, the IFC's output-inductor ripple-current cancellation allows the designer to reduce the size of the filter inductor. However, the total inductance is generally the same size as that in a traditional forward converter to reduce the total losses in high current applications (**Reference 1**):

$$L_1 = L_2 \ge \frac{V_{OUT} \times (1-D_{MIN}}{(0.6) \times \left(\frac{I_{OUT}}{2}\right) \times f_S} =$$

$$\frac{V_{OUT} \times (1-D_{MIN})}{0.3 \times I_{OUT} \times f_S}.$$

It is important for the designer to know that the maximum reduction in capacitor current occurs at a 50% duty cycle. **Figure 4** shows the input- and output-capacitor current waveforms at roughly 40% duty cycle. Because the duty cycle is less than 50%, the interleaved converter's input current is less continuous than the traditional converter's and increases the input capacitance's rms current. The output-inductor ripple currents are no longer symmetrical and do not cancel when the converters are operating at 50% duty cycle. This asymmetry increases the output capacitor ripple current.

The following equations and the graph in **Figure 5** show how the input-capacitor rms current, I_{CIN}(rms), behaves with changes in duty cycle. N is the transformer turns ratio. Note that the lowest input-capacitor rms current occurs at 50% duty cycle and the highest rms current occurs at 25 and 75% duty cycle. The rms current is still less than half of the traditional forward converter at 25 and 75% duty cycle.

For input-capacitor rms current at D of less than or equal to 0.5:

$$I_{CIN}(RMS) \approx \frac{I_{OUT}}{2 \times N} \times \sqrt{2 \times D(1-2 \times D)}.$$

For input-capacitor rms current at D of greater than 0.5:

$$I_{CIN}(RMS) \approx \frac{I_{OUT}}{2 \times N} \times \sqrt{4 \times D(1-0.5 \times D)(1-D)}.$$

The following equations and the graph of **Figure 6** show how the ratio of output-capacitor ripple current and the change in inductor current vary with duty cycle. **Figure 6** illustrates that the maximum inductor ripple current cancellation occurs at 50% duty cycle:

$$\frac{\Delta I_{COUT}}{\Delta I_{L1}} = \frac{1-2 \times D}{1-D} \text{ IF } D < \text{OR} = 0.5$$

$$\frac{\Delta I_{COUT}}{\Delta I_{L1}} = \frac{1-2 \times (1-D)}{1-(1-D)} \text{ IF } D > 0.5.$$

DESIGN CONSIDERATIONS

Designing an IFC to get the maximum reduction in

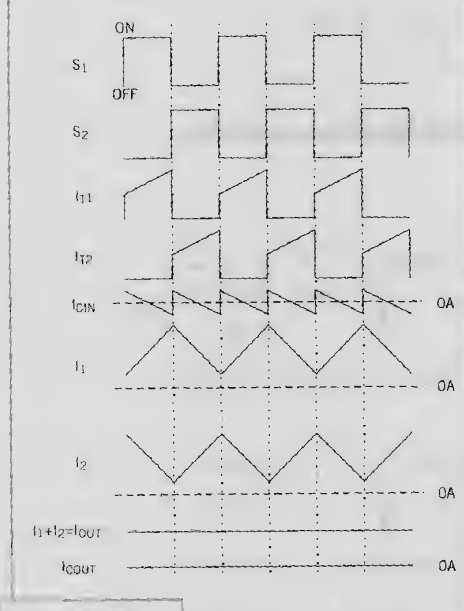

Figure 3 Interleaving reduces input-capacitor rms current (I_{CIN}) and output-capacitor ripple current (I_{COUT}).

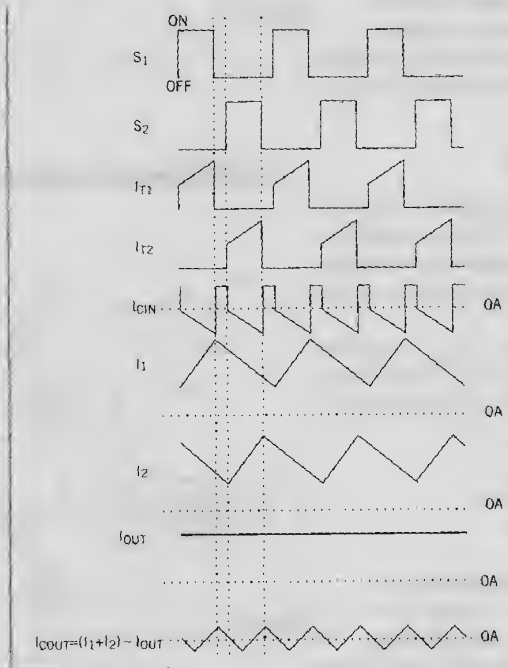

Figure 4 Ripple-current reduction decreases as the duty cycle (D) varies from 50%.

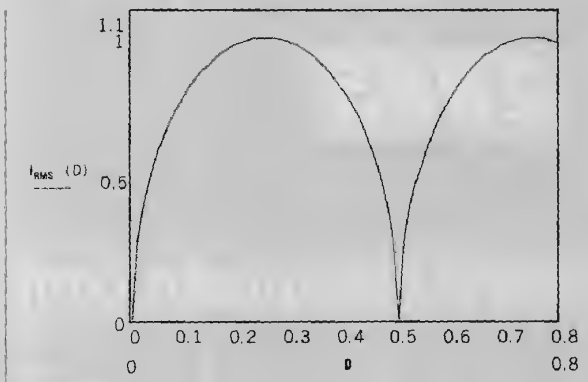

Figure 5 By analyzing normalized input-capacitor rms current versus duty cycle, you can determine the design's worst-case filter-capacitor currents.

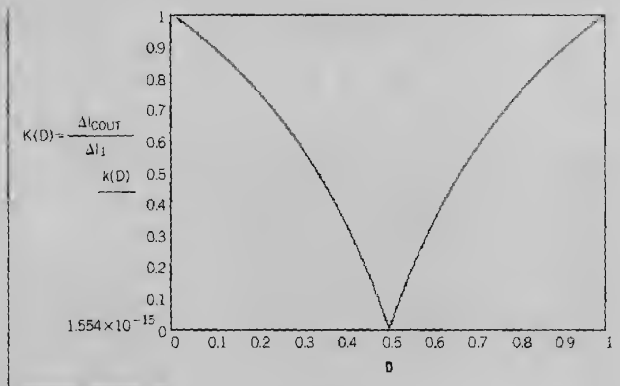

Figure 6 A plot of output-current ripple cancellation ratio versus duty cycle can also reveal the design's worst-case filter capacitor currents.

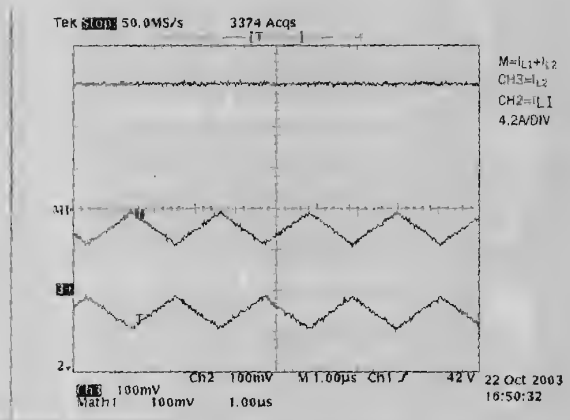

Figure 7 Ripple-current cancellation varies with the duty cycle; in this case, the power converter was operating at a 50% duty cycle.

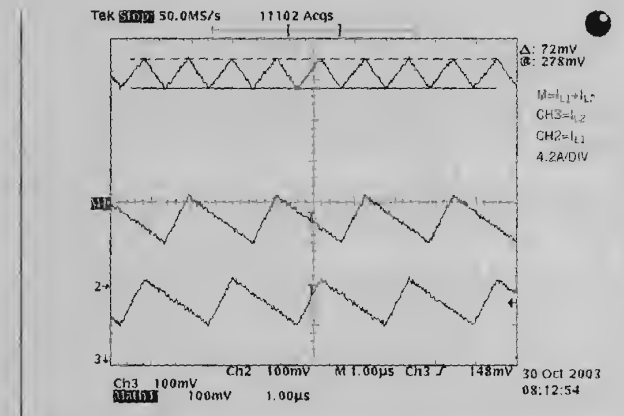

Figure 8 The converter for this oscilloscope waveform operates at a maximum line voltage of roughly 76V; the power converter operates at 30% duty cycle.

filter-capacitor currents requires the proper selection of duty-cycle range. You can achieve this goal by adjusting the transformer turns ratio, N, per the design's input- and output-voltage requirements. The following equation estimates N, where V_{IN}(MIN) is the minimum input voltage and D_{MAX} is the chosen maximum duty cycle. V_D represents the output diode's forward voltage drop:

$$\frac{1}{N} = \frac{(V_{OUT} + V_D)}{V_{IN(MIN)} \times D_{MAX}}.$$

Once you determine the maximum duty cycle and transformer turns ratio, you can calculate the minimum duty cycle (D_{MIN}). With this information and the graphs in **figures 5** and **6**, you can determine the design's worst-case filter capacitor currents:

$$D_{MIN} = \frac{(V_{OUT} + V_D) \times N}{V_{IN(MAX)}}.$$

DESIGN EXAMPLE

A dual IFC constructed using the UCC28221 interleaved PWM (pulse-width- modulator) controller shows how much the capacitor ripple current could vary with duty cycle. The 200W converter targets an input-voltage range of 36 to 76V and a regulated 12V-dc output. The two-to-one variation in input voltage would result in roughly a two-to-one variation in duty cycle. To optimize transformer reset and reduce capacitor current, the design uses a maximum duty cycle of 0.6. To minimize the size of the magnetics, each converter was designed for a 500-kHz switching frequency (f_S). The output Schottky diodes exhibit a V_D of approximately 0.3V. These parameters result in a turns ratio of 1.75- to-1 and a minimum duty cycle of 0.28.

To limit the forward converter's peak input currents, the output inductors are designed for a 60% ripple current, resulting in a filter inductor of roughly 3.5 µH. This inductance is approximately the same as that in a single-switch forward converter sized for an inductor ripple current of roughly 30% of the maximum load current:

$$L_1 = L_2 = \frac{(V_{OUT} + V_F) \times (1 - D_{MIN})}{0.6 \times \left(\frac{P_{OUT}}{V_{OUT} \times 2} \right) \times FS} \approx 3.5\ \mu H.$$

The output-capacitor maximum ripple (V_{RIPPLE}) specification for this design is 200 mV. The output-capacitor ripple current is at its greatest when the power converter is operating at its minimum duty cycle of 0.28. The output capacitance needs to suppress this ripple current to meet the output-ripple requirements. The graph in **Figure 6** shows that the output capacitor's ripple current is roughly 60% of the filter inductor's ripple current, resulting in an output-capacitor ripple current of roughly 3A. This design requires an ESR of less than 66 mΩ to meet output-voltage requirements:

$$\Delta I_{COUT} \approx \Delta I_{L1} \times \frac{1-2\times D_{MIN}}{1-D_{MIN}} \approx 3A$$

$$ESR \le \frac{V_{RIPPLE}}{\Delta I_{COUT}} \approx 67\ m\Omega.$$

The output capacitor of a traditional forward converter operating at an identical switching frequency and power level would have a maximum allowable ESR of roughly 40 mΩ. The interleaved converter allows the use of an output capacitor having an ESR 1.7 times as great. The improvement depends on the design requirements. If the converter were designed with a minimum duty cycle of 0.4, the maximum allowable ESR for a design at the same power level, the output ripple requirement would be 120 mΩ, which is roughly three times the allowable ESR of the output capacitor in a standard forward converter.

$$I_{COUT}(RMS) \ge \frac{\Delta I_{COUT}}{\sqrt{3}} \approx 1.74A.$$

The output capacitor's rms current in this interleaved design would be roughly 1.74A—roughly 60% of what it would have been in a standard forward converter.

The input-capacitor rms current would be at its highest at a duty cycle of roughly 28%. The highest input capacitor rms current would be roughly 2.4A. A traditional forward converter designed with similar power levels would have an input-capacitor rms current of roughly 4.7A. Using an interleaved converter thus reduces the input capacitor rms current by roughly half.

$$I_{CIN}(RMS) \approx \frac{I_{OUT}}{2\times N} \times \sqrt{2\times D(1-2\times D)} \approx 2.4A.$$

Oscilloscope waveforms show how the ripple current cancellation varies with the duty cycle. **Figure 7** depicts the results of a power converter operating at a 50% duty cycle. The sum of the two output inductor currents ($I_{L1}+I_{L2}$) is almost dc, resulting in almost no output-capacitor ripple current.

The oscilloscope waveform in **Figure 8** depicts the results of a converter operating at a maximum line voltage of roughly 76V. Correctly regulating the 12V output requires a duty cycle of roughly 28%. The waveform shows that the sum of the inductor currents has a 3A peak-to-peak ripple current that the output capacitor must filter. This peak-to-peak capacitor ripple current is roughly 60% of the inductor ripple current.

The dual IFC can benefit both high-current and high-power-density designs. It is ideal for intermediate bus converters and merchant power applications, because the reduced input- and output-capacitor ripple current lessens electrical stress on the input and output capacitors. Interleaved converters' inductor ripple-current cancellation allows more output-capacitor ESR, which in turn reduces the converter's output-capacitance requirements.□

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1. Chen, Sophie, "Using the TPS40090-EVM-001, User's Guide," Texas Instruments Literature No. SLUU175, pg 9.
2. Shafer, Brian, "Interleaving Contributes Unique Benefits to Forward Converters and Flyback Converters," Texas Instruments Power Supply Design Seminar, Topic 4, SEM 1600.

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