50W Forward Converter With Synchronous Rectification And Secondary Side Control

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ABSTRACT

This article reviews a new technique for secondary side control of a DC-DC converter without using an auxiliary bias supply. A unique primary side start up circuit is used to drive the primary side power transistor. Gate pulse information for the primary transistor is transmitted through a pulse transformer that is shown to be smaller than an opto-isolator. The discussion includes transformer-reset technique, pulse edge transmission circuit design and forward converter design procedure. The converter start-up transient and control hand-off are explained in detail. Experimental results include operating waveforms, start-up waveforms, and efficiency.

INTRODUCTION

General Overview

The market for DC to DC converters has expanded rapidly with the industry shift to distributed power system architectures. Low voltage logic is the driving force that pushes the market in this direction. Conceptually, power is distributed at moderately high voltages, where conduction losses are low, and have localized low voltage-high current supplies for point-of-use regulation. An additional benefit is realized with distributed power system architectures in modular card based systems; the logic voltage can be easily changed while updating the functional circuitry without changing the main power distribution bus.

A power distribution bus of –48V has been common in telecommunication applications for many years, and +48V has become one of the most general voltages for distributed power architectures. There is a considerable need for an efficient solution to power low voltage logic for operation in these systems, with both small size and high performance. Secondary side control is used in power converters when the output parameters need tighter control or increased functionality over that possible when using primary side control techniques. Secondary side control can be used to implement current sharing among paralleled modules or to enable timed gate drives to a synchronous rectifier.

This design review will cover the design and verification of a 48V isolated converter to supply 15A at 3.3V. Small size and high efficiency are attained through the use of a forward converter power stage with controlled synchronous rectifiers on the output. A new technique is introduced to provide controlled primary side startup with a control hand-off to a secondary referenced controller. This allows the converter to leverage the benefits of a secondary controller without the expense and complexity of an auxiliary supply. The solution is shown to be both very small and reliable.

Secondary Control Bias Techniques

Successful implementation of a secondary side PWM controller requires a means to provide a bias voltage to start and run the control circuitry which is galvanically isolated from the input power source. In the past, several methods have been used to provide bias power to the secondary side of a converter, with most solutions requiring some type of isolating transformer. DC-DC converters such as the present supply usually have a primary to secondary isolation voltage of 1500V, while offline supplies generally must have 3750 V_{rms} isolation.

In some secondary control applications, the controller on the output must interface with the host system to sequence certain outputs or provide critical current or voltage monitoring. This may require a full time secondary bias regardless of whether the output is energized. This could be accomplished as shown below with a line transformer or a separate bias converter to always provide secondary bias power, regardless of the state of the converter. In other systems the requirements for secondary side control are only required when the output is operational. A solution is presented in this design review for power supplies that do not require the elegance of an independent bias supply, yet they merit secondary side control.

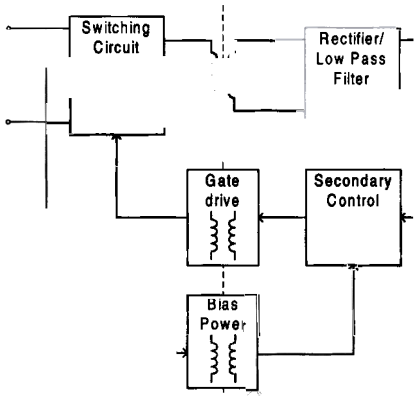

Figure 1. Conventional secondary side bias configuration.

In the simplest case when an AC input voltage is present a line-frequency transformer is used to isolate and step-down the line voltage to feed one or more secondary rectifiers. This method is tried and reliable but requires low frequency magnetics and is not an option with DC input converters. The cost and size of the bulky magnetic unit with the large number of turns required is a major downfall of this solution. A post regulator is generally needed when the line variations are large, adding to the size of the converter.

A housekeeping bias supply might be used to supply one or more bias voltages on either side of the isolation boundary with AC or DC input. This has usually been limited to higher power or high-performance supplies because the housekeeping supply is usually a complete flyback power supply operating at high frequency. Regulation of the secondary bias voltage can be accomplished by sensing a bias winding on the primary side of the power supply, so no additional isolated feedback path is needed. This solution can be reliable and efficient but is complex, expensive, and the space requirements may be a serious concern in low to medium power converters.

Another method to generate a startup bias involves a relaxation circuit on the primary side, which provides pulses through a small transformer to get the secondary bias up to acceptable levels. This technique uses a diac semiconductor device that changes from a blocking state to a conducting state when its voltage is exceeded. The change in conducting state applies a voltage across the pulse transformer primary, sending a packet of energy to the secondary. After enough energy is transferred to start the circuit a bootstrap winding provides the bias for continuous operation. The small pulse transformer and low component count required make this solution attractive, but the selection of available diac voltages can be small, and suppliers are limited for the switching device.

In each of the three previous circuits the secondary controller still needs a means to command the primary referenced switching transistor duty cycle. This is often accomplished with a high frequency gate drive transformer, bringing the total requirement to three transformers to implement secondary side control. In addition, a secondary controller has no direct means to provide over current protection for the power switch device on the primary side. Some designs add a fourth transformer to allow sensing of the primary current.

A Unique Startup Solution

Ideally, a primary startup circuit for a secondary side controller would add a minimal number of low cost components to accomplish the task. The solution should provide a means to start up the primary referenced power switching circuit while maintaining the output within acceptable bounds during the startup transient. The circuit should also be able to handle fault conditions in such a manner to protect the power stage and recover if desired. After consideration of the existing means of startup a unique solution is proposed.

The block diagram of the solution proposed in this review is presented in Figure 2. A primary referenced control IC, the UCC3960, starts up offline with a free-running oscillator and delivers power to the secondary output and bias windings through the main power transformer. The secondary bias is configured to peak charge through the bias winding to quickly bring the secondary controller alive so that the secondary controller can feed back differentiated pulses to the primary through a small pulse transformer. Once this occurs, the UCC3960 assumes the duty ratio and slightly higher switching frequency of the secondary controller, which monitors the rest of the startup transient. This technique results in a controllable startup sequence with a minimal number of added parts.

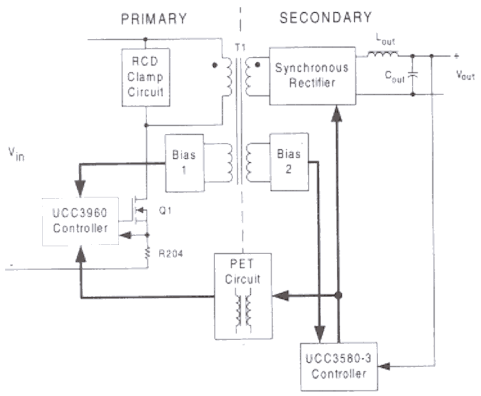

Figure 2. Proposed startup configuration.

Implementation of this converter requires only two transformers, the main power transformer and the small transformer in the Pulse Edge Transmission (PET) circuit. The PET circuit consists of a pulse edge transformer along with a few low-level parts. The secondary controller can use most any Pulse Width Modulation (PWM) based regulator IC, that may include the basic fault protections, with no special communication protocol needed. The secondary controller is selected to provide the secondary control features needed to meet particular design requirements, and be capable of driving the light load of the PET circuit. In the present example the UCC3580-3 was chosen for its ability to directly drive the synchronous rectifier MOSFETs while supplying pulse information through the PET to drive the primary side switch. This is accomplished by driving both the forward MOSFET and the PET circuits from the OUT1 drive signal.

The transformer in the PET circuit can be wound with triple-insulated wire to meet stringent isolation requirements, thus eliminating the need for optocouplers, which introduce complicating factors into control loop design. These factors include concerns with absolute gain value, driving current, temperature effects, aging, and bandwidth. In contrast, the PET circuit transfer function is fixed by the turns ratio. An additional benefit of the PET circuit is that the transformer is much smaller than conventional gate drive transformers. The size advantage is possible because the transformer uses gate pulse edges instead of full width gate pulses.

Overview of Power Topology

The flyback and forward converters are the prime application candidates in the power range from tens of Watts to a hundred Watts. The rated output current of 15A is excessive for the flyback topology because it exerts a severe penalty in the output rectifiers due to the form factor of the current wave shape. Thus, for this single output, high current converter, the single ended forward is deemed the best candidate for an efficient, low-cost design.

A forward converter can be implemented with reset of the power transformer performed in various ways. These include a reset winding, RCD snubber, active clamp, and resonant reset methods. Tradeoffs include semiconductor voltage stress, transformer or control complexity, and efficiency considerations. For the 36V-72V range, an RCD snubber is found to be an acceptable solution, and the snubber power dissipation versus duty cycle is considered.

The advent of ultra low $R_{ds(on)}$ MOSFETs has made synchronous rectification an attractive alternative to passive Schottky rectification. Recent literature indicates that below 40A, synchronous rectifiers have less conduction loss than Schottky diodes [1]. In practice, body diode and gate drive losses narrow the margin in high frequency switching converters. Yet, a careful comparison between synchronous rectification and Schottky diode rectification is merited at this output current level. In this design, we find the use of synchronous-driven MOSFET rectifiers to be more efficient than using comparable Schottky diodes.

A power converter with extensive secondary control features is a candidate for an output ground referenced PWM control circuit. These desirable features include tightly coupled analog control loops, current sharing applications and convenient host system interface.

In this particular case the same error amplifier and control circuit can drive both the synchronous rectifier MOSFETs and also send pulses back to drive the switch in the single ended forward converter. A dedicated primary referenced IC is used to start the supply and then follow the secondary control. An independent bias supply is not needed, merely the usual bias windings on the power transformer.

II. DESIGN PROCEDURE

Detailed Specifications

The design will proceed by selecting components in order that the final design meets the desired detailed specifications listed in Table 1. Most of the specifications are typical for a converter that is intended for a digital logic load. The isolation specification necessitates opto-isolators or magnetic coupling for communication between the primary and secondary. As will be shown in the design, the magnetic coupling that is used in this implementation is competitive with an optical coupler implementation.

Input DC Voltage	*36V to 72V, 48V nom.*
Output DC Voltage	*3.3V ± 5%*
MAX Output Current	*15A*
MIN Output Current	*1.5A*
Output Power	*50W*
Efficiency	*≥ 80%*
Isolation	*1500V*
Output Ripple	*50mVp-p*
Power-up Overshoot	*10% Vout*

Table 1. A list of specifications for this converter.

Throughout the design process, reference designators will be used that are consistent with the final schematics shown in Figure 24 and Figure 25, unless otherwise noted.

Forward Converter Fundamentals

This converter is fundamentally a single-ended forward converter. The power components in the core converter consist of a power transformer, power switch, rectifiers, inductor, reset circuit and output capacitor. The design of the forward converter will progress in the order below. The first eight items are common to most any single-ended forward converter design. Items 9, 10, 11 and 12 are specialized concerns for this implementation.

1. *Switching frequency*
2. *Duty ratio range and clamp fundamentals*
3. *Transformer design*
4. *Output filter components*

5. *Clamp and reset circuit details*
6. *Primary switch transistor*

Secondary modulator

8. *Steady state control dynamics*
9. *Synchronous rectifiers*
10. *Primary startup circuit*
11. *Pulse edge transmission circuit*
12. *Control hand-off*

Switching Frequency

The switching frequency is chosen to be 200kHz. Although the selection might seem arbitrary, it was actually performed by considering switching loss estimates and core loss estimates for a 50W base line design that operates with a maximum of 46% duty ratio. Intuitively, switching loss at this power level could be easily dissipated by convection with stamped aluminum heat sinks if the converter operates at 200kHz or less. Transformer losses were estimated for a variety of cores and materials operating at 100kHz and 200kHz. We found several low profile core shapes made of materials that would operate in our base line converter with less than 0.5W loss at 200kHz.

Duty Ratio and Clamp Fundamentals

The duty ratio was initially chosen for a forward converter with a reset winding. As the design progressed, we changed the reset device to a Resistor-Capacitor-Diode (RCD) clamp circuit. Comparatively, the RCD clamp offers lower switch stress voltage over a wide-ranging input voltage [2]. Furthermore, the RCD clamp circuit limits the turn-OFF voltage spike applied to the primary transistor. Although this clamp circuit permits operation above 50% duty ratio, we found that the losses in the clamp resistor are lower with lower ratios. Thus, we selected the maximum steady-state duty ratio to be 42% in order to allow an additional 8% duty ratio margin for control variations at low line operation, yet take advantage of reduced RCD clamp losses.

Refer to Figure 3 for the details of the RCD clamp circuit. This circuit functions as a buck-boost converter whose inductance is L_m, switch transistor is Q1, rectifier is D_{cl}, output capacitor is C_{cl} and load is R_{cl}. Furthermore, the energy in the magnetizing inductance L_m is completely depleted before the end of each switching cycle, in a Discontinuous Current Mode (DCM) of operation. Thus, the magnetizing inductance, L_m, is energized during the ON-state of the switch transistor. Diode D_{cl} is reversed biased during this interval and C_{cl} is discharging through R_{cl}. The secondary (output) circuitry is effectively disconnected from T1 by the synchronous rectifier after the main switch turns OFF, preventing the magnetizing energy from going to the load. The energy stored in the magnetizing inductance of the transformer flows through diode D_{cl} to the clamp capacitor C_{cl}, which maintains a relatively constant voltage over a switching cycle.

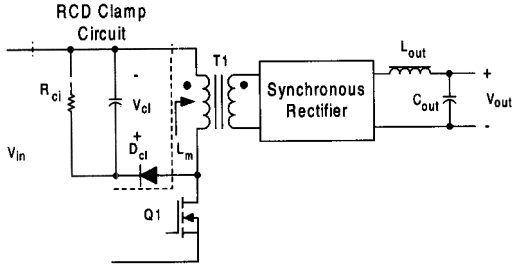

Figure 3. Details of an RCD clamp circuit for resetting a forward converter transformer.

The voltage across C_{cl} can be determined by considering it to be an output voltage of a buck-boost converter that is charged when the main switch turns OFF. Using the model of a classical buck-boost converter operating in DCM, we find the clamp voltage, given in (1).

$$V_{cl} = V_{in} D \sqrt{\frac{R_{cl}}{2 L_m f_s}}, \qquad (1)$$

where D is the duty cycle of the main switch and f_s is the switching frequency. In the usual case, the rest of the circuit determines the magnetizing inductance, switching frequency, and duty ratio. Thus, the clamp voltage is set by selecting R_{cl}.

The power dissipated in the clamp resistor R_{cl} is simply the square of the clamp voltage divided by the value of the clamp resistor. Using (1), we see that the clamp resistor power is proportional to the square of the duty ratio.

$$P_{cl} = \frac{V_{in}^2 D^2}{2 L_m f_s} \qquad (2)$$

Notice that clamp power, P_{cl} in (2), varies proportionally to the square of the duty ratio. If the transformer were redesigned to operate at twice the duty ratio, the possible increase in magnetizing inductance would not significantly affect the clamp power in comparison to the 400% factor that is imposed by the duty ratio increase. We verified this fact by comparing a 13:3 turns ratio design with a 14:2 ratio design. The clamp power loss was 1.46W compared to 3.80W. Clearly, lower duty ratios will afford higher efficiencies when using an RCD clamp. Thus, we chose to keep the maximum duty cycle at 0.42.

Transformer Design

The transformer design uses the Area Product Method that is described in [3]. This produced a design that was found to be core loss limited, as would be expected at 200kHz. The actual core selected is a Siemens-Matsushita EFD 30/15/9 made of N87 material [4]. The effective core area is 0.69cm^2 and the window area is 0.523cm^2. The area-product of the selected core is about 2.5 times more area-product than the method in [3] recommended. We selected the additional margin with the intention of allowing additional losses due to proximity effects in a multi-layer foil winding that is required for carrying the large secondary currents.

The chosen core, operating frequency, and flux density swing place a minimum limit on the number of primary turns the transformer can have to in order to support the normal volt-seconds. We allocated 1% of the converter input power to to be lost in the transformer (0.6W). Assuming that half of the loss is in the core and half is in the windings, the allowable core loss is 0.3W. The volume of the core is 4.69×10^{-6}m^3. The allowable core loss per unit core volume is then 64kW/m^3. We find from the manufacturer's graph of Relative Core Losses versus frequency that the peak flux density is 0.05T for bipolar core excitation. The usable flux density swing is then twice that value or ΔB=0.10T. Using the maximum duty cycle, we calculate the minimum primary turns from [3]:

$$\begin{aligned} N_1 &\geq \frac{V_{in,min} \cdot t_{on,max}}{\Delta B \cdot A_e} \cdot 10^4 \\ &= \frac{V_{in,min} \cdot D_{max}}{\Delta B \cdot A_e \cdot f_s} \cdot 10^4 \\ &= \frac{36 \cdot 0.42}{0.10 \cdot 0.69 \cdot 200000} \cdot 10^4 = 11 \text{ turns} \end{aligned} \qquad (3)$$

These results complete the selection of the transformer core and drive level, and specify the minimum primary turns to prevent core saturation. The specific winding configuration will be determined in the following sections that provide details on the interaction of the turns ratio, maximum allowed duty cycle, and the transformer reset method chosen.

In the ideal forward converter designed to operate over a range of input voltage, the duty cycle varies inversely to the turns ratio as in (4). This formula shows the trade-off between duty cycle and turns ratio, which can be used to move voltage and current stresses from the primary to the secondary of the transformer. In this design the maximum steady state duty cycle is 0.42 at V_{in}=36V.

$$V_{out} = D \frac{N_s}{N_p} V_{in} \qquad (4)$$

We can now define the actual turns ratio for this transformer by accounting for the losses in the power semiconductors, output choke and traces. Here, we allowed 10% additional output voltage drop in order to compensate for the losses. In order to solve for the turns ratio, we can substitute into (4):

$$n = \frac{N_p}{N_s} = \frac{V_{in,min} \cdot D_{max}}{V_{out}(1+0.1)} = \frac{36V \cdot 0.42}{3.63V} \approx 4.2 \quad (5)$$

This allows us to find the secondary turns as the closest integer to (11/4.2), which is 3 turns. The primary turns are now $N_p=nN_s=12.6$; this must be rounded up to 13 turns. The final turns ratio is now $N_p/N_s=13/3=4.33$. We can also calculate the primary magnetizing inductance as:

$$L_m = \frac{\mu_0 \mu_r A_e N_p^2}{} = \frac{(4\pi \cdot 10^{-7})1610(6.9 \cdot 10^{-5})(13t)^2}{} H, \quad (6)$$

$$347\mu H$$

where μ_0 is the permeablility of free space; μ_r, A_e, and l_e are from the data sheet for the EFD 30/15/9 core.

The copper required for the primary and secondary windings is picked using the worst case RMS currents for the respective windings, using a factor of approximately 350A/cm^2. For the primary, the cross sectional area should be approximately 0.007cm^2 of copper; 0.38cm x 0.018cm foil is used. The primary is split and wound in two sections with the secondary sandwiched in between the two sections. The inner primary winding is comprised of 7 turns wound in two layers, and the outer section is made up of 6 turns wound in two layers. The secondary consists of three layers of foil 1.65cm x 0.018cm, between the two primary sections. The primary bias winding was wound with 10 turns of 30AWG on the outermost layer. The secondary bias winding was wound with 5 turns of 30 AWG wire on the layer under the primary winding. The details of the bias windings will be discussed in the section on primary to secondary control hand-off.

In the final design, the transformer had an average temperature rise of 8.4°C at low line. In retrospect, this transformer was perhaps too conservative, but further optimization was left for a future exercise.

Output Filter Components

Consider the selection of the output filter components. In a forward converter, the minimum output is typically ten percent of the full load current. The peak to peak ripple current in the output inductor is then twenty percent of the maximum load current, or (0.2)15A = 3A while maintaining CCM. The freewheeling rectifier voltage, V_{rect}, is estimated to be 0.15V at 15A. With n = 4.33 the maximum off time is (1-D)T_s = (1-0.22)5μs = 3.9μs. At high line the inductor value must be at least:

$$L_{out} = \frac{(V_0 + V_{rect}) \cdot t_{off,max}}{\Delta I_{L,out}} = \frac{(3.3V + 0.15V) \cdot 3.9\mu s}{3A} = 4.5\mu H \quad (7)$$

We chose a ferrite core for L_{out} because the core losses would be too high for a low-cost powdered iron core at our operating frequency of 200kHz. Reference [5] gives core selection guidelines for power inductors similar to those used for the transformer, using the area product method. Using these guidelines we selected Siemens-Matsushita EFD 30/15/9 core, made of N87 material, wound with 5 turns of 12AWG on one layer, with a gap of 0.25mm between core halves.

The filter capacitance is chosen to limit the output ripple voltage to acceptable levels and also must be rated to carry the AC component of the output ripple current of the inductor. The minimum capacitor value is calculated to meet the ripple voltage specification derated by 33%. The method that we used [6] is based on the

relationship between the change in capacitor voltage and the charge that is delivered to the output capacitor each switching cycle.

$$C_{out} = \frac{\Delta I_{L,out} T_s}{8\Delta V_{out}} = \frac{3A \cdot 5\mu s}{8 \cdot 33mV} = 56\mu F \qquad (8)$$

Capacitor C_{out} is implemented in the actual converter as the parallel combination of C204 and C205. The capacitors chosen are two 47µF, 6.3V Panasonic CD Series Specialty Polymer Electrolytic Chip Capacitors, selected for their low impedance at high frequencies. Using these capacitors the ripple voltage at full load was found to be less than $30mV_{pk\text{-}pk}$ as shown in Figure 4, and the characteristics are very stable over a wide range of temperatures.

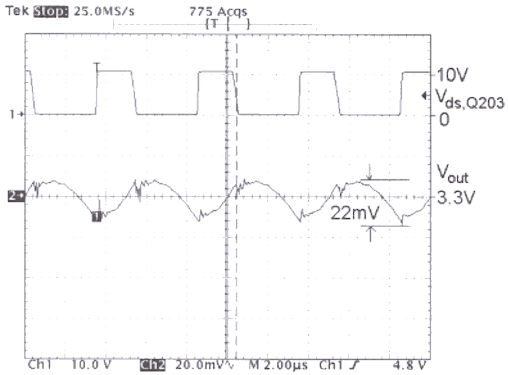

Figure 4. Switching ripple on the 3.3V output.

Clamp and Reset Details

Now that the magnetizing inductance and output filter components are known we can select the components in the clamp and reset circuit. Recall the equations that describe the steady state voltage, (1), and power, (2) for the clamp circuit. Notably missing in the clamp circuit power equation, (2) is the clamp load resistance, R_{cl}. In other words, the clamp circuit operates as a constant power source, regardless of the value of R_{cl}. This phenomenon is known to occur for buck-boost and flyback converters that operate in DCM [7].

Assume for the moment that capacitor C_{cl} is large enough so that the ripple in the clamp voltage is insignificant. What is the acceptable range for the clamp resistor R_{cl}? There are two criteria for selecting the clamp resistor; first, R_{cl} must have sufficiently large resistance in order to allow the core to reset during the smallest steady state OFF time of Q1 and second, R_{cl} must have the power capacity that is described in (2). In other words, R_{cl} must have sufficient resistance in order to maintain DCM operation of the magnetizing inductance. The critical value of resistance that will satisfy the first requirement is found using the same method as with a buck-boost converter operating in DCM [8]. Equation (9) describes the minimum required critical resistance value.

$$R_{cl} \geq \frac{2 L_m f_s}{(1 - D_{max})^2} = 413 \quad \Omega \qquad (9)$$

We selected the clamp resistor value to be R_{cl} = 560Ω to insure that the magnetizing current is discontinuous. Increasing the value of R_{cl} above this value increases the voltage stress on the main transistor. The clamp voltage and clamp power are calculated to be:

$$V_{cl} = V_{in} D \sqrt{\frac{R_{cl}}{2 L_m f_s}}$$

$$= 36 \cdot 0.42 \sqrt{\frac{560}{2 \cdot 347 \cdot 10^{-6} \cdot 200 \cdot 10^3}} \qquad (10)$$

$$= 30.4 \quad V$$

$$P_{cl} = \frac{V_{in}^2 D^2}{2 L_m f_s}$$

$$= \frac{(36)^2 (0.42)^2}{2 \cdot 347 \cdot 10^{-6} \cdot 200 \cdot 10^3} = 1.65 \text{ W} \qquad (1$$

Use a 560Ω, 3W wire wound resistor for R_{cl}.

The clamp capacitor needs to be large enough to sustain DC but small enough to permit its voltage to change as fast as the natural response of the converter output voltage in order to prevent transformer core saturation. The converter output has the dynamics of an LRC circuit where the

clamp circuit has the dynamics of an RC circuit. The clamp capacitor should be selected so that the clamp circuit has a higher corner frequency than the corner frequency of the converter. The corner frequency of the converter will be shown in the controls design section to be $(L_{out}C_{out})^{-\frac{1}{2}}$.

It can be shown that the clamp capacitor affects the corner frequency of the DCM buck-boost clamp circuit by the following relationship [8]:

$$C_{cl} = \frac{2}{\omega_{cl} R_{cl}} \qquad (12)$$

Substituting the clamp resistor value and the radian corner frequency of the converter into the relationship for the clamp capacitor, we get the maximum size for this capacitor.

$$C_{cl} \le \frac{2\sqrt{L_{out}C_{out}}}{R_{cl}} = \frac{2\sqrt{4.5\cdot 10^{-6}\cdot 94\cdot 10^{-6}}}{560\Omega} = 0.073\mu F \qquad (13)$$

Actual selected value: $C_{cl} = 0.068\mu F$

The clamp voltage was measured at $26V_{dc}$ and the ripple was 2V, peak to peak. The circuit did not show any evidence of transformer saturation during transients.

Primary Switch Transistor

Turning now to the main transistor selection, the key considerations are RMS switch current capacity and peak switch voltage stress. RMS switch current capacity translates into $R_{DS(on)}$ specifications for MOSFETs. The peak switch voltage stress is the line voltage plus the clamp voltage plus a turn-OFF voltage spike, V_{spike}. The voltage spike is due to the forward recovery of the clamp diode and stray inductance in the clamp circuit, and was measured as 15V in the actual circuit. The clamp voltage was calculated earlier in (10).

Notice that the clamp voltage does not vary significantly with line voltage. The RMS switch current can be simplified because the output inductor ripple effects are negligible in this design. The two design equations and their values are given below.

$$V_{Q1} = V_{in,max} + V_{in}D\sqrt{\frac{R_{cl}}{2L_m f_s}} + V_{spike} = 72V + 30.4V + 15V = 117.4V$$

$$I_{Q1,RMS} \cong \left(I_{out}\frac{N_2}{N_1} + \frac{V_{out}}{2\cdot L_m}\cdot\frac{N_1}{N_2}\cdot T_s\right)\sqrt{D_{max}} = \left(15\cdot\frac{3}{13} + \frac{3.3V}{2\cdot 347\mu H}\cdot\frac{13}{3}\cdot 5\mu s\right)\sqrt{0.42} = 2.31Amps$$

An IRF640 MOSFET, with a voltage rating of 200V, is selected for this application because it can provide the required performance while being cost-effective. In order to verify the performance of the device in our application, we must estimate the conduction losses at the operating temperature of the die. The drain-source resistance at 100°C is given by:

$$R_{DS(on)} = (0.18\ \Omega)\cdot(1.65) = 0.3\ \Omega$$

The conduction loss is then calculated at nominal line to be 1.6W. The device is in a TO-220 package and it has a junction to ambient thermal resistance of $R_{\theta JA}$=62°C/W. The MOSFET will require a heatsink, yet there is sufficient margin for switching losses while relying on convection cooling.

Secondary Modulator

We will now turn our attention to the modulator to define the steady state control elements for this converter. The modulator has a feature that limits flux in the power transformer. The components R_r and C_r that set the flux limit also shape the ramp that defines the feed-forward and feedback gains of the modulator. We must account for these features in the steady-state controller design.

The secondary side controller is based on a UCC3580 Single Ended Active Clamp/Reset PWM integrated circuit [9]. In order to keep the MOSFET gate drive losses as low as possible we chose the low voltage option of the secondary controller (UCC3580-3). The minimum secondary bias in order to guarantee start-up for this option is 10.5V. The peak detector configuration of the secondary bias supply requires a linear post regulator because of the 2:1 input line variations.

The Pulse Width Modulator (PWM) on the secondary side is a sawtooth modulator with a leading edge ramp. Refer to Figure 24 and Figure 25 for reference designators. Resistor R_r, capacitor C_r and the reflected line voltage, V_{peak2} set the slope of the leading edge ramp. The reflected line voltage, V_{peak2}, is the feed forward control input to the modulator. The UCC3580 has an internal flux comparator that terminates the OUT1=ON portion of a switch cycle if the ramp voltage exceeds 3.3V. Thus, the "Volt-seconds" that can be applied to the power transformer, T1, is clamped. The peak Volt-seconds, λ, that we wish to apply to the transformer and reflected to the bias 2 winding is given by:

$$\lambda_{B2,peak} = \frac{N_{B2}}{N_1} \cdot \frac{V_{in,min} D_{peak}}{f_s} = \frac{5}{13} \frac{36 \cdot 0.5}{200{,}000} = 0.346 \cdot 10^{-6}\ \text{Volt} - \text{sec} \quad (17)$$

The selection of R_r and C_r are given by the data sheet [9] as:

$$R_r C_r = \frac{\lambda_{B2,peak}}{3.3\ \text{Volts}} \quad (18)$$

Arbitrarily choose C_r to be 1000pF, which leads to $R_r = 10.5k\Omega$. Be sure to use a 5% tolerance C_r in this application in order to insure that the range is met.

The control parameters are selected here in order to provide stable operation. Figure 5 shows the linearized small signal model for the modulator, converter and controller.

The values of R_r and C_r are also gain parameters for the secondary modulator. The large signal model that describes the modulator employed by the UCC3580 is given as:

$$D(t) = R_r C_r f_s \cdot \frac{N_1}{N_{B2}} \frac{V_c(t)}{V_{in}(t)} \quad (19)$$

where $V_c(t)$ is the output voltage of the error amplifier.

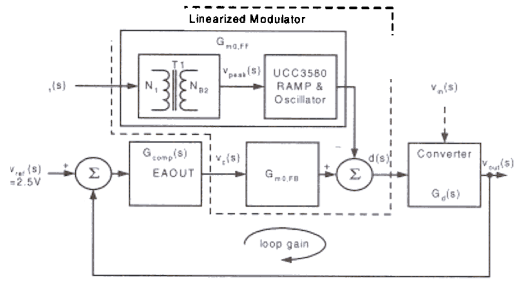

Figure 5. Linearized small signal block diagram of the power supply.

Perturbation analysis of (19) and the substitution of the DC modulator gain results in the linearized small signal modulator model:

$$d(t) \cong \left(\frac{N_1}{N_2} \cdot \frac{1}{V_{in,0}} \right) v_c(t) - \left(\frac{N_1}{N_2} \cdot \frac{V_{out,0}}{V_{in,0}^2} \right) \cdot v_{in}(t) \quad (20)$$

$$= G_{m0,FB} v_c(t) - G_{m0,FF} v_{in}(t)$$

The $v_c(t)$ term represents the gain of duty ratio variations due to error amplifier output variations; the $v_{in}(t)$ term represents the gain of duty ratio variations due to line variations. The "0" subscripts denote the steady state values at the operating point of the converter. In the purest sense, the units of d(t) are dimensionless.

However, we will resort to using the units "duties" for d(t) when clarity is necessary.

Steady State Control Dynamics

We are now ready to design the control loop for this converter. The control loop is a simple voltage mode controller. A spreadsheet is recommended to calculate the dynamic features and parameters over several line and load conditions. For the loop design, assume that the components are ideal and the load is resistive. Thus, the load is assumed to be the only source of damping in the system.

The outline of the control system design procedure follows the design of a classical Proportional plus Integration plus Derivative (PID) controller using magnitude versus frequency and phase versus frequency response plots. A suitable crossover frequency is chosen at a frequency where the converter and modulator have consistent phase response over the full load and line range. Then, the integration gain of the controller is selected to improve steady state and low frequency dynamics. Next, the derivative gain of the controller is selected to stabilize the system in the frequency bands near the crossover frequency. Finally, the proportional gain is adjusted to set the crossover frequency at the desired frequency.

This converter has consistent phase response at either frequencies much lower than the resonance of the output filter, or frequencies much higher than the resonance of the output filter. In order to have reasonably sized bias capacitors, the secondary side must respond quickly to start-up. Thus, the control loop needs to respond to disturbances that are of higher frequencies than the corner frequency that is set by the output inductance and output capacitance. This control loop design will neglect parasitic effects such as output capacitor ESR.

For normal forward converters, the worst-case phase problems occur at light loads where the converter is barely in Continuous Current Mode (CCM). In this converter, the CCM theoretically extends to no-load due to the controlled synchronous rectifier, which will allow the output ripple current to go negative. However, our specifications spare us from considering that condition with a minimum load of 10% rated load.

The small signal duty ratio to output transfer function was found by averaging the dynamic responses during each interval and linearizing the result. Taking the Laplace transform of the linearized differential equations, the duty control to output transfer function of the converter is then solved by substitution. The resulting transfer function is:

$$\frac{v_{out}(s)}{d(s)} = G_d(s) = \frac{G_{d0}}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \qquad (21)$$

where:

$$G_{d0} = \frac{V_{out}}{D_0} = 7.92 \rightarrow 15.8 \text{ Volts/duty}$$

$$\omega_0 = \frac{1}{\sqrt{L_{out} C_{out}}} = 48.6 \text{ k rad/sec} = 7.74 \text{ KHz} \qquad (22)$$

$$Q = R_{load} \sqrt{\frac{C_{out}}{L_{out}}} = 0.995 \rightarrow 9.95$$

The loop gain is the product of $G_{m0,FB} G_d(s) G_{comp}(s)$, where $G_{comp}(s)$ is the compensator response. For a forward converter, the feed-forward compensator has the additional benefit of making the product of the modulator and converter gains invariant over line variations. Hence, the controller design need only consider load variations.

Begin the control loop design by considering the loop gain and phase under the assumption that the compensator gain, $G_{comp}(s)$, is unity (no compensation). The loop gain and phase responses without compensation are shown in Figure 6.

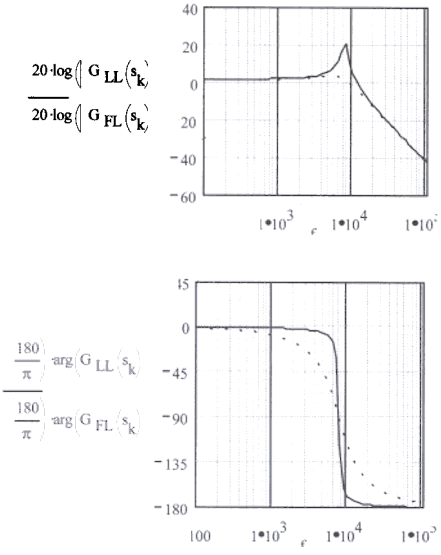

Figure 6. Magnitude and phase frequency response plots of the uncompensated converter over Light-Load, LL, and Full-Load, FL conditions.

We selected the crossover frequency of the loop to be 22kHz because the phase of the duty ratio control to output transfer function is consistent, yet it is above the resonant frequency of the output filter and it is sufficiently below the switching frequency. In order to avoid overshoot, we targeted the controller to have a minimum phase margin of 52°, which occurs at light load. The maximum phase margin will be 71°, occurring at full load. The controller gain must be at least 9 at 120Hz in order to reject the 10% line ripple from V_{in}. An integrator provides the necessary gain at 120Hz. In order to maintain the crossover at the selected frequency of 22KHz, the integration is cancelled by a zero at 528Hz. The controller that we used to obtain the desired dynamics is shown in Figure 7.

Examination of Figure 7 reveals a point concerning the feedback gain. The internal reference on the UCC3580 is used as the control reference for the power supply. However, the sensed output voltage must be attenuated from 3.3V to 2.5V using a resistive divider. Notice that the gain through the resistive divider R401 and R404 is effectively cancelled in the compensator topology, and it does not effect the loop gain.

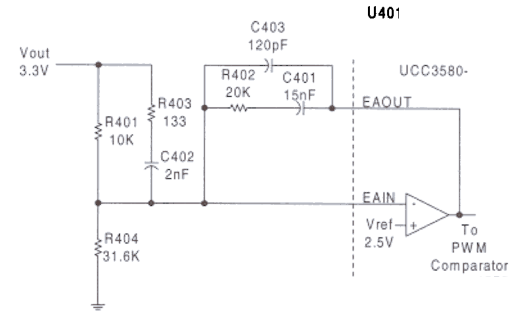

Figure 7. Controller for the forward converter

The frequency responses of the compensator, loop gain at light load and loop gain at full load are shown in Figure 8. The minimum phase margin is 51° at light load and 71° at full load. Although the minimum phase margin is 51° instead of 52°, it provides sufficient damping in the final system. The gain at 120Hz is 11 due to the standard value selection. Crossover occurs at 22kHz, as planned.

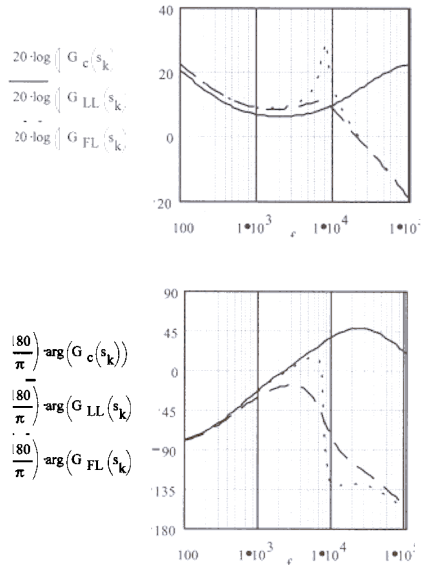

Figure 8. Magnitude and phase frequency response plots of the controller, G_c, and the closed loop gain over light load (G_{LL}) and full load (G_{FL}) conditions.

At this point, the Forward Converter portion of this design is complete. The turns ratio of the main transformer was selected for low-loss rectification. The controller design is specifically arranged for secondary side control by using the internal reference. The control response is designed to be fast, in order to keep the start-up transient brief.

Synchronous Rectifiers

The output current of this converter is in a range where a comparison should be made between passive Schottky rectification and synchronous rectification. The result should reveal superior performance with synchronous rectification. A suitable Schottky rectifier will be selected and compared in this converter to the synchronous rectifier version in order to verify the design direction.

In the present application the most suitable Schottky rectifiers were determined to be the 32CTQ030, a dual TO-220 pair with common cathode, manufactured by International Rectifier [10]. The forward diode will use the parallel combination of both diodes in the package, as will the freewheel diode. The parallel combination has a forward drop of approximately 0.35V at 15A and 100°C, with a resulting power loss of:

$$P_{loss,\,Schottky} = 15A \cdot 0.34V = 5.1\,\text{Watts} \quad (23)$$

The use of synchronous rectifier MOSFETs instead of Schottky diodes can increase efficiency, reduce power system size or yield better thermal management. Several manufacturers produce low voltage MOSFETs with ON resistances on the order of 5mΩ to 10mΩ, with a mixture of specifications at 5V and 10 V. Key parameters with notable variations between devices include the gate threshold voltage range, body diode charge storage, and the dynamic switching behavior. Table 2 shows the key parameters for the device that was selected in for this design [11].

The Siliconix TrenchFET SUP75N05-06 was chosen for the present application for three reasons. First, the device has a low $R_{DS(on)}$ (6mΩ at V_{gs}=10V), at the bias voltage for the secondary control circuit. Second, the device body diode exhibits low stored charge and short reverse recovery times. Third, the minimum gate threshold of 2V provides noise margin and simplifies the requirements of the gate drive circuitry.

Synchronous rectifiers on a transformer-isolated forward converter may be implemented using an externally driven control circuit or by self-driving the MOSFET gates directly from the power transformer windings. In [12], it is shown that the efficiency of Synchronous Rectifier (SR) circuits using an RCD clamp reset circuit is higher when using the control-driven rectifier over the self-driven rectifier. This occurs because the self-driven scheme will turn off the MOSFET and allow the body diode to come into conduction after the transformer reset is completed, conducting the full load current through the MOSFET diode's large forward voltage. In contrast, the control-driven circuit reduces the conduction loss by keeping the SR in a low resistance ON-state throughout the free-wheel interval. A control-driven SR is thus the preferred choice for this application.

Manu.	Part #	Vds	Rds,on Ω max	Vgs	trr, nsec typ,max	Qrr, nC, typ,max	Qgate nC typ,max	Ciss pF typ	Coss pF typ	Crss pF typ	Vgs,th.
Sili.[11]	SUP75N05-06	50	0.006	10	65,120	160,480	85,120	4500	1100	360	2v xx 4v

Table 2. Key parameters to consider for a synchronous rectifier MOSFET.

The MOSFETs in the SR were configured as shown in Figure 9, in order to use the body diodes in the MOSFET body to block current in the reverse biased direction. This configuration also features secondary ground connected sources for both devices permitting direct drive from the control IC. Both MOSFETs in the synchronous rectifier are positioned so that the regular conductive period is in the third quadrant of the device characteristics. The turn-ON transition of both devices in the synchronous rectifier occurs with nearly zero drain voltage.

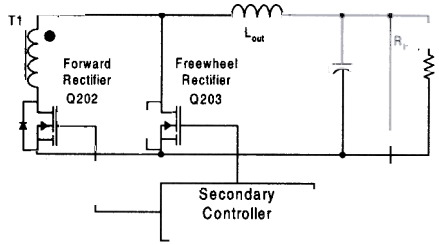

Figure 9. Configuration of MOSFETs in the control driven synchronous rectifier.

Conduction loss in synchronous rectifiers is proportional to the square of the current. In contrast, Schottky rectifier conduction losses are proportional to the current. It follows that Schottky rectifiers will have lower losses than synchronous rectifiers when operating above some current level. A fair comparison must also include the switching, recovery and gate drive losses that are incurred by the synchronous rectifier. Is the operating current of this converter below the efficiency crossover?

In the present design the synchronous rectifier losses can be divided up into $R_{ds(on)}$ conduction losses, gate drive losses, diode recovery losses, and body diode conduction losses. The combined conduction losses of the two SR MOSFETs, operating at 100°C junction temperature are estimated as:

$$P_{cond} = (I_{out}\sqrt{D_{SR}})^2 \cdot R_{DS(on)} \cdot K_{Temp}$$
$$= (15A \cdot 0.979)^2 \cdot (0.0055\ \Omega) \cdot (1.4) \quad (24)$$
$$= 1.66\ \text{Watts}$$

where

$$D_{SR} = \frac{T_s - (Delay1 + Delay2)}{T_s}$$

is the ratio of conduction of both SR MOSFETs and Delay1 and Delay2 are as specified later in this section.

The gate drive power loss is estimated from the device gate charge curve to be 87nC with a gate to source voltage of 10V. This gives the following estimate for the current to charge the gate at a switching frequency of 200kHz:

$$I_{gate} = \frac{dQ}{dt} = \frac{87\ nC}{5\ \mu sec} = 17.4\ mA \quad (25)$$

Since two gates must be driven, 34.8mA must be supplied from our nominal 17.7V pre-regulated bias to give a power loss of (17.7V) · (34.8mA) = 0.62W.

The reverse recovery losses of the body diodes occur after the gate of each MOSFET is turned off and the body diode changes from a conducting state to a non-conducting state. A useful approximation utilizing the charge stored in the diode, Q_{rr}, and the OFF-state voltage of the switch, V_{off} can be expressed as:

$$P_{rr} = Q_{rr} \cdot V_{off} \cdot F_s \quad (26)$$

At 50V input, both devices have a peak applied voltage of approximately 10V in the OFF-state, so the reverse recovery charge translates into a power loss of 0.32W for each device. The total reverse recovery loss is then 0.64W.

The body diode conduction loss occurs during the delay times between OUT1 and OUT2 of the UCC3580. A delay is required between OUT1 and OUT2 transitions in order to prevent excessive currents during commutation. The details of the delay will be discussed later in this section. During the delay, the SR MOSFETs are disabled and the current passes through their respective body diodes, according to natural commutation. Using the delay equation (28), Delay 2 is set for 127ns and Delay 1 is then 87ns. The loss due to body diode conduction for the combined pair of synchronous rectifier diodes is then:

$$P_{body\ diode} = (Delay\,1 + Delay\,2) \cdot f_s \cdot I_{out} \cdot V_{d,body}$$
$$= (127n\,sec + 87n\,sec) \cdot 200 \cdot 10^3 \cdot 15 \cdot 0.65 \qquad (27)$$
$$= 0.42\ Watts$$

The estimated total losses in the synchronous rectification MOSFETs are 3.34W. This is a reduction of 1.69W from the power loss estimate of 5.1W for the Schottky rectifiers. This comparison indicates that the selected MOSFET will show an improvement in this converter's efficiency over rectification using Schottky diodes.

Actual waveforms of the synchronous rectifier MOSFET drains and gates are shown in Figure 10. In the actual circuit, the gate charge time to threshold is also added to the delay time, as seen in Figure 10. However, the additional delay is small and it does not significantly effect the total power loss.

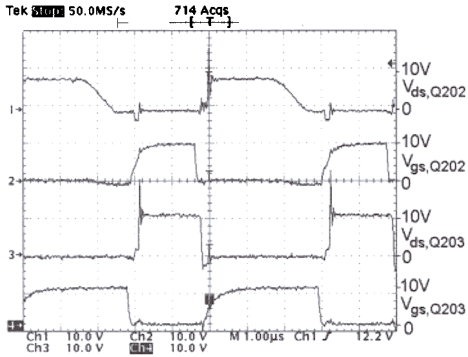

Figure 10. Forward MOSFET V_{ds}, forward MOSFET V_{gs}, freewheel MOSFET V_{ds} and freewheel MOSFET V_{gs} are shown from top to bottom. Notice that these two MOSFETs turn ON with nearly zero volts.

How should the secondary controller drive the SR MOSFETs? Is it possible to drive them directly from the secondary controller, the UCC3580 or are additional drive circuits necessary? Direct drive of the SR MOSFETs from the UCC3580 control IC requires a careful study of IC gate drive capability.

OUT1 of the UCC3580 can source up to 1A and sink up to 0.5A. Using the typical high and low driver saturation voltages, the typical output impedance for OUT1 is 8Ω when high and 4Ω when low. With a secondary bias voltage of 10.5V, a conservative design would specify 12Ω external to the IC to limit the source current to 0.5A. Likewise, 6Ω would be required to limit the sink current to 1A.

OUT2 is able to sink and source 0.3A, and it has an internal impedance of 13Ω. This output requires 36Ω to limit the source and sink current to 0.3A. When these values of resistors are substituted into the breadboard and waveforms examined, the gate waveforms are slow for 200kHz operation, and the high gate drive impedance can lead to shoot-through losses due to dV/dT turn-on. These gate drive waveforms are shown in Figure 11 under bias power only.

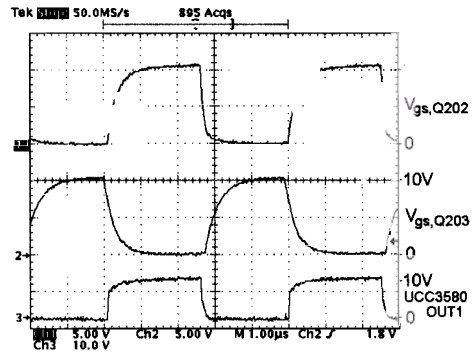

Figure 11. Gate waveforms of the synchronous rectifier.

A drive circuit was added at the gate of the SR MOSFETs to produce a crisper turn-off waveform, as shown in Figure 12. This circuit also holds the gate low during the interval when the drain voltage rises and the drain-gate capacitance is charged, helping prevent undesired turn-on and the resulting shoot-through losses.

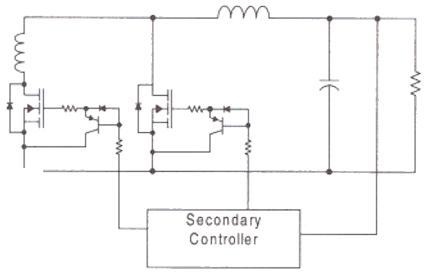

Figure 12. Synchronous rectifier shown with gate turn-OFF drivers.

The gate waveforms of the SR MOSFETs and the primary switch are shown in Figure 13. These waveforms clearly show the quick turn-off of the SR MOSFETs by the circuitry added local to the gate. The disparity between the current sourcing capability of the two outputs is evidenced by the quicker enhancement of the upper device compared to the lower one.

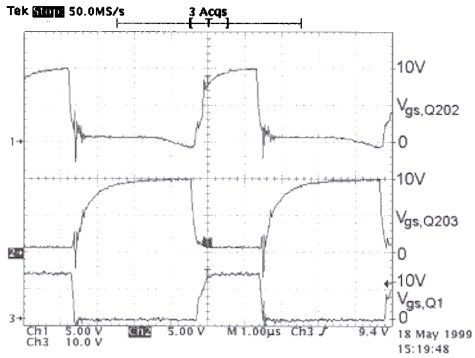

Figure 13. Gate waveforms of the synchronous rectifier with gate turn-OFF drivers.

The adjustable delay feature on the UCC3580 was used to set the delays for optimum efficiency by using the smallest delay possible without introducing a conduction conflict with the primary MOSFET. The potential conduction conflict is a result of the delay that the UCC3960 imposes when translating the OUT1 signal edges into the primary-side gate drive signal. Figure 14 shows that the important delay to consider here is Delay2.

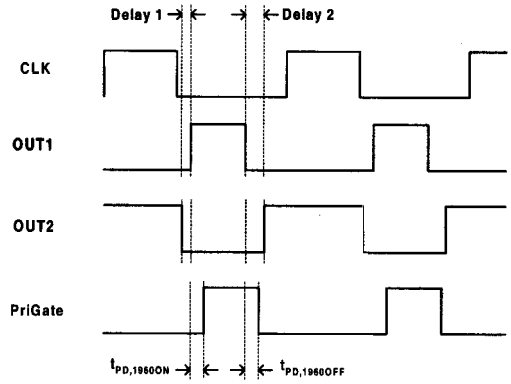

Figure 14. Timing signals of UCC3580 outputs relative to the UCC3960 output. The falling edge of the UCC3960 should occur before the rising edge of OUT2 on the UCC3580.

Delay 2 is set to be larger than the delay of the falling edge of the UCC3960 (125ns) in order to avoid having the primary MOSFET in the ON-state while the freewheeling rectifier (Q203) is conducting. Using the Delay Times curves in the UCC3580 data sheet, an equation for the appropriate value for R405 can be calculated to give the desired delay time.

$$R405 = \frac{Delay\ 2 - 40.4ns}{1.27 \cdot 10^{-12}} = \frac{125ns - 40.4ns}{1.27 \cdot 10^{-12}} = 67\ k\Omega \quad (28)$$

use R405 = 68kΩ, causing Delay 2 to be 127ns and Delay 1 to be 87ns.

How do the power supply efficiencies compare between the synchronous rectifier configuration and the Schottky rectifier configuration? The results here serve as a checkpoint to verify that the power loss estimations are realistic. The comparison between two circuit variations was measured under the same bench conditions with only the rectifier configuration being changed. The efficiency comparison at 50V line is shown in Table 3. The efficiency improvement with the SR circuit is found to be more than 2% over that of the Schottky circuit, and it agrees with earlier power loss estimations.

	V_{in}, V	I_{in}, A	V_{out}, V	I_{out}, A	P_{in}, W	P_{out}, W	eff., η
UCC3580 Direct Drive	50	1.255	3.334	15	62.75	50.01	79.7
Schottky Rectifier	50	1.294	3.326	15	64.7	49.89	77.1

Table 3. Measured efficiency comparison of schottky vs. synchronous rectifier.

Primary Start-up Circuit

Now turn our attention to designing the primary side start-up circuit. Here, the unique features of UCC3960 make it a cost-effective choice for implementing the primary side start-up circuit [13]. A functional diagram of the converter is shown in Figure 15.

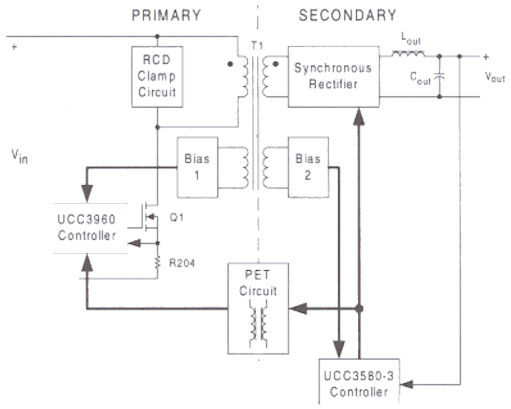

Figure 15. Simplified block diagram of the power supply system that shows the primary and secondary bias supplies.

The UCC3960 performs the initial soft-start ramp function, and then it passes control to the secondary side controller when it detects the first falling edge of a gate pulse from the secondary side controller. Figure 16 describes the events during a typical start up sequence by showing the progression of D(t) versus time. The start up sequence is divided into four distinct control intervals; two control intervals originate from the primary side and two control intervals originate from the secondary side. If an over current fault or a primary bias supply fault occurs at any point during operation, the UCC3960 discontinues operation and awaits a restart.

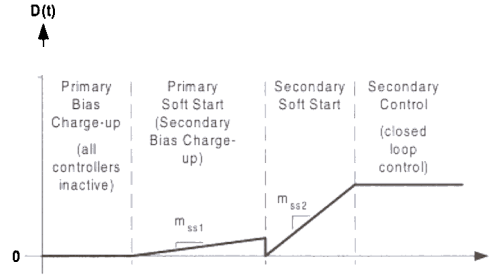

Figure 16. Duty ratio vs. time during normal start-up

At this point, select the primary side components that do not directly impact the control hand-off dynamics. They will be selected in the following order. First, select the primary bias topology and number of primary bias winding turns, N_{B1}, that are required in the power transformer, T1. Next, select the primary start-up charge resistor, R212, and the primary bias inductor, L202. Then, select the primary start-up switching frequency and associated timing resistor, RT. Finally, select the over-current protection components and then the primary gate drive components.

The circuit for transmitting the gate pulse will be described in the Pulse Edge Transmission (PET) circuit section. The primary side soft-start ramp components and the design of both bias supplies will be described in the section on Primary to Secondary Control Hand-off.

The primary bias circuit discussion begins with the bias topology that is needed for this application. We structured the primary bias output to be a forward converter output in order to make it approximately track the main 3.3V output and maintain a reasonably constant bias voltage in spite of large input voltage variations. Hence, the primary bias circuit requires the components that are shown in Figure 17. A startup resistor (R212) is required to initially charge the bias capacitor to the VDD Start Threshold.

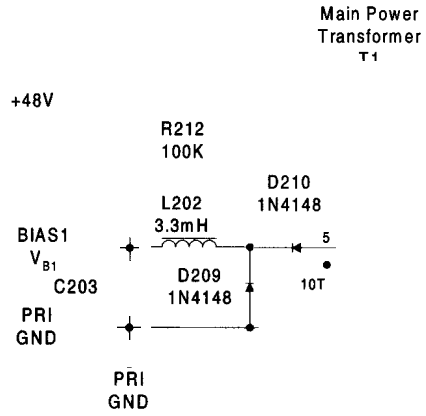

Figure 17. Topology and components chosen for the primary bias supply.

The number of turns for the primary bias winding in power transformer T1 are calculated using the ratio of the converter output voltage to the secondary turns. The UCC3960 can operate with a bias of VDD=11V. The number of turns for the primary bias winding is then:

$$N_{B1} = \frac{VDD}{V_{out}} \cdot N_2 = \frac{11}{3.3} \cdot 3 = 10 \text{ turns} \qquad (29)$$

When line voltage is first applied to the circuit, startup current is supplied from V_{in} to C203 and the UCC3960 through R212. Resistor R212 is picked to allow C203 to charge to the VDD startup threshold of 10V under low-line conditions,

$$R212 = \frac{(V_{in,min} - VDD)}{I_{VDD},Starting} = \frac{(36-10)}{250\mu A} 100k\Omega \qquad (30)$$

Once the UCC3960 starts switching, C203 must be large enough to supply the average primary bias current for the total duration of the start up transient without its voltage falling more than the UVLO Hysteresis voltage of 2V. The total average current requirements of the Bias 1 Supply include the operating current of the UCC3960 (2.3mA) plus the current to drive the IRF640 (estimated as I = (52nC) / (5□s) = 10.4mA). Thus, C203 must supply 12.7mA bias current during the 1.5ms startup transient. We will defer the calculation of the value of C203 to the section on control handoff, when the duration of the start up sequence is better understood. It will suffice to say here, that C203 will be large enough that its voltage will essentially be DC.

As stated earlier, the primary bias output will behave like a forward converter output. It was found in the general design of the forward converter that the smallest duty ratio, 0.2, occurred at high line (V_{in}=72V). In order to maintain the primary bias inductor in Continuous Current Mode (CCM), the value of the primary bias inductor is selected as follows:

$$L202 \geq \frac{V_{B1} \cdot (1-D_{min})}{2\, I_{B1,avg}\, f_s} = \frac{11 \cdot (1-0.2)}{2 \cdot 13mA \cdot 200KHz} = 1.7mH \qquad (31)$$

use : $L202 = 3.3\ mH$

The next higher standard value of 3.3mH was selected to ensure that the bias output current remains continuous to keep the output quasi-regulated. This winding is well regulated with respect to line changes but varies as the load on

the 3.3V winding changes. Prototype testing showed a primary bias voltage change from 13.2V to 11.5V as the 3.3V output goes from full load to 20% load.

A single resistor, RT, sets the primary side start up frequency. The frequency of the free-running primary side oscillator should be selected to be 90% of the secondary side free running oscillator. For our switching frequency of 200kHz, the value of RT is selected as:

$$RT = \frac{90\%}{100\%}\,\frac{8\cdot 10^9}{f_{S,\,secondary}} = \frac{(0.9)\cdot 8\cdot 10^9}{200kHz} = 36\ k\Omega \quad (32)$$

Resistor RT should be 1% tolerance in order to consistently obtain an oscillator frequency that is 90% of the secondary side free running oscillator frequency. Note: The test circuit used RT = 49.9kΩ owing to the use of preliminary silicon for the UCC3960. Consult the most recent UCC3960 data sheet that is available for the correct relation between RT and the switching frequency.

Primary-side power stage over-current protection is incorporated into the UCC3960. The CS input, pin 9, performs a pulse-by-pulse current limiting function with a 1V threshold, and initiates a complete shutdown if the 1.375V level is attained. The current sense resistor R204 is selected to perform the pulse-by-pulse current limit at 120% of full load output, referenced to the primary side:

$$R204 = \frac{1V}{1.2\cdot I_{pri,\,peak}} = \frac{1V}{1.2\cdot 3.8A} = 0.22\ \Omega, \quad (33)$$

where $I_{pri,\,peak} = \frac{N_2}{N_1}\cdot\left(I_{out} + \frac{I_{ripple}}{2}\right)$

$$= \frac{3}{13}\left(15A + \frac{3A}{2}\right)$$

A value of 0.22Ω, ½W is selected. A small R-C filter is inserted between the current signal and the CS input to reduce noise sensitivity, in this case R307 = 499Ω and C305 = 470pF. An internal device discharges the filter capacitor during the off period of the main switch to improve the fidelity of the current sense signal.

The primary gate drive resistor, R202, is selected per the UCC3960 data sheet specifications in order to meet the safe area of operation. A minimum of 4Ω of gate resistance is required for a MOSFET of similar die size to the IRF640. Select R202 = 4.7Ω.

Pulse Edge Transmission Circuit

The UCC3960 receives gate pulse information from the secondary side controller through a pulse edge transmission (PET) circuit. The FB pin uses the rising edge pulses to turn on the primary MOSFET and the falling edge pulse to turn it off. The PET circuit is required to have adequately high damping (which means low Q factor) in order to prevent false triggering associated with excessive overshoot. The circuit and typical waveforms are shown below in Figure18.

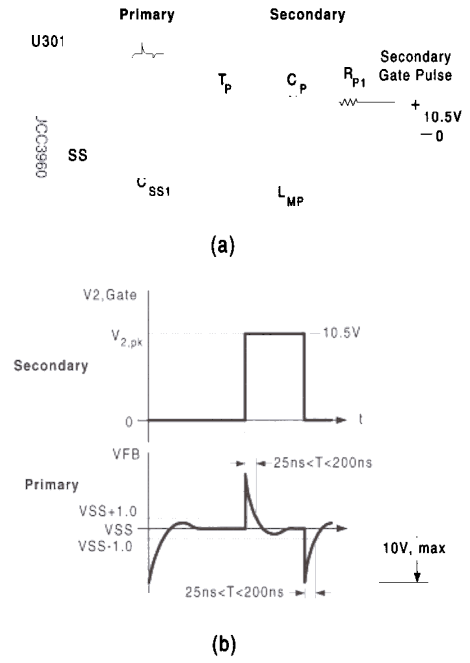

Figure 18. Pulse Edge Transmission (PET) circuit schematic is shown in (a) and typical waveforms are shown in (b).

Transformer T_P provides Secondary to Primary isolation for the PET circuit. A turns ratio of 1:1 is preferred in order to improve the signal to noise ratio that is transmitted across the isolation boundary. The magnetizing inductance of T_1 also controls the width of the FB signal. R_{P1} and R_{P2} attenuate, dampen and limit the current of the signal edges as they pass from the secondary to FB. Attenuation is required in order for VFB to be with in the $10V_{p-p}$ maximum rating. VFB requires sufficient damping (meaning low Q factor) in order to prevent false triggering from overshoot. The peak current in the FB pulse should be in the range of 5mA to 50mA (or $R_{p1}+R_{p2} = 210\Omega$ to $2.1k\Omega$). C_P blocks DC voltage from the transformer and provides a reset voltage for the Pulse Edge Transformer, T_P.

The outline of the PET circuit design for the given secondary gate pulse voltage begins with the selection of the pulse edge width, the Q factor and the transformer. Then the design progresses through selecting specific resistor and capacitor values with a final check on the flux density in the transformer core.

The UCC3960 requires that the pulse edge duration be between 25ns and 200ns, as shown in Figure 18. Select the duration to be 45ns. In order to avoid false triggering, the Q factor must be between 0.1 and 0.28. Select a Q factor of 0.25. The PET circuit must attenuate the secondary gate pulse signal by $10/(2 \cdot V_{2pk})$, in order to limit the AC voltage on the FB pin to $10V_{p-p}$.

Given parameters:

- $V_{2,pk} = 10.5V$
- $\tau_2 = 45ns$
- $Q = 0.25$

This design will target minimum transformer size. The time constant τ_2 will be in the 45ns range. The core material needs to have a relatively consistent permeability up to about 3.5MHz (or $1/(2\pi\tau_2)$. Ferronics J material has a suitable permeability versus frequency curve. The saturation flux density of this material is 0.28 Teslas. Approximating the attenuation to be 50% and considering the ranges of R_1 (peak pulse edge current) and τ_2, the range of L_{MP} is between 2.5µH to 120µH. Select L_{MP} to be around 4µH to 8µH in order to facilitate narrow duty ratios and small physical transformer size. Triple insulated wire is necessary on at least one of the windings in order to meet agency isolation requirements. A triple insulated, 30AWG, 0.022" outside diameter Rubadue Wire (T30A01TXXX-2) will meet the requirements. Expect to use about 3 to 5 turns. Formulating the range of core constants, $160nH/turns^2$ to $890nH/turns^2$, we see that the Ferronics 11-622J core is in this range with a core constant of $337nH/turns^2$. The effective core area is 0.0411 cm^2. Four turns on this core gives an inductance of L_{MP}=5.4µH.

Using an approximation of the time constant τ_2, we can now solve (34) for the resistance of the parallel combination of R_{P1} and R_{P2}:

$$R_{P1} \| R_{P2} \cong \frac{L_{MP}}{\tau_2} \qquad 120\,\Omega \qquad (34)$$

The required attenuation then sets the values of R_{P1} and R_{P2} in (35) and (36). The AC voltage of the FB pin is 10V.

$$R_{P1} = (R_{P1} \| R_{P2}) \left(\frac{2V_{2,pk}}{VFB_{AC,p-p}} \right) \qquad (35)$$

$$= 252\,\Omega$$

Use $R_{P1} = 270\Omega$.

$$R_{P2} = \frac{R_{P1}}{\frac{2V_{2,pk}}{VFB_{AC,p-p}}} \qquad 245\,\Omega \qquad (36)$$

Use $R_{P2} = 240\,\Omega$.

The relationship between Q and the time constants, τ_1 and τ_2, combined with the approximation that the time constant τ_1 is $R_{P1}C_P$ yields the desired capacitor value in (37).

$$C_P = \frac{\tau_2}{R_{P1}(Q)^2} = 2.67\,nF \qquad (37)$$

Use $C_P = 2.7$ nF.

Check to insure that core of the transformer is not saturated. The procedure is to use (38) to calculate the longest time constant, τ_1. Then the applied Volt-seconds is found using (39) and finally, calculate the maximum flux density with (40).

$$\tau_1 = R_{P1}C_P \quad = \quad 0.73\,\mu\text{sec} \tag{38}$$

$$\lambda_{max} \cong V_{2,pk}\frac{1}{\tau_1}L_{MP}C_P = 2.1\times10^{-7}\ \text{V}-\text{sec} \tag{39}$$

$$B_{max} = \frac{\lambda_{max}}{2\cdot n\cdot A_e}\times10^4 = 6.4\times10^{-3}\ \text{Teslas} \tag{40}$$

where λ_{max} is in Volt-sec, n = 4 is the number of primary turns in T_P and A_e = 0.0411 is the effective core area in cm^2.

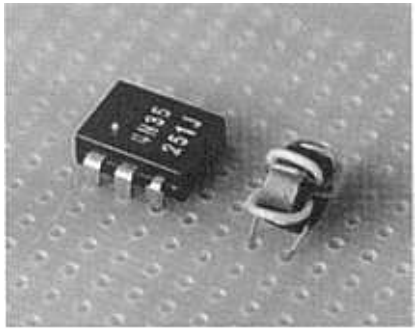

Figure 19. The transformer is shown with an opto-isolator for size comparison.

The selected core can withstand a flux density of 0.28 Teslas, in contrast to the actual 0.0064 Teslas. Although the transformer is considerably over designed from the flux density perspective, it has an outside diameter of less than 6mm. Compare the size of the finished transformer with an opto-isolator, as shown in Figure 19. Notice also that neither the converter duty cycle nor the converter switching frequency has a significant role in the size of the pulse edge transformer. In contrast, a conventional gate pulse transformer design is driven by both duty cycle and switching frequency and it would be at least twice that diameter.

Control Hand-Off

Both primary and secondary bias supplies in addition to both primary and secondary soft start circuits strongly affect the control hand-off dynamics. "Overshoot" specifications are usually the means of quantifying the desired hand-off dynamics requirements. Often, the load for a power supply of this nature will be a digital logic circuit that includes sequential logic. Many logic circuit loads can only tolerate about 10% overshoot during the power up transient. Furthermore, steps must be taken in the design to insure that the control hand-off point occurs at an output voltage that is below potential logic threshold levels in the secondary. The purpose here is to avoid the contamination of sequential logic during the power up transient. Careful selection of bias supply topologies and components yield a power supply that meets these requirements.

Consider the bias topologies. The primary bias topology is selected as a forward output, much like the main output of the power supply. The primary bias will pretty much follow the output of the power supply, and it will maintain a constant level in spite of two to one variations in line voltage. This is a result of regulation by the controller that is designed for the main output.

What about the secondary bias supply? In order to prevent output overshoot, the secondary bias must be above the secondary Under-Voltage-Lock-Out (UVLO) level before the output voltage of the power supply reaches 3.3V. However, the synchronous rectifier efficiency considerations limit the peak value of the secondary bias to around 10.5V. The secondary bias will thus need a post regulator. Taking further advantage of the secondary bias post regulator, the secondary bias supply can use a peak-detecting rectifier instead of a forward rectifier. The advantage here is that the secondary

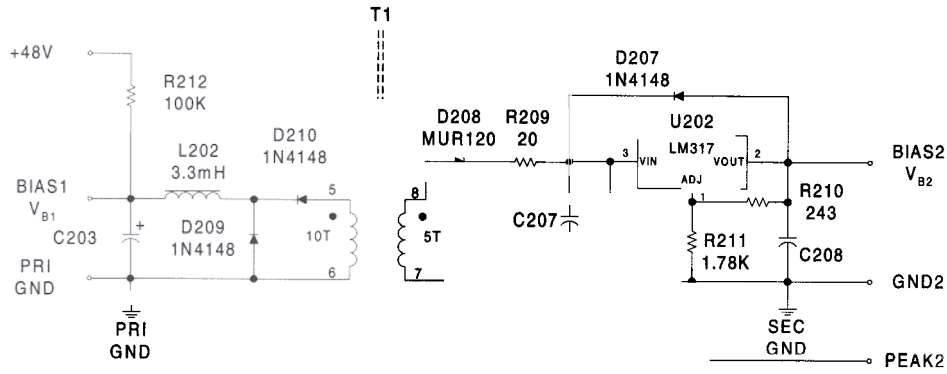

Figure 20. Schematic of bias supplies. T1 is the main power transformer.

bias will be capable of reaching UVLO threshold far in advance of the rise time of the power supply output.

Figure 20 shows the bias supplies. Resistors R210 and R211 set the regulated secondary bias voltage to 10.5V as shown in [14]. The LM317 in the TO-220 package can withstand the worst case power dissipation without a heatsink. The number of turns for the secondary bias was chosen to allow a dropout voltage of 3.3V for the LM317 during low line conditions. Hence the number of turns for the secondary bias is N_{B2}=5 turns.

Notice the addition of R209 in Figure 20. The purpose of R209 = 20Ω is to limit the peak bias current so that the peak charge current in C207 will not trip the primary side over current protection. During operation, the effective value of R209, relative to the secondary bias is R209/(duty ratio D). Thus, R209 significantly affects the secondary bias transient dynamics.

When should the hand off point occur between the primary side soft start and the secondary side soft start? Both soft start ramps are essentially open loop operations relative to the power supply output voltage. It would be difficult to perform the transfer near the steady state output voltage and maintain the 10% output overshoot specification. It is apparent here that the hand off should occur at a voltage that is noticeably lower than the steady state output voltage. We chose the hand off voltage to occur at a maximum of 1V.

Examine closely the operation of the UCC3960 through a typical start up sequence. Consider the plot of the duty ratio D(t) versus time during a typical start up, in Figure 21. The plot of duty ratio versus time will resemble the plot of the power supply output voltage. The amount that the power supply output voltage falls during the secondary soft start interval depends on how quickly the secondary supply reaches regulation compared to the natural response of the power supply output filter.

Imagine that the power supply is at zero energy state, disconnected from the 48V input power. In other words in the graph, time t is at slightly less than zero. Immediately following the application of the 48V input power, the primary bias capacitor begins charging through a low current line resistor while the UCC3960 is internally held in the OFF-state. The OFF-state is maintained until the primary bias voltage reaches the start threshold (10V) of the UCC3960.

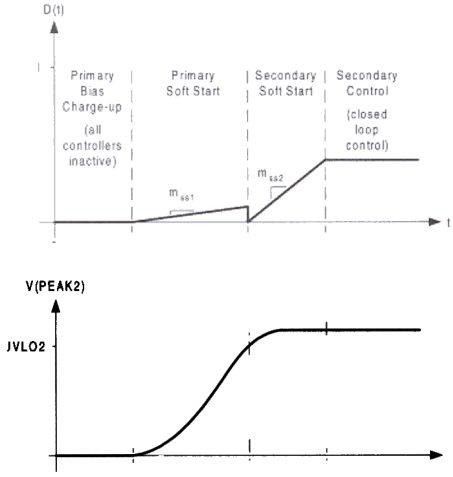

Figure 21. Duty cycle, D(t) and Bias 2 unregulated voltage during start up.

When the primary side UVLO is reached, the UCC3960 begins the Primary Soft Start interval by sending gate pulses to the primary MOSFET, Q1. The gate pulses are of constant frequency and variable duty ratio. The duty ratio starts at zero, then ramps up at a constant rate that is determined by a soft-start capacitor on the primary side, m_{ss1} duties per second. The frequency of the pulses during this interval is about 10% lower than the switching frequency of the converter under secondary side control. The switching action of the primary MOSFET Q1 begins ramping up the output and it also begins charging the secondary bias supply. When the secondary bias supply reaches the start threshold of the secondary controller (UCC3580-3, 9V), the secondary controller responds with its first pulse. Secondary side generated pulses are transmitted to the primary side UCC3960 through a Pulse Edge Transmission (PET) circuit.

Upon reception of the first pulse edge from the secondary controller, the converter commences the Secondary Soft Start interval. The secondary controller takes over control of the primary MOSFET, Q1 and it begins ramping the duty ratio from nearly zero to the point where the error amplifier in the secondary controller takes control.

Under control of the secondary controller, the UCC3960 enters a mode of operation where it waits to detect another pulse edge. Then the UCC3960 translates the pulse edge into the appropriate primary MOSFET Q1 gate level. If an edge is not detected within a predetermined window, the UCC3960 enters into a fault mode and terminates gate pulses to Q1.

During a normal Secondary Soft Start interval, the secondary controller continues to transmit pulse edges to the UCC3960, commanding an increasing power pulse width, determined by the secondary side soft start ramp components. During this interval, the soft start ramp slope is m_{ss2} duties/second. The soft start ramp of the secondary drives the output voltage of the converter up until the error amplifier on the secondary detects that the output voltage is near its set point. Then the secondary side control loop assumes control and the converter reaches steady state operation.

The selection strategy of the start up hand-off components begins by selecting the secondary soft-start slope, m_{ss2}, then select the secondary bias capacitor, then select the primary soft-start slope, m_{ss1} and finally, select the primary bias capacitor. Key constraints include the voltage rating of the MOSFETs in the synchronous rectifier, the steady state and idling bias currents, and the speed of the secondary steady state control loop.

The control loop was designed earlier to respond to disturbances up to 22kHz (138k rad/sec). The idea here is to select a soft-start ramp that is within the capacity of the closed loop converter. Experimentally, we found that there is no detectable power-up overshoot if m_{ss2} drives the output voltage about one tenth as slow as the slope of the step response of the closed loop converter. The fastest rate occurs at high line because the converter is the most sensitive to duty ratio changes at high line. We can then select the secondary soft start ramp rate in the following manner:

$$m_{ss2} \cong \left(\frac{1}{10}\right)\omega_{cf} V_{out}\left(\frac{D_{min}}{V_{out}}\right)$$
$$= (0.1)\cdot 138\cdot 10^3 \cdot 3.3\left(\frac{0.208}{3.3}\right) \qquad (41)$$
$$= 2880\ \frac{\text{duties}}{\text{sec}}$$

The secondary modulator gain and the charge rate of the soft-start capacitor set the slope m_{ss2}. The secondary soft start capacitor, C_{ss2} is charged by a 20μA current source, I_{ss2} that is internal to the UCC3580. The relationship can be rearranged in order to solve for the secondary side soft-start capacitor, C_{ss2}.

$$C_{ss2} = R_r C_r f_s \left(\frac{N_1}{N_{B2}}\right)\left(\frac{I_{ss2}}{V_{in} m_{ss2}}\right)$$
$$= 10^4 \cdot 10^{-9} \cdot 2\cdot 10^5 \cdot \left(\frac{13}{5}\right)\cdot\left(\frac{20\cdot 10^{-6}}{72\cdot 2880}\right) \qquad (42)$$
$$= 502\,\text{pF}$$
$$\text{use}\quad C_{ss2} = 560\,\text{pF}$$

The secondary bias capacitor must sustain the secondary bias voltage for the duration of the secondary soft start ramp. The secondary bias voltage must not drop by more than the 0.5V UVLO hysteresis voltage of the UCC3580-3. The secondary controller and synchronous rectifier gates will draw their average current during the secondary soft start ramp. The total secondary bias current is then 3.5mA (UCC3580) plus 34.8mA (synchronous rectifiers), or 38.3mA. The duration of the soft start ramp is the duty ratio at steady state divided by the soft start ramp rate, m_{ss2}. At high line the steady state duty ratio is 0.208 and the soft start ramp rate is 2880 duties/sec. The duration of the secondary soft start ramp will be 80.7μs. The total bias capacitance is then selected as follows:

$$C_{bias2} \geq I_{bias2}\frac{\Delta t(V_{out} = 0 \rightarrow 3.3V)}{\text{UVLO 2 Hysteresis}}$$
$$= 38.4\cdot 10^{-3}\cdot\frac{80.7\cdot 10^{-6}}{0.5} \qquad (43)$$
$$= 6.2\mu F$$
$$\text{use}\quad C_{bias2} = C207 + C208$$
$$= 10\mu F + 1\mu F$$

The output voltage at which the primary side soft-start turns over control to the secondary soft-start is a function of V_{in}, V_{UVLO2}, R209, C_{bias2} and m_{ss1}. Voltage V_{UVLO2} is the unregulated secondary bias voltage, peak2, at which the UCC3580 start threshold occurs. The UCC3580 start voltage is 9V, the LM317 saturation voltage is 1.75V and the bias rectifier voltage is 0.7V. Voltage V_{UVLO2} is then 11.5V. If a particular output hand-off voltage, V_{outHO} is required, the maximum primary soft start slope, m_{ss1} is approximated by (44). Notice here that the worst case occurs at low line condition. This may vary between topologies, so we recommend the use of a spreadsheet in order to select the correct slope for the full operating range.

$$m_{ss1} \leq -\left(\frac{N_1}{N_2}\frac{V_{out,HO}}{V_{in}}\right)^2 \frac{1}{2(R209)C_{bias2}\ln\left(1-\frac{N_1}{N_{B2}}\frac{V_{UVLO2}}{V_{in}}\right)} \qquad (44)$$
$$= -\left(\frac{13}{3}\cdot\frac{1.0}{36}\right)^2 \frac{1}{2\cdot(20)\cdot 11\cdot 10^{-6}\ln\left(1-\frac{13}{5}\cdot\frac{11.5}{36}\right)}$$
$$= 21\ \frac{duties}{\text{sec}}$$

In order to select the primary soft start capacitor, C_{ss1}, the soft start slope, m_{ss1} must be formulated using the modulator characteristics of the UCC3960. The UCC3960 has a trailing edge modulator for the primary soft start ramp. The duty ratio of the UCC3960 varies linearly from zero to 0.70 as the voltage of the primary soft start capacitor, C_{ss1}, varies from 1V to 4V. The voltage of the primary soft start capacitor rises linearly due to the charge from a 6μA current source, I_{ss1} that is internal to the UCC3960. For a maximum given primary soft-start slope, m_{ss1} the minimum soft start capacitor is given by:

$$C_{ss1} \geq \frac{I_{ss1}}{m_{ss1}}\frac{\Delta D_{max}}{\Delta V_{ss1}} = \frac{6\cdot 10^{-6}}{21}\cdot\frac{0.7}{4-1}$$
$$= 0.067\mu F \qquad (45)$$
$$\text{use}\quad C_{ss1} = 0.1\mu F$$

Using the selected value of the primary soft start capacitor, calculate the resulting primary soft start slope, using (46) and solve for the time it takes for the primary ramp to reach the soft start hand off point, using (47). The longest hand-off time occurs at low line condition.

$$m_{ss1} = \frac{I_{ss1}}{C_{ss1}} \frac{\Delta D_{max}}{\Delta V_{ss1}}$$
$$= \frac{6 \cdot 10^{-6}}{0.1 \cdot 10^{-6}} \cdot \frac{0.7}{4-} \qquad (46)$$
$$= 14 \frac{\text{duties}}{\text{sec}}$$

$$t_{hand\ off} = \sqrt{\left(-\frac{2\, R209 C_{bias2}}{m_{ss1}} \right) \ln\left(1 - \frac{N_1}{N_{B2}} \frac{V_{UVLO2}}{V_{in}} \right)}$$
$$= \sqrt{\left(-\frac{2 \cdot 20 \cdot 11 \cdot 10^{-6}}{14} \right) \ln\left(1 - \frac{13}{5} \cdot \frac{11.5}{36} \right)} \qquad (47)$$
$$= 7.4\ \text{m sec}$$

The minimum primary bias capacitor can be estimated as the size of capacitor that is required to sustain primary bias current without sagging by more than the primary side UVLO hysteresis voltage during the total power up transient. The duration is the sum of the hand-off time, calculated in (47), plus the secondary soft start time. In the usual case, the soft-start time of the secondary is insignificant, compared to the time to reach hand-off for the primary soft-start. The minimum primary bias capacitor is given in (48). A larger value was selected in order to allow margin for the UVLO hysteresis.

$$C203 \geq I_{bias\,1} \frac{t_{hand\ off}}{V(\text{UVLO1 hysteresis})}$$
$$= 0.0127 \cdot \frac{0.0074}{1.9} = 50.2\ \mu\text{F} \qquad (48)$$
$$\text{use} \quad C203 = 68\mu\text{F}$$

The results of the circuit with the power up transient are shown in Figure 22. Notice that the hand-off voltage occurs below 1V, as intended by the design. The duration of the primary side soft start is about 4ms, which is a little shorter than the predicted 5.5ms. This is probably due to DCM operation during the earliest parts of the primary soft-start ramp. The slope near the primary to secondary soft start hand off measures about 14 duties/sec, in agreement with the predictions.

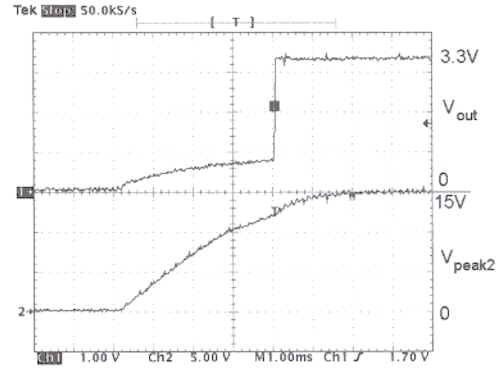

Figure 22. The power up transient at 48V line. The top trace is the 3.3V output and the bottom trace is the unregulated secondary bias voltage, V_{peak}.

The secondary soft start ramp is nearly vertical in Figure 22, as anticipated. There is no evidence of overshoot at the transition between the secondary soft start ramp interval and the steady state control interval on V_{out}. Figure 23 shows a magnified view of the power up transient at that instant.

Notice from Figure 23 that the overshoot is virtually zero, well within the 10% specifications of the converter. The slope of the secondary soft start is around 75kV/sec, which translates into about 6.8k duties/sec, compared to the expected slope of 3.9k duties/sec. This is due to the natural response of the open loop converter in the power supply. The output voltage initially develops tracking error relative to the gradually increasing duty ratio. Later during the transient, the output voltage catches up to the expected duty ratio.

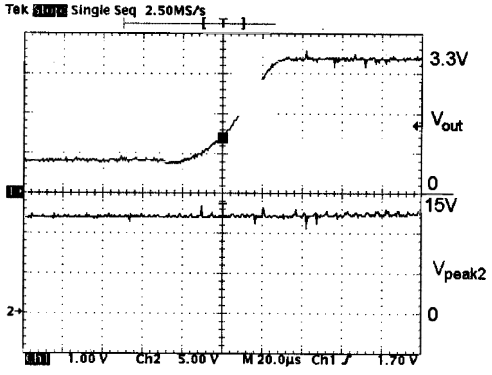

Figure 23. Close up of power up transient. The top trace is the 3.3V output and the bottom trace is the unregulated secondary bias voltage, V_{peak}.

III. EXPERIMENTAL RESULTS

The final schematic of the power stage in the synchronous rectifier configuration and the controller section are shown in Figure 24 and Figure 25, respectively. Some of the experimental results include tests that use 32CTQ030 Schottky rectifiers instead of the synchronous rectifiers. In those cases, Q202 and Q203 drain to source was replaced by a 32CTQ030 connected with both Schottky diodes in parallel.

The heat sinks that are used on power MOSFETs Q1, Q202 and Q203 are Thermalloy THM7020. These were small enough to permit approximately 30°C rise under convection cooled conditions.

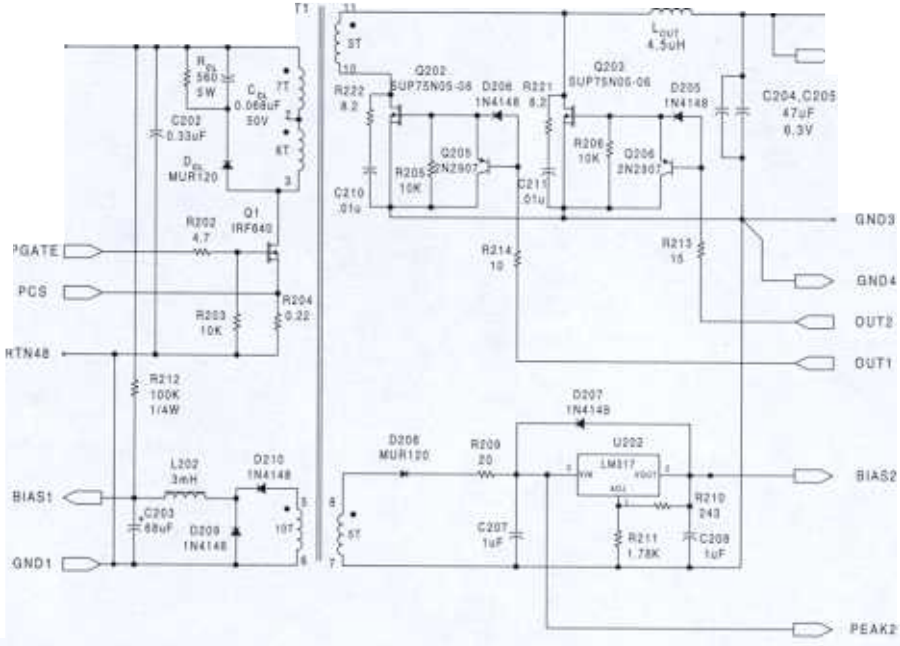

Figure 24. Power stage of the single ended forward converter with synchronous rectification, including primary and secondary bias supplies.

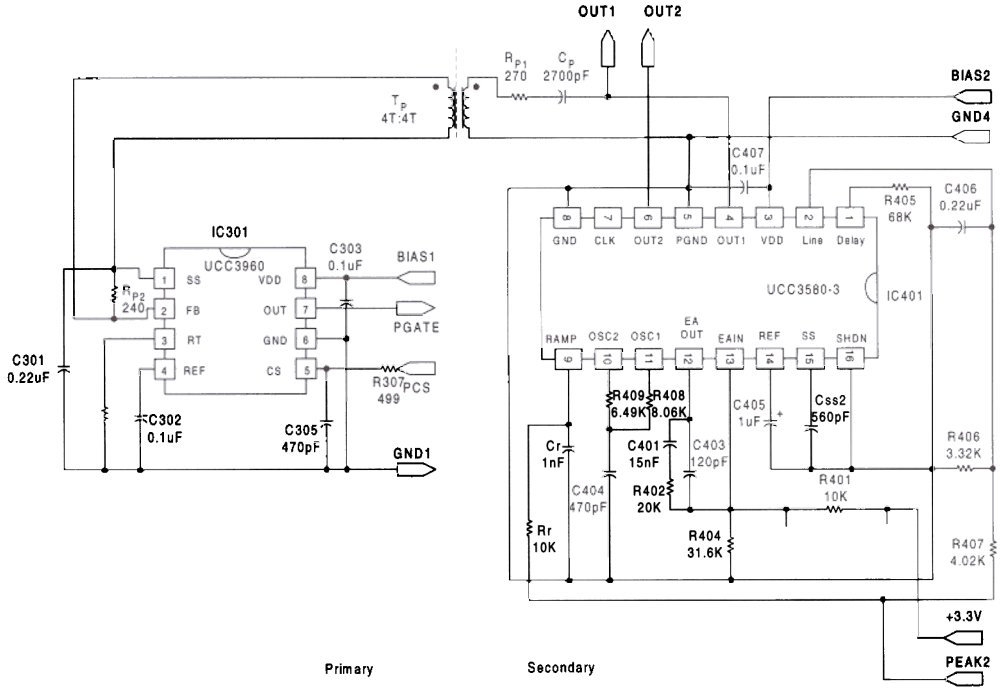

Figure 25. Primary and secondary controllers for the single ended forward converter with synchronous rectification.

Notice the snubber components, R222, C210, R221, C211, in Figure 24. These components were added in order to control the OFF-state ringing that occurred due to stray inductances and capacitances in the actual circuit. The ring frequency without the snubber was 12.3MHz for Q202 and 10.1MHz for Q203. The output capacitance of Q202 and Q203 is 1100pF. The snubber resistor value and capacitor value is given in the following equations:

$$R_{snubber} \cong \frac{1}{2\pi f_{ring} C_{oss}} \qquad (23)$$

$$C_{snubber} \cong \frac{1}{2\pi f_{ring} R_{snubber}} \qquad (24)$$

Capacitors C210 and C211 were selected as 0.01μF, which is somewhat larger than the anticipated values. The additional capacitance provided extra clamping on the initial overshoot ring. Resistors R221 and R222 were selected as 8.2Ω, which provided suitable damping during the turn-OFF interval of the parallel MOSFET. The same snubber components were needed and used in the Schottky rectified version of this converter.

Figure 26 shows a graph of efficiency versus output current. The efficiency data was measured with a line voltage of 50V. Furthermore, the experiment was performed with the identical converter and controllers; the only difference is the rectifier devices (Q202 and Q203) were replaced by a Schottky diode pair.

The graph in Figure 26 shows that the Synchronous Rectifier (SR) is more efficient than the Schottky rectifier over a load range of 3A to 14A. Both the SR configuration and the Schottky rectifier configuration operate in Continuous Inductor Current Mode over this range of output current. At output currents above 14A, the SR conduction loss becomes a larger percentage of the overall losses and eventually the Schottky rectifier becomes a more efficient configuration.

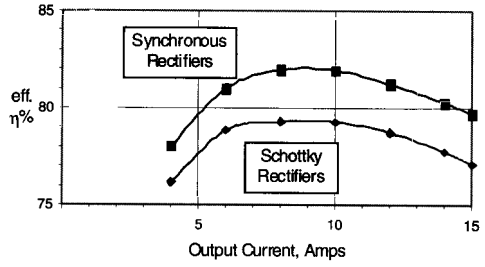

Figure 26. Efficiency versus output current of the synchronously rectified converter and the schottky rectified converter.

IV. CONCLUSION

This design review has presented a new primary side startup controller to allow the implementation of secondary control features without having the burden of a discrete auxiliary bias supply. In this example, the secondary controller was used to provide timed gate drive for a controlled synchronous rectifier while simultaneously providing duty cycle control of the primary referenced switching MOSFET. Furthermore, the implementation with the UCC3960 has the added benefit of using a small pulse edge transformer instead of an opto-coupler or a large gate pulse transformer for transmitting PWM information from the secondary to the primary side of the converter. We have demonstrated a power supply configuration that is thermally competitive to a power supply with Schottky rectifiers, yet simpler than a power supply with an independent bias supply.

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