# UC 3841 PWM CONTROLS 300 WATT OFF-LINE POWER SUPPLY

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## INTRODUCTION

With the introduction of the UC3841, Unitrode has provided a control chip uniquely optimized to implement primary side control for a broad range of power supply applications. This form of control requires significant programming and fault protection intelligence over and above the requirements for merely regulating an output voltage. These are included in the UC3841 in the form of over-voltage, under-voltage, and over-current sensing, in addition to low-current start-up, feed-forward line regulation, duty cycle limiting, slow turn-on, and optional fault latch-off.

Although all of these features are important to most off-line power supplies - and are incorporated in the design described herein - it is beyond the scope of this paper to discuss the inner workings of the control circuit. Rather, the reader is referred to the UC1841/3841 data sheet and to Unitrode Application Note U-91 describing its predecessor, the UC1840 for details of the IC implementation. This note describes the use of the UC3841 as the controller in a typical application - a 300 watt off-line power supply.

## TOPOLOGY OVERVIEW

A buck-derived, two transistor forward topology was selected for this example for several important reasons: two 400 volt transistors are typically much less expensive than one 800 volt unit; peak currents and ripple are much less than with a flyback configuration; clamping is done to the bulk DC lines eliminating the need for dissipative high-voltage snubbers; and transformer reset is automatic requiring only a 50% maximum duty cycle limitation. The basic power stage configuration and typical operating waveforms are shown in Figure 1.

While the UC3841 is compatible with either voltage or current mode control, this design is a voltage-mode configuration which takes advantage of the UC3841's controlled PWM ramp waveform to accomplish fast feed-forward line regulation while also guaranteeing an absolute 50% maximum duty cycle clamp.

## SWITCHING FREQUENCY

A design decision of equal importance to the power topology is the choice of switching frequency. For this example, 200 kilohertz was selected as an optimum compromise between minimizing the sizes of the magnetic and storage components and achieving a high overall efficiency. This frequency is high enough to keep the number of transformer turns low and yet not so high as to incur significant switching or core losses. Standard commercial devices were used throughout to demonstrate the cost effectiveness of this design.

## DESIGN SPECIFICATIONS

The specification goals which were established - and met - for this design example are the following:

Input voltage (110 VAC input) = 85 min, 135 max VAC

Input voltage (220 VAC input) = 170 min, 275 max VAC

AC line frequency = 50 Hz min

DC bulk voltage = 200 min, 385 max VDC

Output voltage = 15 volts

Output current = 20 amps max continuous

Switching frequency = 200 kilohertz

Line regulation = 10 mV

Load regulation = 10 mV

Output voltage ripple = 100 mV pk-pk, DC to 20 MHz

Efficiency = 85% at full load

## CIRCUIT OVERVIEW

The complete schematic for this 300 watt power supply is shown in Figure 2 but before discussing the details of the design, it is instructive to understand the overall approach.

The design starts with a 110 volt input voltage doubler for a nominal 290 volt DC main allowing either 110 or 220 volt operation. The control and drive circuitry are configured for low start-up current so that starting energy is accumulated in a low voltage capacitor, C10 in Figure 2, which is charged from the high-voltage bulk DC through a large-valued resistor, R2. After starting, the higher operating currents of the control and drive circuits are supplied from an efficient low-voltage winding on the power transformer. This would normally be a separate primary-referenced axillary winding and isolation would be incorporated in the feedback path for output voltage control. For this example, isolation was

# TWO-TRANSISTOR FORWARD CONVERTER

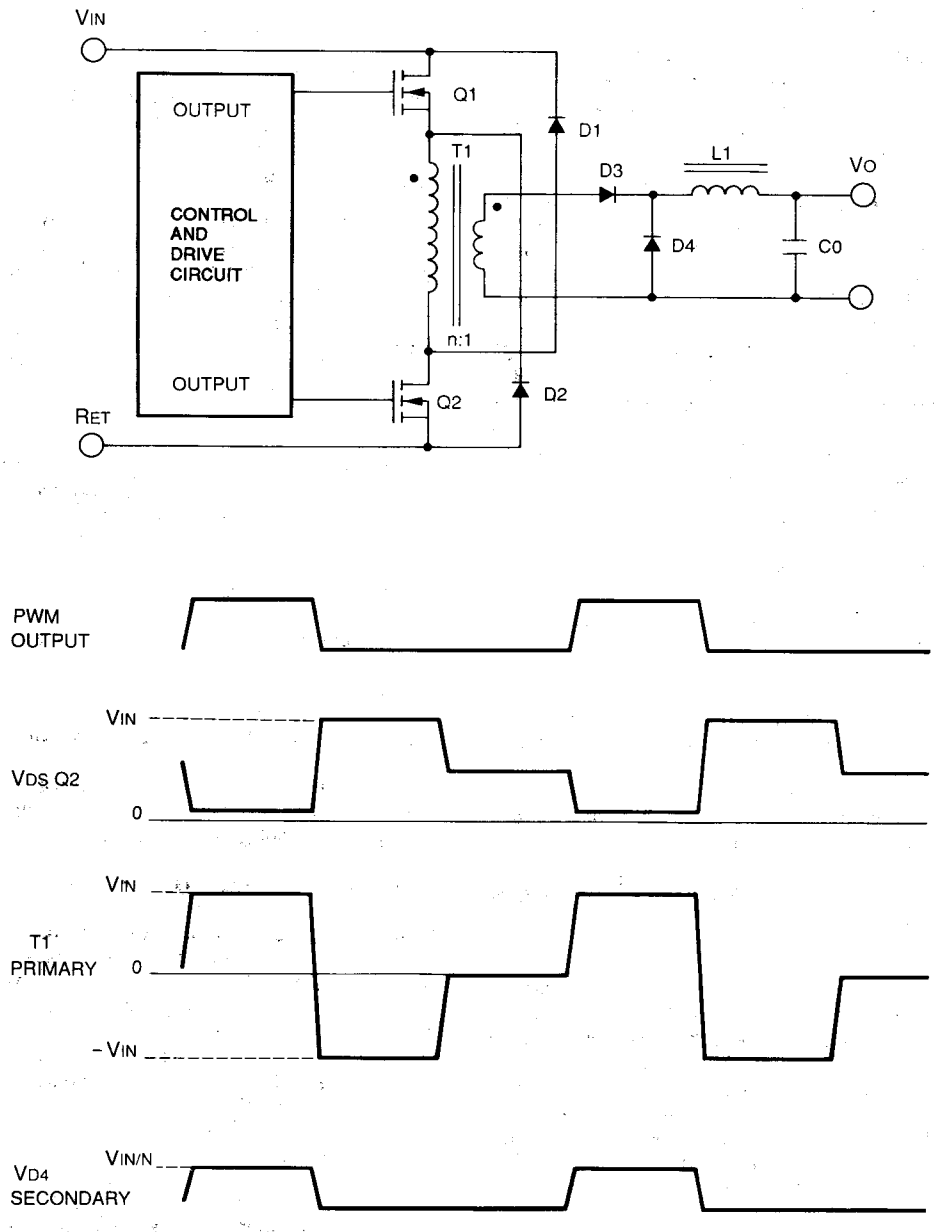


Figure 1. Basic power topology and typical waveforms for the Two-Transistor Forward Converter

ignored and operating power after start-up was taken from the 15 volt output - a simplification which can easily be remedied using common techniques which will not affect the remaining design.

The UC3841 provides the means to sense adequate energy in the start-up capacitor and initiate the turn-on sequence. It then activates the UC3707 Driver which boosts the PWM output from the UC3841 to a high peak current, source/sink drive command.

This signal is level-shifted by transformer T1 and applied simultaneously to the gates of the two power MOSFET switching devices, Q2 and Q3. These two FET's drive the power transformer, T2, in the forward direction with reset provided by D6 and D9.

Additional features which are incorporated in this design include slow turn-on - both initially and after fault shutdown, over-voltage and over-current shutdown, pulse-by-pulse current limiting for light overloads, feed forward for fast line regulation, and a maximum duty cycle clamp.

## CIRCUIT DESIGN DETAILS

### INPUT STORAGE CAPACITANCE

The amount of input, or bulk storage capacitance for a given power supply design will be determined by the more stringent of three separate requirements:

1. Maintaining a minimum DC bulk voltage as the input capacitor supports the converter between AC cycles.

2. Providing a minimum hold-up time for operation after loss of the AC line voltage.

3. Meeting the requirements for AC RMS charging current.

In this case, the value was calculated to support the primary voltage between AC cycles to a minimum of 200 VDC. In a dual voltage system, the most stringent case is the doubler configuration where there is a 180 degree phase shift between the voltage waveforms on each of the series capacitors. The minimum DC bulk voltage is then the sum of the minimum voltage on one series capacitor plus the average voltage on the other. The value of each capacitor is calculated from the following formula:

$$C1 = C2 = \frac{\text{Output power}}{\text{Efficiency} \times \text{AC frequency} \times (Vc\ peak^2 - Vc\ min^2)}$$

Where, in this example,

AC frequency = 50 Hz,

Vc peak = ( 80 x 1.414 ) - Vd = 115 V, and

Vc min = .33 ( 2 x 200 - Vc peak ) = 95 V

which determines a value for C1 and C2 of 1680 microfarads each. This was actually implemented as shown in Figure 2 by four 1000 uF units, C1 through C4.

### PRIMARY AND SECONDARY CURRENT

An estimate of the maximum primary and secondary currents is needed to select the power switches, diodes, and transformer wire sizes. A first-order approximation can be calculated from the equation:

$$Ipeak = \frac{\text{Output power}}{\text{Efficiency} \times \text{Input voltage} \times \text{Max duty cycle}}$$

$$= \frac{300}{0.85 \times 200 \times 0.50} = 3.52 \text{ Amps}$$

For rectangular wave forms, RMS currents are calculated by multiplying peak current by the square root of the duty cycle yielding 2.5 Amps of primary current and 14 Amps for the secondary winding.

### MOSFET SELECTION

As described in the Topology section, one advantage of the two-transistor forward converter is that the maximum voltage on the power switches does not exceed the peak input voltage. In this example, it allows the use of 500 Volt IRF 840 power MOSFETs which have a fairly low on resistance of 0.8 ohm, more than adequate current capability, and are available in plastic TO-220 packages. Heatsink requirements can be calculated by starting with the DC losses:

$$P\ loss = Ip\ peak^2 \times Rds\ on\ max \times D\ max$$

Extrapolating the maximum Rds on value for the IRF 840 to a junction temperature of 110°C yields 1.75 ohms which means a DC loss of 10.8 watts. Rounding up to 12 watts to include switching losses means that with a maximum ambient temperature of 70 °C, the junction will stay below 110 °C if the total thermal resistance, including the 1.0°C/W of the TO-220 package, is held to less than 3.3°C/W.

### RESET DIODES

Since the current through the reset diodes, D9 and D10, returns to zero when the core completes reset, diode reverse recovery time is not critical. Forward turn-on time is still important, though, in order to catch the transformer energy when the power switches turn off, but this is a much simpler problem and UES 1106 rectifiers are more than equal to the task.

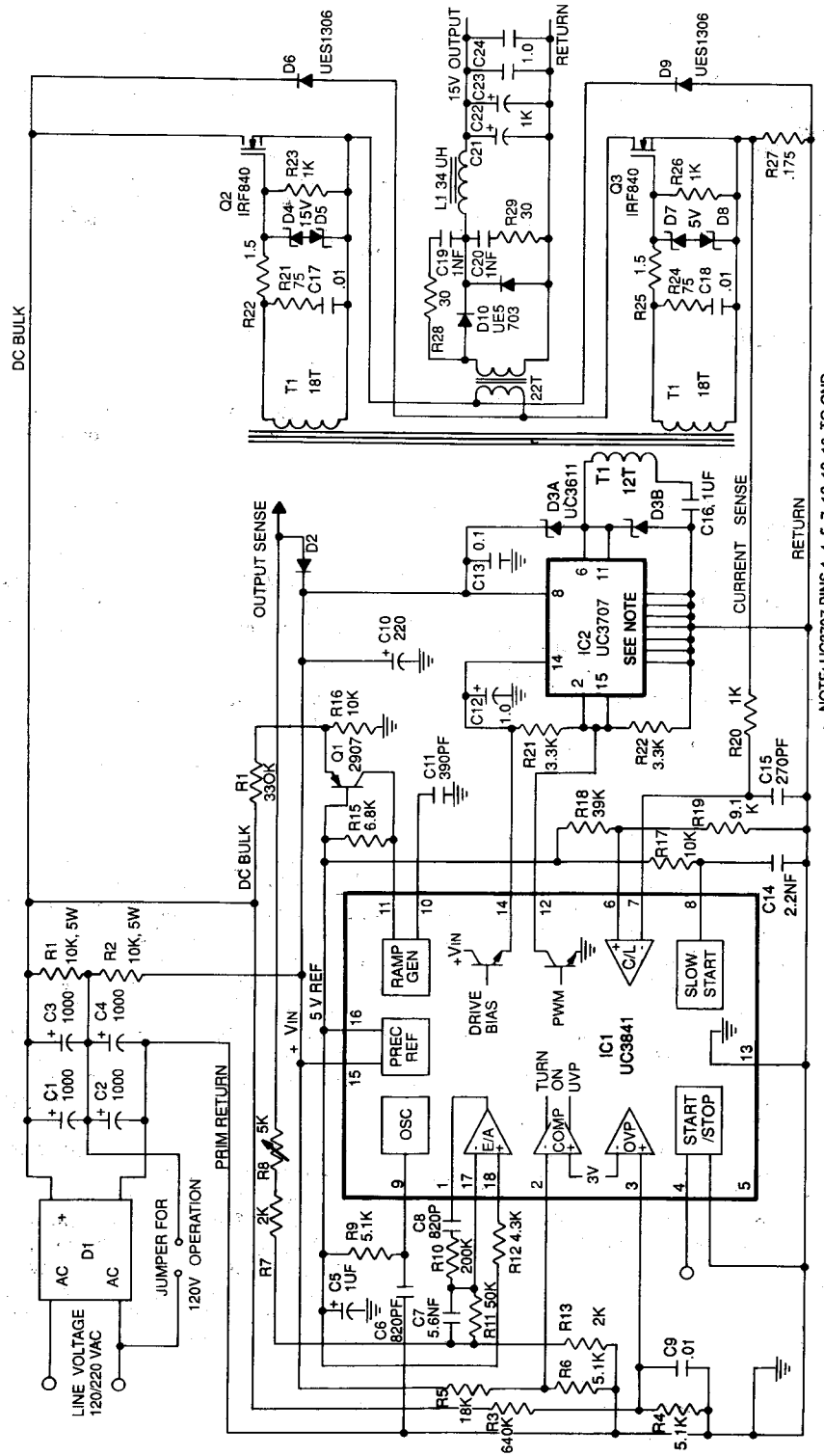


Figure 2. Overall schematic for a 300 watt, off-line power converter using the UC 3841 for control

## TRANSFORMER DESIGN

As a general guideline, operation at higher frequencies usually produces a transformer design which is core loss, rather than flux swing, limited. Under these conditions, it is best to start with the core area-product calculation using the formula:

$$AP = AwAe = \left( \frac{Pin \times 10^4}{120\ K\ 2f_t} \right)^{1.58} \times (Kh\ f + Ke\ f^2)^{.66} cm^4$$

where:

Pin = Input Power = 353 Watts

K = Winding Factor = .141 (for a fwd conv)

$f_t$ = Transformer Frequency = 200 kHz

Kh = Hysteresis Coefficient = $4 \times 10^{-5}$ (3C6A)

Ke = Eddy Current Coefficient = $4 \times 10^{-10}$ (3C6A)

For this design, the area-product calculates to 2.9 $cm^4$ allowing a comfortable selection of an ETD-44 ferrite core made of 3C6A material. Core selection is typically an iterative process with the first core choice used to define the windings which, in turn, allows calculation of both winding and core losses. If these answers are not acceptable, another core size is selected and the process repeated.

The manufacturer defines the ETD-44 core as having a volume of 18.0 $cm^3$ and a thermal resistance of 12°C/W. Selecting 40° C as a reasonable limit for the maximum temperature rise of the transformer and recognizing that core loss will be an important factor, an arbitrary starting point for the transformer design is to allocate 30°C to the core and 10°C to the copper. With this assumption, the core power density can be calculated from:

$$\text{Power Density} = \frac{\text{Temp rise}}{\text{Therm Resist x Volume}} = 140\ mW/cm^3$$

The manufacturer's curves of core losses for the 3C6A material at an operating frequency of 200kHz show a corresponding peak flux density of approximately 600 Gauss which equates to a peak-to-peak value of 1200 Gauss, or 0.12 Tesla. Additional data needed to calculate the primary turns are the primary voltage, Vp = Vin - Vsat, and an estimate of the maximum duty cycle which, to provide some margin, is initially set at 0.47. With these inputs, the primary turns are defined by:

$$Np\ min = \frac{Vp \times Ton \times 10^4}{\text{Flux swing x Core area}}$$

$$= \frac{190 \times 2.35 \times 10^{-6} \times 10^4}{12 \times 1.74} = 21.3\ turns$$

The transformer turns ratio is defined as:

$$\frac{Np}{Ns} = \frac{Dmax \times Vp}{Vo + Vd} = Dmax \times \frac{190}{15.8} = 12.025\ Dmax$$

At this point, there are two considerations to balance: The desire to make Dmax as close to 0.5 as possible so that the peak current is low, while keeping the number of turns to low, whole numbers. For this example, the best choice is

$$\frac{Np}{Ns} = \frac{22\ Turns}{4\ Turns}$$

and Dmax = 0.46.

With this duty cycle, the peak primary current can be more accurately calculated as 3.84 Amps with an RMS value of 2.6 Amps.

The remaining transformer calculations are summarized below:

Primary inductance, Lp = Al x $Np^2$ = 1.26 mH

Magnetizing current, Im = Vp x Ton / Lp = 347 mA (peak)

Primary conductor area, Axp = Ip rms / 450 = .00578 $cm^2$ min

Secondary conductor area, Axs = Is rms / 450 = .0301 $cm^2$ min

While the primary wire area corresponds to a wire size of AWG 19, and the secondary is equivalent to AWG 12, both have to be evaluated in terms of their active area at 200 kHz. From Eddy Current calculations it can be determined that the depth of penetration of current at 200 kHz is .017 cm which does not effectively utilize the .091 cm diameter of AWG 19 wire. While multiple strands of finer wire help, increasing the number of strands also increases the number of layers which forces the wire thickness to be substantially less than the penetration depth in order to minimize the AC loss.

A more effective solution - which is made more practical because of the relatively few number of turns - is the use of flat copper strip. For the primary, a strip .0044 cm thick (approximately 2 mils ) and 2.5 cm wide was insulated with 2 mil mylar between each turn and wound in two sections - eleven turns under and eleven turns over the secondary. The secondary was also made of copper strip, in this case .020 cm thick. A cross section sketch of the transformer winding technique is shown in Figure 3.

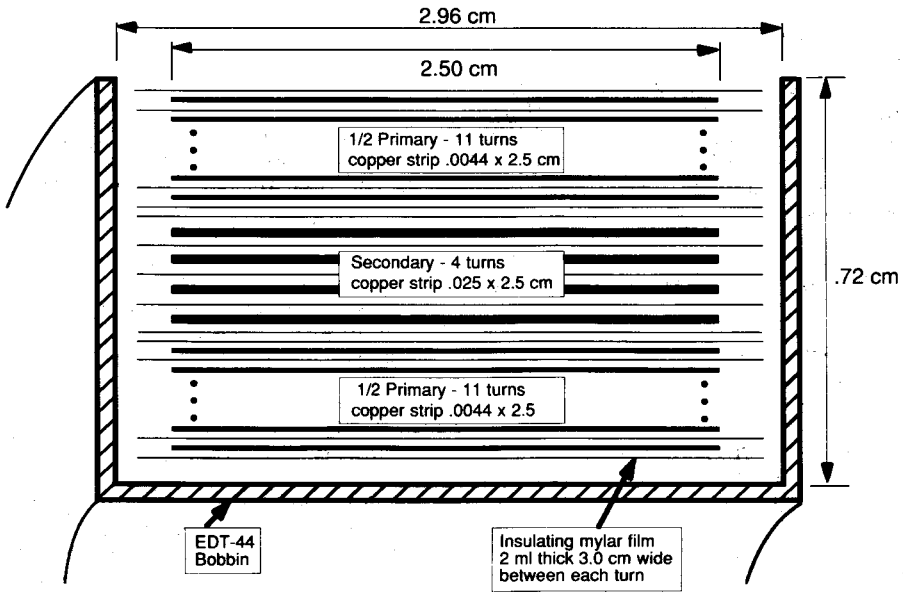


Figure 3. Cross section of one-half of the power transformer illustrating the strip winding techniques which minimize both Eddy Current losses and leakage in ductance.

With the windings defined, the total transformer losses may be calculated as follows:

Core loss = Power density x Volume = 2.52 Watts

$$\text{Primary resistance} = \frac{\text{Copper ohm-cm x ave cm/turn x Np}}{\text{Strip cross-section area}}$$

$$= \frac{2.29 \times 10^{-6} \times 7.6 \times 22}{.0044 \times 2.5} = 35 \text{ milliohm}$$

Wire loss (prim) = $Ip_{rms}^2$ x Rp = 0.24 Watts

$$\text{Secondary resistance} = \frac{2.29 \times 10^{-6} \times 7.6 \times 4}{.020 \times 2.5} = 1.39 \text{ milliohm}$$

Wire loss (sec) = 0.26 Watts

Total power loss = 2.52 + 0.24 + 0.26 = 3.02 Watts

Temperature rise = 3.02 W x 12 °C/W = 36 degrees.

## GATE DRIVE TRANSFORMER

Since both the number of turns and the currents are small for this gate drive transformer, a toroidal core shape is an efficient solution and the core selected was the Ferroxcube 846T250 made of 3C8 ferrite material with an outside diameter of 0.875 inches. The design equations and guidelines are similar to the power transformer example. In this case, the primary winding is capacitively coupled to the driver IC to prevent core saturation. Because of the DC offset voltage on the capacitor, the primary voltage will now be to some extent dependent upon pulse width. A step-up turns ratio was used to the secondary with 15 volt zener clamps to limit the gate-to-source voltage on each FET. Twelve turns were used for the primary resulting in a 500 Gauss flux swing. Each secondary winding consists of 18 turns and the total core loss is calculated at 0.13 Watt.

## OUTPUT INDUCTOR

The output inductor was designed for less than 1.8 Amps of ripple current at full load and minimum duty cycle using the equation:

$$L = \frac{(Vo + Vd) \times Toff}{\Delta Io \text{ max}}$$

and from:

$$Dmin = Dmax \times \frac{Vin \text{ min}}{Vin \text{ max}} = 0.46 \times \frac{200}{385} = 0.239 \text{ and}$$

$$Toff \text{ max} = \frac{1 - Dmin}{f_t} = \frac{0.761}{0.2 \text{ MHz}} = 3.81 \text{ us}$$

the inductance value is then defined as:

$$L = \frac{15.8 \times 3.81}{1.8} = 33.4 \text{ uH Min}$$

Selected for this application was an ETD type core made from 3C8 material. This material was chosen because of its high saturation flux density of greater than 3000 gauss. Here again, it is necessary to determine whether the design will be core loss or saturation limited but since this is a forward converter with the inductor in the continuous mode, the AC ripple current is a small percentage of the DC load current and the core should be saturation limited.

The core selection process again starts with a calculation of window - area product using the equation:

$$AP = AwAe = \left( \frac{L \times Ipk \times Ifl \times 10^4}{420 \times K \times Bmax} \right)^{1.31} cm^4$$

$$= \left( \frac{34 \times 10^{-6} \times 25 \times 20 \times 10^4}{420 \times 0.7 \times 0.3} \right)^{1.31} = 2.36\ cm^4$$

With this AP value, an ETD-39 core was selected with a value of Ae = 1.25 $cm^2$. The minimum number of turns can then be calculated from:

$$Nmin = \frac{L \times Ipk \times 10^4}{Bmax \times Ae} = 23\ Turns$$

The gap length is then calculated using the classic inductance formula:

$$lg = \frac{\mu_o \times \mu_r \times N^2 \times Ae \times 10^{-2}}{L} = 0.219\ cm$$

with $u_o = 4\ \pi \times 10^{-7}$ and $u_r = 1$. To obtain the desired inductance, however, the actual gap must be almost twice as large to account for the fringing field which is not included in the above formula.

This inductor was also wound with copper strip but in this application the task is easier as neither Eddy Current losses nor space for high-voltage insulation need be considered. A strip 2.5 cm wide of 10 mil ( .025 cm ) copper was used which, with a mean turn length of 6.7 cm, gave a DC resistance of

$$R = \frac{2.29 \times 10^{-6} \times 6.7 \times 23}{0.025 \times 2.5} = 5.65\ mohms$$

and a power loss at full load of 2.26 Watts.

## OUTPUT CAPACITOR

There are two sources of ripple voltage which need to be considered in meeting the design goal of 100 millivolts and they are both caused by the inductor ripple current. The first is merely

$$\Delta Vo = \Delta Q / Co$$

and, for a given ripple current, is minimized by increasing the capacitor value. The minimum capacitance, if this was the only contributor, is

$$Cout\ min = \frac{1 \times \Delta Io \times 1 \times 1}{2 \times 2 \times 2f \times \Delta Vo}$$

$$= \frac{1.8}{8 \times 200k \times 0.10} = 11.25\ microfarads$$

The second source of ripple voltage is the voltage drop across the ESR of the capacitor caused by the ripple current. The maximum ESR allowable for 100 mV ripple is

ESR max = 100 mV / 1.8 A = 56 mohms.

The two contributors of ripple voltage do not add directly as there is a 90 degree phase difference between them. Typically, in order to achieve a reasonable ESR, the capacitance value becomes so much greater than the minimum value that the $\Delta Q / Co$ term can be ignored. An added benefit of a large output capacitance is the improvement in load transient capability.

For this design, two 470 uF electrolytic units were used in parallel to achieve an ESR value of 3 to 15 mohms - a broad range necessitated by the difficulty in getting specified high-frequency data from capacitor manufacturers.

A final component added to the output filter is a good, high-frequency capacitor to bypass the inductive components of the electrolytics and shunt any switching spikes which might get to the output. A 1.0 uF ceramic monolythic capacitor is a good selection for this application.

## OUTPUT RECTIFIERS

The output diodes need to be able to handle the output current of 20 Amps, have 150 Volt reverse capability, and be extremely fast. Unitrode UES 703 rectifiers were selected for this application because of their 35 nsec reverse recovery specifications, as well as their low forward drop of 0.8 Volts max. Since one of the output diodes will always be conducting, it is advisable to mount both on the same heatsink designed to dissipate approximately 16 Watts with a 30 °C temperature rise. This will keep the junction temperature below 100 °C in a 70 °C ambient.

## PROGRAMING THE CONTROL FUNCTIONS

With the completion of the power path design, the remaining tasks all relate to programing the many functions of the UC3841. In the interests of readability, the description which follows is a somewhat qualitative discussion of the methods for implementing the functions rather than a rigorous derivation of each component's value. Again, reference to the UC3841 data sheet is necessary for detailed specification limits and tolerances.

POWER SUPPLY START UP

When line voltage is first applied, the UC3841 is in its OFF state and draws less than 5mA from the line through R1 and R2. While there is an additional 2.4 mA due to the various programing resistors, the UC3707 draws no current as it is powered from the Driver Bias output of the UC3841 which is off during start up. Therefore, resistors R1 and R2, which are necessary anyway to discharge the bulk storage capacitors, can easily provide the current to charge the start up capacitor, C10, without the power dissipation which would require complex circuitry to disconnect them after start up.

The resistor divider of R5 and R6 performs two functions. The ratio of these resistors determines the actual turn-on voltage at C10 while their effective series impedance provides hysteresis such that turn-off occurs at a lower level than turn-on. In this circuit, the turn-on voltage is 17V and the hysteresis is 3.5V. This means C10 will charge to 17V while most of the circuit is off. When turn-on is initiated, the added load of the driver will cause this voltage to decay and it will fall either to 14.4V where the power supply output will catch it through D2, or, if start up does not take place, to 13.5V where the control will turn off and start a new cycle.

Prior to turn-on, and after a low-voltage turn off, the Soft-Start capacitor, C14 on Pin 8, is clamped low. At turn on, although the Driver Bias immeadiatly activates the UC3707, no power pulses are generated while Pin 8 is low. As C14 charges, PWM commands begin and the pulse width increases with a rate of increase defined by the time constant of C14 and R17. This time constant needs to be selected remembering that while start up is taking place, all the drive energy is coming from C10 so the charge of C14 has to be faster than the discharge of C10. These waveforms are shown in perspective in Figure 4.

## START-UP WAVE FORMS

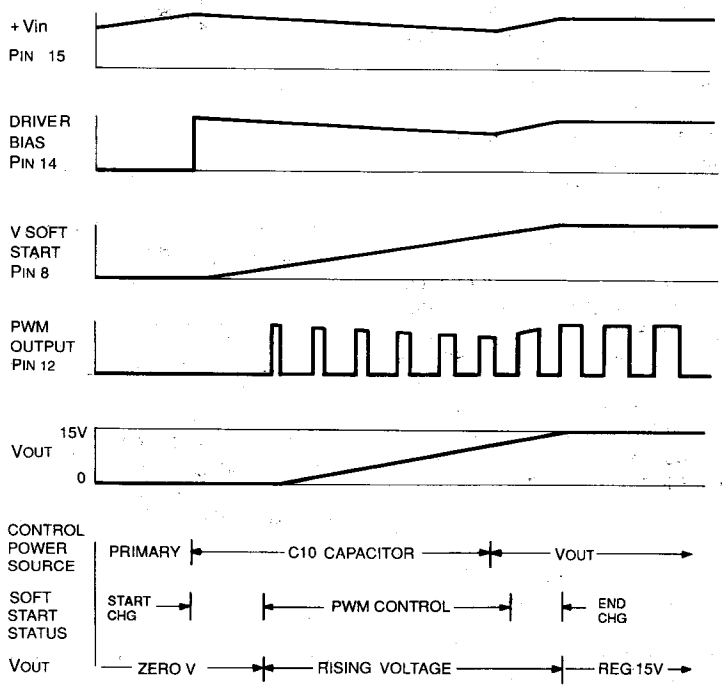


Figure 4. Initial start-up waveforms showing the slow turn on of the power output stage.

## OSCILLATOR AND RAMP

The UC3841 operates at a fixed frequency determined by R9 and C6 on Pin 9. The pulse width modulation is performed by comparing the Error Amplifier's output to a separate ramp waveform generated on Pin 10. The slope of this ramp is given a minimum value by R15 charging C11 from the 5.0V reference. These components define a rise time of 2.5 usec and thereby establish a maximum duty cycle clamp of 47 percent. The network of Q1, R14, and R16 sense the DC bulk voltage and provide an increasing charge current to C11 - thereby increasing the slope of the ramp for bulk voltages above 200 volts. This increase in slope linearly tracks the input line voltage and modulates the PWM output signal providing fast, pulse-by-pulse, open-loop line regulation which greatly eases the requirements of the feedback control loop.

## FAULT PROTECTION

Load current is sensed through the power transformer by a sense resistor, R27, in series with the power switches. The value of R27, in conjunction with the divider of R18 and R19, establish a threshold at Pins 6 and 7 of 23 Amps as related to the output. When this threshold is exceeded, the UC3841 goes into a pulse-by-pulse reduction in width to limit the energy and allow the power supply output to fall. Because of circuit delays, however, this limiting only works to a minimum pulse width which might allow too much energy to protect against a short circuit. This eventuality is covered by a second, higher threshold in the current sensing circuit which triggers a Fault Latch for immediate shut down. This Fault Latch is also activated by the Over-Voltage comparator which, in this case, is monitoring the input line voltage through R3 and R4.

Once triggered, the Fault Latch immediately terminates the PWM signals and discharges the soft-start capacitor. If the Reset Pin 5 is high, once latched, the circuit will stay off until either the input line is recycled or Pin 5 is momentarily pulled low. If Reset is already low, the Fault Latch will reset when the soft-start capacitor completes its discharge, allowing an automatic restart. The Fault Latch may also be activated externally by forcing positive current into Pin 4.

## THE UC3707 DRIVER

This device is used only as an interstage driver to take the pull-down output from the UC3841 and develop the high current turn-on and turn-off commands to the power MOSFETs. This is a dual driver but in this case the two channels are connected in parallel to provide a maximum peak current of 3 Amps, source or sink. Of course, the DIL package would provide a power limitation were it not for the fact that the high currents are needed only to charge and discharge the MOSFET gate capacitance. When driving a load which has both inductance and capacitance, it is important to keep any ringing which might appear on the output of the driver chip confined within the limits of the supply voltage to that chip. This is easily accomplished with the UC3611 Schottky diode array used for diodes D3A and D3B.

## CLOSING THE LOOP

In this voltage-mode application, the output filter will exhibit a two pole response to the control loop. Loop compensation at the Error Amplifier is designed to contain two pole-zero pairs by using the configuration shown in Figure 5. This will insure overall loop stability with maximum high frequency response while retaining a large low frequency gain.

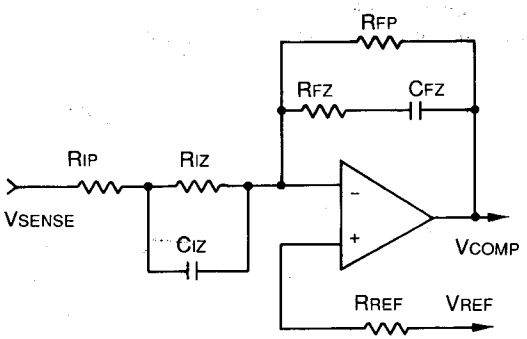


Figure 5. A generalized two pole-zero compensation approach to providing good loop stability.

The generalized approach to this compensation network is to place the first pole at a low frequency, typically around one Hertz. Two zeros are then introduced at approximately one-half the output filter break frequency to compensate for its two-pole rolloff. The amplifier's second pole is placed at a fairly high frequency to provide a predictable gain reduction; however, the amplifier will usually run out of gain-bandwidth prior to reaching this pole.

The output filter response is defined by:

Lout = 34 uH, Cout = 1000 uF,

Rload = 0.75 to 10 ohms, ESR = 3 to 15 mohms

$$\text{Pole freq} = \frac{1}{2\pi\sqrt{LC}} = 865 \text{ Hz}$$

$$\text{ESR zero} = \frac{1}{2\pi \times C \times ESR} = 10.6 \text{ to } 53.1 \text{ KHz}$$

The error amplifier compensation poles and zeros are located at the following frequencies referenced to the components of Figure 5:

$$\text{Input zero} = \frac{1}{2\pi \times Riz \times Ci} = 568\ Hz$$

$$\text{Input pole} = \frac{Rip + Riz}{2\pi \times Rip \times Riz \times Ci} = 23\ kHz$$

$$\text{Feedback zero} = \frac{1}{2\pi \times Rfz \times Cf} = 970\ Hz$$

$$\text{Feedback pole} = \frac{1}{2\pi\,(Rfp + Rfz)\,Cf} = 1\ Hz\ (approx)$$

The effect of these poles and zeros is shown graphically in Figure 6 where it can be seen that they provide an overall response with a single pole roll-off to 10 kHz. The gain crosses zero dB at approximately 8 kHz with more than adequate phase margin, regardless of the output capacitor's ESR.

## POWER SUPPLY PERFORMANCE

The use of the UC3841 control IC has allowed a very straight forward and simple implementation of a relatively high performance power supply with a remarkedly small number of components. Representative waveforms of performance at several points within the supply are shown in Figures 7 - 10. All the initial performance goals defined for this design were met and it is hoped that with the information presented above, application to more sophisticated or specialized design tasks will be eased.

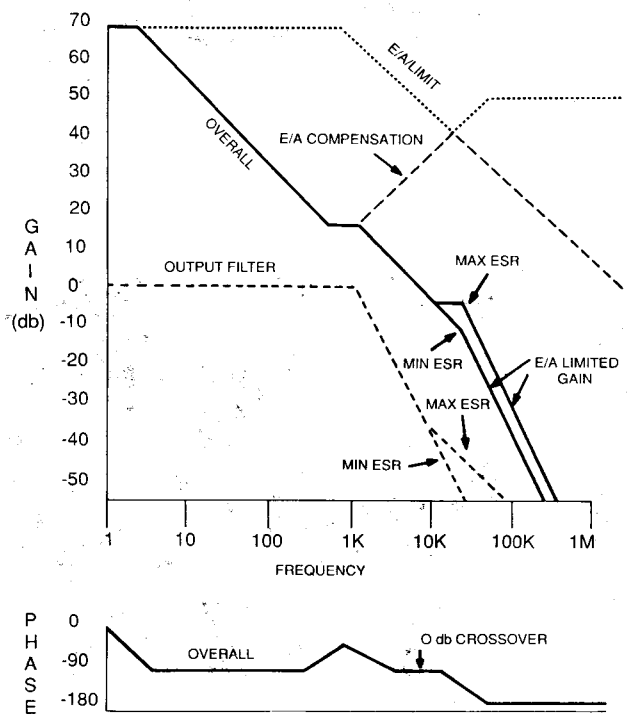


Figure 6. Total power gain and phase relationships showing the effects of loop compensation.

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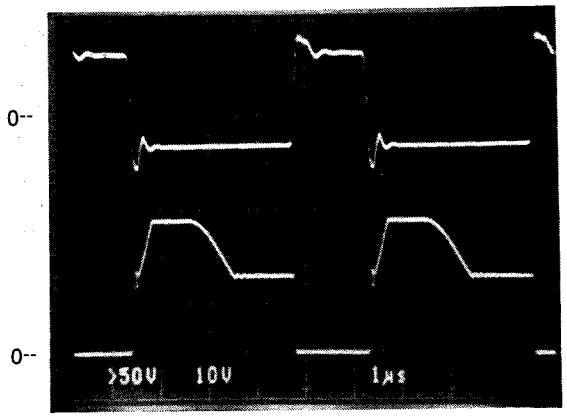
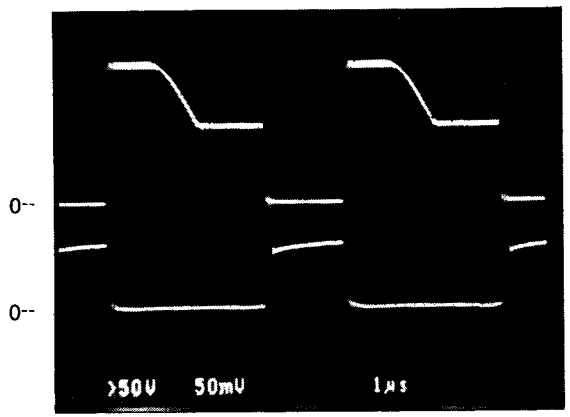
# OPERATIONAL WAVEFORMS




PRIMARY

Top: $V_{GS}$ Q1 10 v/cm
Bottom: $V_{DS}$ Q1 100 v/cm
Horizontal: 1 µs/cm

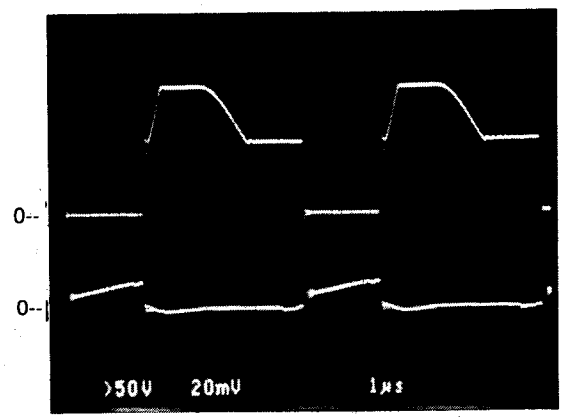
Figure 7. Gate-to-source and Drain-to-source voltage waveforms for the upper FET switch




FULL LOAD

Top: $V_{DS}$ Q1 100 v/cm
Bottom: Ipri 2 A/cm
Horizontal: 1 µs/cm

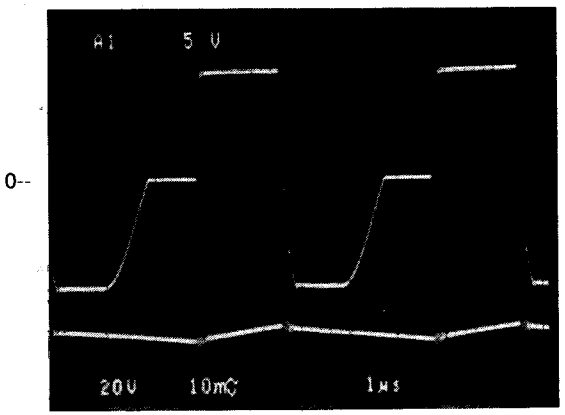
Figure 8. Power switch voltage and current waveforms at full load.




LIGHT LOAD

Top: $V_{DS}$ Q1 100 v/cm
Bottom: Ipri 1 A/cm
Horizontal: 1 µs/cm

Figure 9. Power switch voltage and current waveforms at light load.




SECONDARY

Top: Vsec 20 v/cm
Bottom: Vout (AC) 10 mv/cm
Horizontal: 1 µs/cm

Figure 10. Transformer secondary voltage and power supply output ripple.

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