A 250 Watt Current-Controlled SMPS With Synchronous Rectification

(HEXFET is the trademark for International Rectifier Power MOSFETs)

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Introduction

This application note illustrates ways in which International Rectifier's HEXFET power MOSFETs may be used in switched mode power supplies. In particular it focuses on circuit ideas which in the past may not have been attractive because of the relatively large number of HEXFETs that are employed. However, now that efficient high volume production has reduced the costs of HEXFETs in many cases to less than that of the equivalent bipolar transistor, these circuits are worthy of serious consideration.

One of the features illustrated here is the use of a pre-regulator to form a current source for the subsequent push-pull transformer converter stage. The use of a pre-regulator permits the dc link voltage to be reduced to a value which allows the use of 400 volt HEXFETs with power supplies operating from a 240 Volt ac supply. Since the Rds(on) of power MOSFETs is approximately proportional to $V^{2.6}$, reducing the voltage rating of the HEXFETs often results in a reduction in the cost of the switching devices required.

A second feature illustrated here is the use of synchronous rectification, in which the rectifier diodes in the output stage of the power supply are replaced by HEXFETs switching in synchronism with the HEXFETs controlling the primary winding of the transformer. The synchronous rectifier employed in this design results in rectifier losses about 40% lower than would be incurred by using an output rectifier stage based on Schottky diodes.

The basic performance figures for the supply are:

Input voltage 240/120 V ac

Output voltage 5 V dc

Output current 10 – 50 Amps

Efficiency 86%

Switching frequency 100 kHz

Ripple <1%

Power Circuit Operation

Figure 1 shows the circuit diagram of the power section of the power supply; the control circuit is shown in Figure 2 (see page 2).

As Figure 1 shows, the ac line is rectified to produce a nominal dc link voltage of up to 340 V. Switch S1 selects the input voltage range. A current source, made up of Q6, Q7, D9 and L2 supplies current to the push-pull inverter formed by T5, Q8, and Q9. The output of transformer T5 is rectified by the synchronous rectifier composed of Q10 to Q17.

Q8 and Q9 operate in anti-phase with a 50% duty cycle. Since T5 is current fed no harm results if there is a slight overlap of the conduction periods of Q8 and Q9 and therefore simple circuitry can be used to generate the gate waveforms for Q8 and Q9. Furthermore there is no possibility of the core of T5 becoming saturated due to "flux walking." Q10 to Q17 in the synchronous rectifier also operate with a 50% duty cycle and can be driven from the same source that drives Q8 and Q9.

The conduction period of Q6 and Q7 is pulse-width modulated under the control of the output voltage feedback signal. If the output voltage falls, the conduction period is lengthened to increase the flow of current to the inverter stage. The resulting rise in output current restores the output voltage to the desired level. The switching frequency of Q6 and Q7 is identical with that of Q8, Q9 and Q10 to Q17.

D10 and D11 in conjunction with C15 clip the voltage spikes produced at the drains of Q8 and Q9 by leakage inductance in T5. Energy recovered by the clipping diodes is fed back to the dc link.

Transformer T4 senses the instantaneous value of the dc link current and provides a signal for the current limit function of the control IC.

Control Circuit Operation

Figure 2 shows the circuit diagram of the control circuit. A type 3526 integrated circuit (IC 1) forms the central control element. This IC is supplied from a small auxiliary power supply driven from the line via transformer T1. This permits the control IC to be referenced to the output ground thereby avoiding the necessity to provide an isolated feedback signal from the output. An alternative approach is to supply the IC from an auxiliary secondary winding on T5 with a zener regulated supply derived from the main dc link rail providing the current during start-up with some form of feedback signal isolation. An auxiliary supply using a main transformer has the advantage of being simple and efficient.

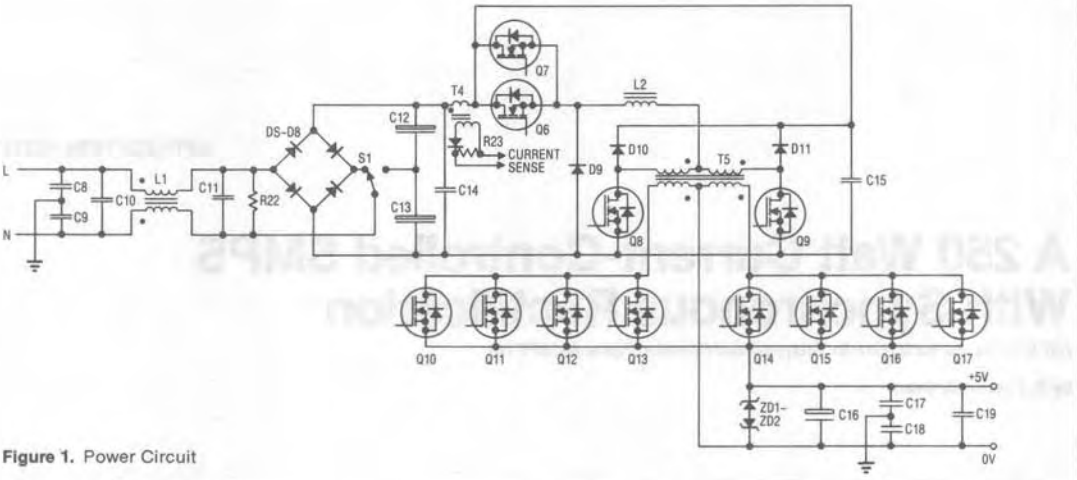
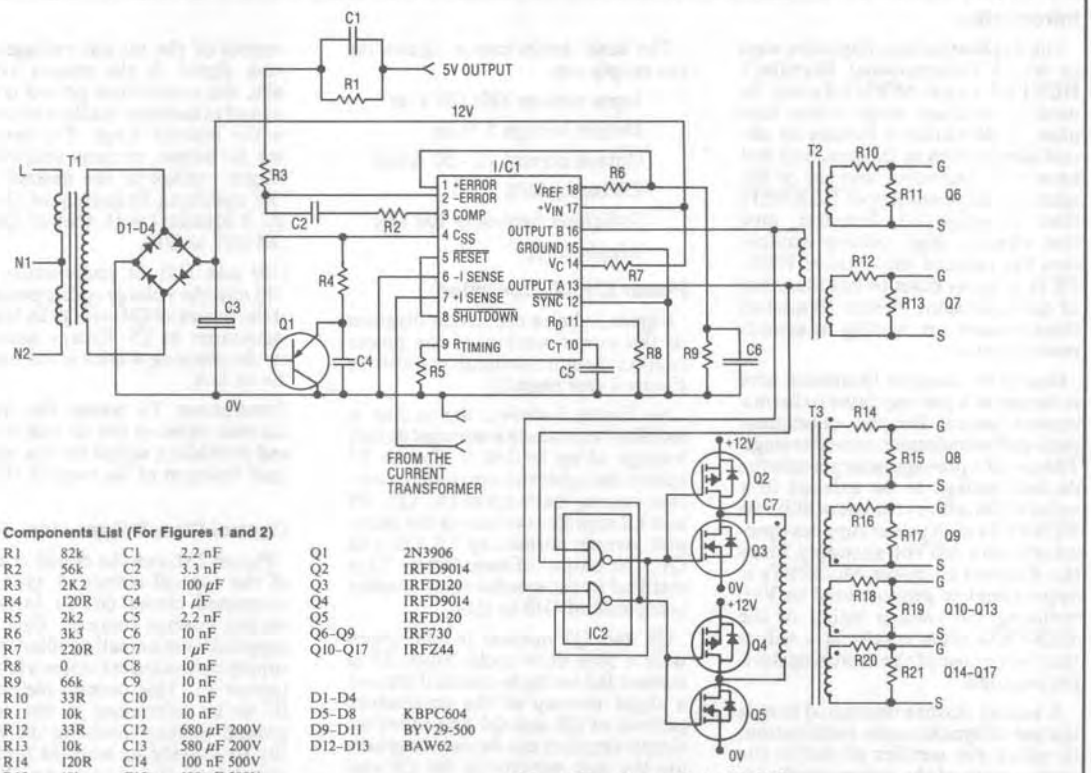


Figure 1. Power Circuit



Components List (For Figures 1 and 2)

R1	82k	C1	2.2 nF	Q1	2N3906
R2	56k	C2	3.3 nF	Q2	IRFD9014
R3	2K2	C3	100 μF	Q3	IRFD120
R4	120R	C4	1 μF	Q4	IRFD9014
R5	2k2	C5	2.2 nF	Q5	IRFD120
R6	3k3	C6	10 nF	Q6–Q9	IRF730
R7	220R	C7	1 μF	Q10–Q17	IRFZ44
R8	0	C8	10 nF		
R9	66k	C9	10 nF		
R10	33R	C10	10 nF	D1–D4	
R11	10k	C11	10 nF	D5–D8	KBPC604
R12	33R	C12	680 μF 200V	D9–D11	BYV29-500
R13	10k	C13	580 μF 200V	D12–D13	BAW62
R14	120R	C14	100 nF 500V		
R15	10k	C15	100 nF 500V		
R16	120R	C16	3X 1000 μF 10V	ZD1	12V 400 mW
R17	10k	C17	100 nF 100V	ZD2	12V 400 mW
R18	120R	C18	100 nF 100V	IC1	3526
R19	10k	C19	470 nF 100V	IC2	4011B
R20	120R				
R21	10k				
R22	1M				
R23	1R				

C12 and C13 are Nippon Chemical NMHR
C16 (3 of) are Nippon Chemical RXVD

L1 347 μH (2 windings of 10 turns. d = 0.8 mm on an FX4054 core).
L2 2 mH (120 turns. d = 0.8 mm on ETD39 with 1 mm air gap).

T1 3 VA 240/110 V 10V secondary.
T2 3 x 30 turns of d = 0.24 mm on FX4053 (Lm = 2 mH)
T3 5 x 30 turns of d = 0.24 mm on FX4054 (Lm = 3.12 mH)
T4 Primary 1 turn, secondary 60 turns of d = 0.2 mm on FX4053
T5 2 x 29 turns of 1.0 mm primary windings wound in separate layers (Lp = 3.11 mH, R = 43 mOhms). 2 x 2 turns secondary winding of 81-strand Litz wire (d = 0.2 mm). Core type ETD49.

Figure 2. Control Circuit

The gate drive signals for Q6 and Q7 are derived from the IC's complementary outputs via transformer T2. The complementary outputs are also used to toggle the flip-flop composed of two gates from IC 2. The square wave outputs of IC 2 control Q2 to Q5 which act as drivers for transformer T3. T3 provides the gate signals for Q8 to Q17.

Design Issues

Input Stage

A conventional RFI filter with common mode (C8 and C9) and differential mode (C10 and C11) stages has been used. It is important to take the impedance of this filter into account when designing the voltage feedback control circuit. The impedance of the filter should be low at frequencies that are within the control bandwidth but it should be high at the switching frequency. The turnover frequency of the filter in this design is 85 kHz.

S1 permits the input rectifier stage to be connected as a full-wave bridge rectifier for 240 V operation or in the doubler configuration for 120 V (or 110 V) operation. C12 and C13 provide dc smoothing. Due to the poor form factor of the input current with this simple form of smoothing a choke input filter should be considered if the design is extrapolated to higher power levels. As it is, C12 and C13 operate comfortably within their ripple current ratings.

Current Regulator Stage

Current regulation is performed by Q6 and Q7. A single IRF730 could adequately handle the full load current. The use of a second IRF730 cuts the full-load losses by 3 Watts. Alternatively, Q6 and Q7 could be replaced by a single IRF740.

Diode D9 carries the freewheeling load current during the period when Q6 and Q7 are off. This should be a fast-recovery type (trr $<$ 50 nS) to keep switching losses low.

The required value of L2 may be determined by first calculating the inductance that would be required on the secondary side of T5 and then referring this value to the primary side of T5 by multiplying by the square of the turns ratio of T5. The number of turns in L2 may be determined from the required inductance and the load current in accordance with the manufacturer's data. Attention should be paid to the parallel capacitance of the inductor. Non-adjacent layers in series will keep this to a minimum.

The ripple current in the filter capacitor is given by:

$$\Delta I = \frac{Vo}{L}(1-\delta)$$

and the minimum current for continuous conduction will be:

$$Io_{min} = \frac{Vo\,(1-\delta)\,T}{2L}$$

When the load current falls below this level the loop gain of the control circuit increases greatly tending to produce instability at light loads. The output ripple voltage is given by:

$$\Delta V = \frac{Vo}{2L}\left\{\frac{ESR^2 \cdot C}{\delta} + \frac{(1-\delta)\,T^2}{4C}\right\}$$

The values chosen for L2 and C16 represent a compromise between the need to keep the voltage ripple small and the practical difficulties of obtaining a capacitor of the required value with acceptable values of ESR and ripple current rating. The filter corner frequency and transient response of the supply are other factors which impinge on the choice of these components.

The Inverter Stage

Q8 and Q14 to Q17 conduct at the same time with a 50% duty cycle. Q9 and Q10 to Q13 conduct in anti-phase. The gates of Q8 to Q17 are driven from transformer T3. Because of the capacitive load on T3 the primary current waveform includes high current peaks. HEXDIPs are an ideal choice for the transformer drive transistors since they can handle the current pulses and the intrinsic body-drain diodes provide a clamp for the primary winding of the transformer on power-down.

The design of T5 is conservative. The primaries are not bifilar wound because of insulation requirements. The secondary is wound from Litz wire. Strip conductor could be used although the center tap connection may be less simple to implement than with Litz wire.

The voltage at the center tap of the primary winding is always less than half the dc link voltage since the duty cycle of the current regulator is never greater than 50%. By transformer action the voltage impressed on Q8 and Q9 is twice the center tap voltage. Therefore Q8 and Q9 under ideal conditions would not experience a voltage greater than the dc link voltage. However leakage inductance in T5 gives rise to voltage spikes at the drains of Q8 and Q9 and these need to be suppressed either with a snubbers or, as in this design, by use of a voltage clipper. Diodes D10 and D11 conduct when the voltage at the drains of Q8 or Q9 rises above the dc link voltage. The use of diode clippers ensures maximum efficiency since the energy stored in the transformer leakage inductance is returned to the dc link. When the gate signals are removed from Q6 to Q17 on power-down, D10 and D11 provide a safe discharge path for the energy trapped in T5.

The Control Circuit

This is based on the widely used 3526 integrated circuit. The 3526 is referenced to the output ground, isolation being preserved by T1, T2, T3 and T4. T2 and T3 are wound on torroidal cores to achieve lower leakage reactance than that readily obtainable with E-cores.

Stabilization of the supply is achieved in the conventional manner. The output filter and load (assumed resistive) have two poles, and a zero due to the ESR of the smoothing capacitor. The transfer function of the filter is given by:

$$\frac{Vo\,(s)}{Vsec\,(s)} = \frac{(s \cdot C \cdot ESR + 1)}{s^2LC(R+ESR)/R + s(L/R + C \cdot ESR) + 1}$$

Thus the phase shift can approach 180 degrees resulting in instability of the control loop. This is overcome by adding phase advance with two zeros in the error amplifier. The two-zero amplifier must have two poles, one at the origin to give good regulation and one to roll off the gain so that it is small at the switching frequency. This is necessary since the Pulsed Width Modulation is a source of delay in the control loop and therefore adds further poles near and beyond the switching frequency. In practice the slew rate of the operational amplifier will also limit the high-frequency gain. The gain of the error amplifier is given by:

$$g(s) = \frac{(s+1/C_2R_2)(s+1/C_2R_1)}{s(s+(C_2R_1+C_2R_3)/C_1C_2R_1R_3)} \cdot \left[\frac{R_2}{R_3}\right]$$

The gain of the power circuit can either be measured, or calculated from the proportionate change in duty cycle at pin 3, the link voltage and the turns ratio of T5.

Figure 3 shows the Bode plot for the power supply obtained from a computer model.

Performance

The efficiency of the supply is 90.7% at 20% load but falls to 86% at full load. About 18 Watts are dissipated in the synchronous rectifier under full-load conditions. The IRFZ44s used in the synchronous rectifier are rated at 50 Amps but carry an average current of only 6.25 Amps at full load in this application. Therefore even with a modest heat sink quite low junction temperatures may be expected. 18 Watts of rectifier losses at 50 Amps equate to an individual Rds(on) for the IRFZ44s of 0.028 Ohms indicating a HEXFET junction temperature of approximately 75 degrees C for typical devices.

If a Schottky diode rectifier were used, as shown in Figure 4, the rectifier losses would be considerably higher. The average current carried by each diode would be 25 Amps with a 180 degree conduction period. An International Rectifier 50HQ Schottky diode is rated at 50 Amps average and thus would be lightly loaded in this application. The 50HQ has a typical forward voltage drop of 0.6 Volts at an instantaneous current of 50 Amps and a junction temperature of 100 degrees C. Therefore rectifier losses would be approximately 30 Watts using Schottky diodes.

The synchronous rectifier losses may be reduced further at the cost of increasing the number of HEXFETs employed. Whether or not the extra cost is justified will depend on the importance given to minimizing losses. As the design output voltage is reduced the forward voltage drop in the rectifier assumes a greater significance, so that while Schottky diodes are likely to continue to predominate in 5 Volt supplies, synchronous rectification is likely to become a popular technique for lower voltage supplies.

Note

This design is given as an illustration of ways in which International Rectifiers HEXFETs may be used in power supplies and should be viewed as a source of ideas rather than a guaranteed formula for a successful design. Since the performance of a power supply of this kind is dependent on such factors as layout and transformer construction, the performance data quoted here must be regarded only as a guide to what may be achieved. □

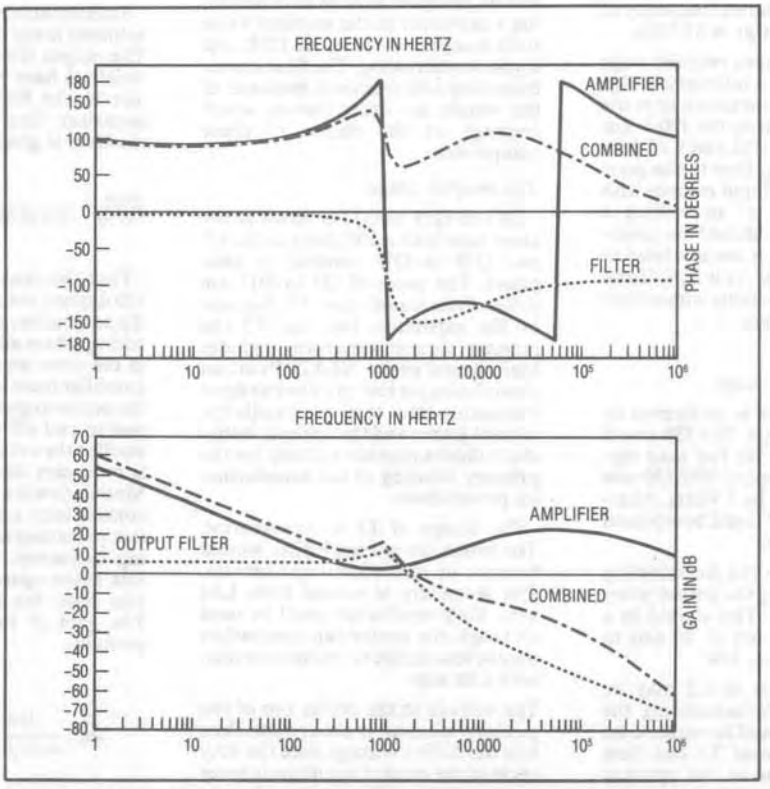


Figure 3. Bode Plot of Control Loop