1.5 MHZ CURRENT MODE IC CONTROLLED 50 WATT POWER SUPPLY

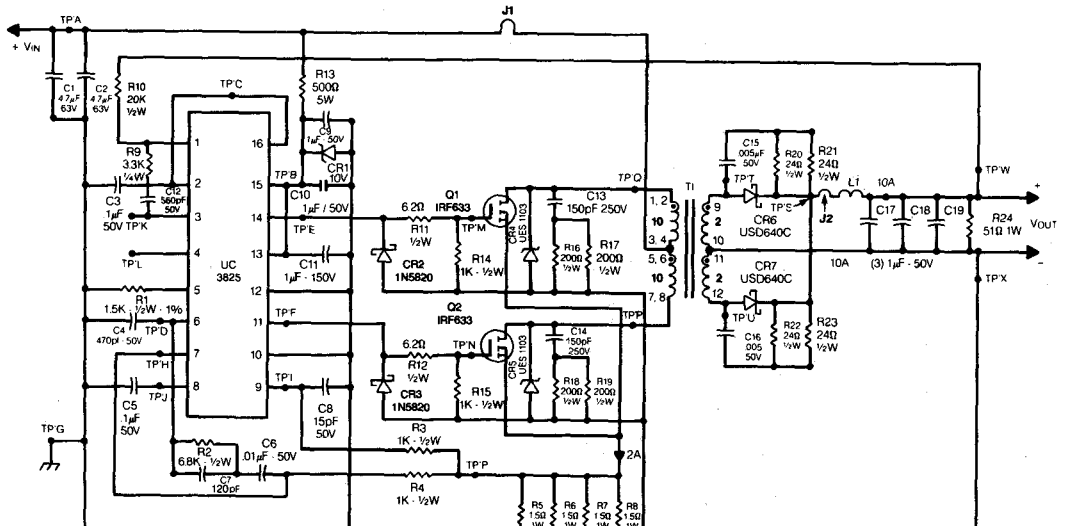
Abstract

This application note highlights the development of a 1.5 megahertz current mode IC controlled, 50 watt power supply. Push-pull topology is utilized for this DC to DC converter application of +48 volts input to +5 volts at 10 amps output. The beneficial increase in switching speed and dynamic performance is made possible by a new pulse width modulator, the Unitrode UC3825. Reductions in magnetic component sizes are realized and the selections of core geometry, ferrite material and flux density are discussed. The effects of power losses throughout the circuit on overall efficiency are also analyzed.

Introduction

The switching frequencies of power supplies have been steadily increasing since the advent of cost effective MOSFETS, used to replace the conventional bipolar devices. While the transition time in going from twenty to hundreds of kilohertz has been brief, few designers have ventured into, or beyond, the one megahertz benchmark. Until recently, those who have, had utilized discrete pulse width modulation designs due to the absence of an integrated circuit truely built for high speed. The 1.5 MHZ power supply shown schematically in figure 1 was designed to exemplify high frequency power conversion under the supervision of such an IC controller, the UC3825.

Figure 1. Schematic Diagram



II. POWER SUPPLY SPECIFICATIONS

Input Voltage Range:	42 to 56 VDC
Switching Frequency:	1.5 MHz
Output Power:	51 Watts Max.
Output Voltage:	5.1 VDC Nom.
Output Current:	2–10 ADC
Line Regulation:	5 MV
Load Regulation:	15 MV
Output Ripple:	100 MV Typ.
Efficiency:	75% Typ.

III. OPERATING PRINCIPLES

Power can efficiently be converted using any of several standard topologies. Design tradeoffs of cost, size and performance will generally narrow the field to one that is most appropriate. For this demonstration application, the center-tapped push-pull configuration has been selected.

Current mode control provides numerous advantages over conventional duty cycle control, and has been implemented as the regulation method. In review, the error amplifier output (outer control loop) defines the level at which the primary current

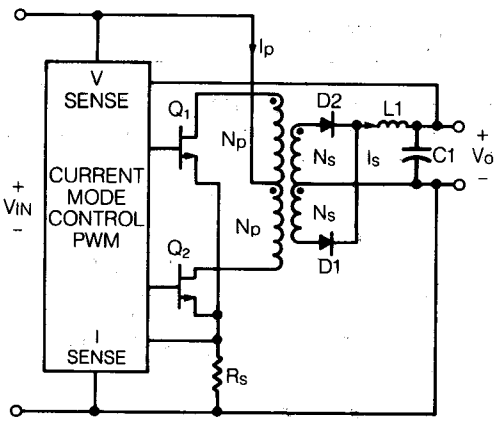


Figure 2. Basic Diagram — Push-Pull Converter Using Current Mode Control

(inner loop) will regulate the pulse width, and output voltage. Pulse-by-pulse symmetry correction (flux balancing) is inherent to current mode controllers, and essential for the push-pull topology to prevent core saturation.

A basic current mode controlled, mosfet switched push-pull converter is shown in figure 2. Transistor Q1 is turned on by a drive pulse from the PWM, causing primary current I_p to flow through the transformer primary, mosfet Q1 and sense resistor R_s. Simultaneously, diode D1 conducts current $I_p \times N_p/N_s$ in the secondary, storing energy in inductor L1 and delivering power to the output load. When Q1 receives a turn-off pulse from the PWM, it halts the current flow in the primary. Secondary current continues due to the filter inductor L1. Diodes D1 and D2 each conduct one-half the DC output current during these converter "off" times. This entire process is repeated on alternate cycles, as Q2 next is toggled on and off. The basic waveforms are shown in figure 3 for reference.

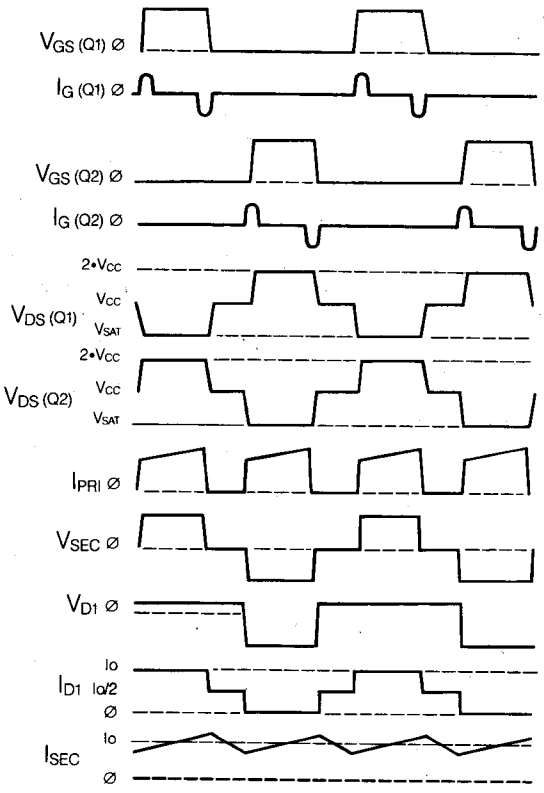


Figure 3. Basic Push-Pull Waveforms

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IV. DESIGN CONSIDERATIONS

Auxiliary Supply Voltage

The 9.2 volt minimum requirement of the UC3825 and 20 volt gate-source maximum of the mosfets imply an approximate 10 thru 18 volt range of inputs. The 10 volt value was selected to supply both V_{CC} and V_C (totem pole outputs) while keeping power dissipation in the IC low. The circuit used is a simple resistor-zener dissipative network with ample bypassing capacitors located near the IC to reduce noise.

Oscillator Frequency

The oscillator frequency selected is 1.5 MHz, resulting in a 670 nanosecond period. From the UC3825 data sheet, oscillator frequency versus R_t, C_t, and deadtime curves:

F_o = 1.5 mHz; T period = 670 ns
C_t = 470 pF
R_t = 1.5 K

Therefore; T (on) = 570 ns (max)
T (off) = 100 ns (min)

$$\text{DUTY CYCLE, d max} = \frac{\text{T (on) max}}{\text{T (period)}} = \frac{570\text{ ns}}{670\text{ ns}} = 85\%$$

NOTE: These times will determine the mosfet device selection and transformer turns ratio.

Preliminary Considerations

Prior to designing the main transformer, several parameters need to be defined and determined. Standard design procedures are used for this "first cut" approximation.

Input Power

$$\text{Input power, P (in)} = \frac{\text{Output power, P (out)}}{\text{Efficiency, n}}$$

Let n = 75% for a 5 v, single output power supply.

$$\text{P (in)} = \frac{5.1\text{ v} \cdot 10\text{ a}}{0.75} = \frac{51\text{ watts}}{0.75} = 68\text{ watts}$$

Primary Current

The primary current can be approximated using the low-line constraints of 42 volts DC input:

$$\text{Primary Current (dc)} = \frac{\text{Input power P (in)}}{\text{Input voltage V (in)}} = \frac{68\text{ watts}}{42\text{ volts}} = 1.62\text{ A}$$

The primary current during the transistor on time is:

$$\text{I (p)} = \frac{\text{I (dc)}}{\text{d (max)}} = \frac{1.62\text{ A}}{0.85} = 1.9\text{ amps, or approx. 2A}$$

The RMS primary current is:

$$\text{Ip (rms)} = \text{Ip}\sqrt{\text{duty}} = 1.24\text{A (rms)}$$

Sense Resistor R (s)

Primary current is sensed and controlled in a current mode controller by first developing a voltage proportional to the primary current, used as an input to UC3825. This is accomplished by sense resistor R (s) with a calculated value of the I limit threshold value divided by the primary current at the desired current limit point, typically 120% I (max).

$$\text{R (s)} \leq \frac{\text{V th (pin 9)}}{120\% \cdot \text{I (pri)}} = \frac{1\text{ volt}}{1.2 \cdot 2\text{ amps}} = 0.42\text{ ohm}$$

Mosfet DC Losses

A high quality mosfet is used to keep both DC and switching losses low, with an R (ds) on max of 0.8 ohms. Calculation of the voltage drops across the device are required for the transformer design.

V ds (on) = Rds (max) • I (p) = 0.8 • 2 = 1.6 v

During an overload; V ds (max) = 0.8 • 2 • 1.20 = 1.92 v (2 v)

P dc = I dc² Rds max • duty
= 2² • 0.8 • 0.85/2 = 1.35 watts

Selection of Core Material

Few manufacturers provide core loss curves for frequencies above 500 khz. To minimize power dissipation in the core, the flux density must be drastically reduced in comparison to the 20 -150 khz versions. Typical operation is at a total flux density swing, delta B, of 0.030 Tesla (300 Gauss) while approaching the 1 megahertz region. TDK's H7C4 material was selected for it's low loss, high frequency characteristics.

Main Transformer Design

The first step in transformer design is to determine the preliminary turns ratio. Once obtained, the minimum cross-sectional area core (Ae) can be calculated, and core selection made possible.

Calculation of Transformer Voltages and Turns Ratio

V pri (min) = V in (min) - V xtor (max) - V (Rs) max
V p (min) = 42 v - 2.0 v - 1 v
= 39.0 v

V sec (min) = V out (max) + V diode (max)
+ V choke (dc) + V (losses)
V sec (min) = 5.1 + 0.65 + 0.1 + 0.05 (est) = 5.9 v

$$\text{Turns ratio N} = \frac{\text{V pri (min) Duty (max)}}{\text{V sec (min)}} = \frac{39.0 \cdot 0.85}{5.9} = 5.6{:}1$$

The secondary is designed for excellent coupling using copper foil, and the primary has been rounded to the nearest lower turns.

Turns ratio: N = N pri / N sec = 5:1

The actual number of both primary and secondary turns will be determined by the ferrite core characteristics as a function of operating frequency and Gauss level.

Minimum Core Size

The minimum cross-sectional area core that can be used is calculated with the following equation for core loss limited applications.

$$Ac\ (min) = \frac{V\ (pri)\ min \bullet Duty\ (max) \bullet 10^4}{2 \bullet Freq. \bullet N\ (p) \bullet \Delta B\ (Tesla)}\ (cm^2)$$

At first it would seem that the core area required for this 1.5 MHZ switcher would be ten times smaller than that of a 150 KHZ version. This would be true if the flux density, number of turns and core losses remained constant. However, losses are a function of both frequency and frequency squared[2] and as it increases, the flux density swing (ΔB) must be drastically reduced to provide a similar core loss, hence temperature rise. In this example, an acceptable figure was selected of one percent of the total output power, or one-half watt. Empirically, this translates to a temperature rise of 25°C, at 325 Gauss (0.0325 Tesla) for cores with a cross-sectional area of 0.70 sq. cm, a ballpark estimate of the true core size.

This formula can be rewritten as:

$$Ac \bullet Np = \frac{V\ pri \bullet D\ max \bullet 10^4}{2 \bullet F \bullet \Delta B}$$

This is a more convenient formula because the right hand side of the equation contains all constants. Input voltage, frequency of operation and flux density have already been determined. The selection of core size (cross-sectional area) is inversely proportional to the number of primary turns, and vice-versa. Based on the five-to-one turns ratio, an original assumption of five turns for the primary would result in a large core size for this 50 watt application. Alternatively, a ten turn primary is used to minimize core size.

Substituting previous values for high line operation at 0.0325 Tesla (325 Gauss) and a magnetic operating frequency of 750 kHz:

$$Ac\ (min) = \frac{39 \bullet 0.85 \bullet 10^4}{2 \bullet 750{,}000 \bullet 10 \bullet 0.0325} = 0.68\ cm^2$$

Core Loss Limited Conditions

As the switching frequencies are increased, generally a reduction of core size or minimum number of turns is realized. This is true, however, but only to the point at which the increasing core losses prevent a further reduction of either size or minimum turns. This crossover point occurs at different frequencies for each individual ferrite material based upon their losses and acceptable circuit losses, or temperature rise[3]

Core Geometry Selection

A variety of standard core shapes are available in the cross-sectional area range of 0.62 to 0.84 cm^2. Considerations of safety agency spacing requirements, physical dimensions, window area and relative cost of assembly must be evaluated.

Core Style	Description	AC (cm^2)	Weight (g)
PQ	PQ 20/20	0.62	15
POT CORE	P 22/13	0.63	13
LP	LP 22/13	0.68	21
TOROID	T 28/13	0.76	26
EE	EE 35/28	0.78	28

The LP 22/13 style was selected to easily terminate (breakout) the high current output windings. For a given cross-sectional area, it occupies less PC board space, and has good shielding characteristics.

Wire Size Selection

The single, most difficult task in high frequency magnetic design is to minimize the eddy current losses, or skin effects while optimizing wire sizes. Penetration depth refers to the thickness (or depth) into a copper conductor in which a wave will penetrate for a specific frequency. For copper at 100°C:

$$d\ pen = 7.5 / (frequency^{0.5})\ (cm)$$

At 750 kHz, this corresponds to $8.66 \bullet 10^3$ cm, or about the thickness of an AWG #39 wire. Larger size wire can be used, however the AC current flows only in the depth penetrated at the switching frequency. Consult the UNITRODE DESIGN SEMINAR SEM-400 book, appendix M2 for additional information on this subject.

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For low current windings, several strands of thin wire can be paralleled, or twisted together forming a "bundle." Seven wires twisted around each other closely approximate a round conductor with a net diameter of three times the individual wire diameter. This twisting is commonly done at 10-12 turns per foot, and significantly reduces parasitics between wires at high frequencies.

Medium to high current windings require the use of Litz wire, a similar bundle of numerous conductors. Copper foil is also an excellent choice.

Industry practice is to operate at 450 amps (RMS) per centimeter squared, or $2.22 \cdot 10^{-3}$ cm²/A. This applies to windings operating at an acceptable temperature rise.

Area required = I rms / 450A / cm²

Primary area (Axp) = 1.24A / 450A / cm² = $2.75 \cdot 10^{-3}$ cm²

Calculate Secondary RMS Current.

$$I\,rms\,(sec) = \frac{I\,sec^2\,(duty\ on) + \frac{I\,sec^2}{2}\,(2 \cdot duty\ off)}{2}$$

$$I\,rms\,(sec) = \frac{10^2\,(.425) + \frac{5^2}{2}\,(2 \cdot .075)}{2}$$

$$I\,rms\,(sec) = 4.81A$$

Secondary Area (Axs) = 4.81A / 450A / cm²
= $1.07 \cdot 10^{-2}$ cm²

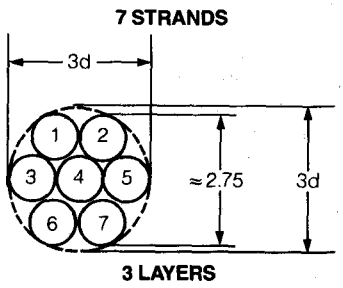

Figure 4.

For a given bundle of 7 conductors, the cross-sectional area of each conductor equals:

$$\frac{\text{Required area}}{\#\ \text{conductors}} = \frac{\text{Axp}}{7} = \frac{2.75 \cdot 10^{-3}}{7} = 3.93 \cdot 10^{-4}\ \text{cm}^2$$

The cross-sectional area of an AWG #36 wire is $1.32 \cdot 10^{-4}$, therefore, three bundles of seven conductors each should be used. Two bundles were utilized as a compromise between practical winding considerations and acceptable eddy current losses.

Copper foil is used for the secondary, with a required width slightly less than the bobbin width, and thickness determined by:

$$\frac{\text{Secondary area (Axs)}}{\text{Bobbin width}} = \frac{1.07 \cdot 10^{-2}\ \text{cm}}{1.40\ \text{cm}} = 7.64 \cdot 10^{-3}\ \text{cm}$$

This corresponds to 0.003" thick foil, a standard value. In practice, slightly thicker foil (0.004" to 0.005") may be required to minimize power losses in the transformer.

Transformer Assembly

Standard practice to increase coupling between primary and secondary is position both as closely as possible to each other inside the transformer. In this design, the first layer wound is one primary, and the next layer is the corresponding secondary. This is again followed by the other secondary and primary. It is important to keep the secondaries in close proximity since both will be conducting simultaneously twice per period. The primaries do not conduct in this manner, so coupling from primary A to primary B is not critical, only primary A to secondary C, and primary B to secondary D.

Referring to the transformer schematic, primary A is wound closest to the bobbin. After insulation, secondaries C and D are wound bifilar and insulated. Primary B is wound last, then terminated so that primaries A and B are wired in series, likewise for secondaries C and D.

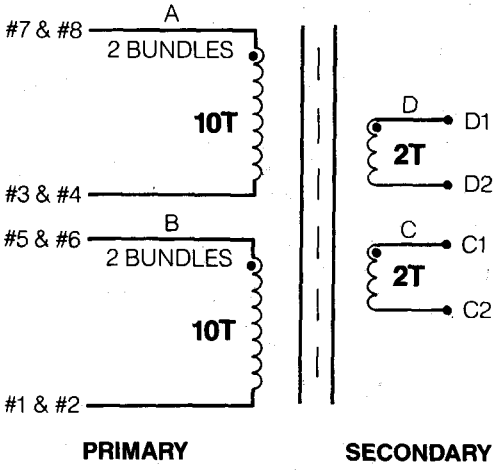

Figure 5. Transformer Schematic

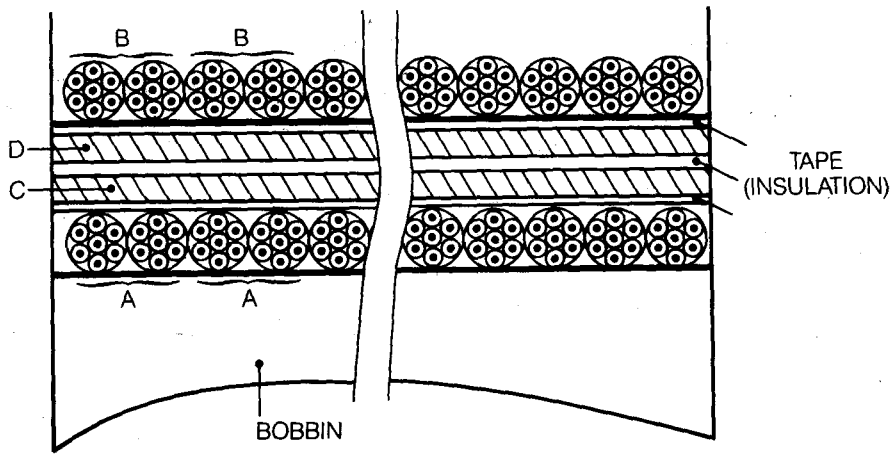

Figure 6. Transformer — Exploded View

Calculation of Winding Resistances and Losses

The mean length of turn for the bobbin can be determined from the specifications of O.D. and I.D., and for the BLP 22/13 a figure of 4.51 cm or 1.77 in. was obtained. AWG #36 wire has a resistance of $1.82 \cdot 10^{-2}$ ohms/cm at 100°C for the following:

Primary resistance can be calculated:

$$R_{pri} = \frac{R_{wire} \cdot M.L.T. \cdot \#\,turns}{\#\,wires} = \frac{0.0182 \cdot 4.51 \cdot 10}{14} = 0.0586 \text{ ohm}$$

Voltage drop and power loss in each half winding can be also calculated:

$V(R_{pri}) = I_{pri} \cdot R_{pri} = 2.0 \cdot 0.58 = 0.116$ volt (negligible)

$P(R_{pri}) = R_{pri} \cdot I_{pri}^2 \cdot duty = 0.0586 \cdot 4 \cdot 0.425$
$= 0.0996$ watts

The resistance of the secondary can be approximated by using the wire tables, and substituting the foil for wire of similar cross-sectional area. In this example, AWG #16 wire is used to obtain Rsec $= 1.58 \cdot 10^{-4}$ ohms/cm.

$R_{sec} = R_{foil} \cdot M.L.T. \cdot \#\,turns = 1.58 \cdot 10^{-4} \cdot 4.5 \cdot 2$
$= 0.00143$ ohm

$V(R_{sec}) = 1.43 \cdot 10^{-3} \cdot 10 = 0.0143$ volt (negligible)

$P(R_{sec}) = R_{sec}\,((I_{dc}^2 \cdot D\,on) + ((I_{dc}/2)^2 \cdot 2 \cdot D\,off))$

$P(R_{sec}) = 0.00143\,((10^2 \cdot 0.425) + (5^2 \cdot 0.15) =$
0.066 watts

Transformer Power Losses

The total copper losses for two windings are then:

$P_{cu} = P(R_{pri}) + P(R_{sec}) = 2 \cdot (0.066 + 0.0996)$
$= 0.332$ watts

Estimated eddy current losses are approximately 50% of the copper losses. $P_{cu} \approx 0.50$ watts.

Given the core material type, geometry, frequency and operating Gauss level, the ferrite losses can be calculated. From the manufacturers information, the typical loss coefficient for H7C4 material operating at a flux density swing of 0.035 Tesla (350 Gauss) at 750 kHz is 0.15 watts per cubic centimeter of core volume, which is 3.327 cm^3 per LP 22/13 core set. Therefore:

$P_{core} = 3.327 \cdot 0.15 = 0.50$ watt

The total power lost is a summation of the copper and ferrite losses:

$P_{xfmr} = P_{cu} + P_{core} = 0.50 + 0.50 = 1.00$ watts

OUTPUT SECTION

Output Choke Calculations

Typically, the RMS output ripple current is less than 15% I dc, or 1.5 amps in this case. Delta I, the peak to peak ripple therefore is twice the RMS, or 3 amps.

$$V = \frac{L\,di}{dt} \therefore L = \frac{V\,dt}{di} = \frac{5.9\text{ v } (350)\ 10^{-9}\text{ s}}{3.0\text{ A}} = 690 \text{ nanohenries}$$

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Due to the small value of inductance required, the conventional approach will not be used. Instead, a simple RF type wound coil will be designed using the solenoid equation found in most reference texts. A thick pencil will be utilized as the coil form with a diameter of 0.425 inches, however any similar item will suffice.

The form factor, F, is a function of the form diameter divided by the length of the wound coil, or D/L. A few gyrations will take place before the exact values are obtained, however this goes quickly. The form factor is listed below for various practical values of D/L.

Coil Dia./Length	Form Factor "F"
0.1	0.0025
0.25	0.0054
0.50	0.010
1.0	0.0173
2.0	0.026
5.0	0.040

$L\ (\mu H) = F \cdot N^2 \cdot D\ (in)$, $N = (L/F \cdot D)^{1/2}$ (turns)

For D = 0.425, D/L = 1 (approx); F = 0.0173

$N = (0.690 / 0.0173 \cdot 0.425)^{1/2} = 9.76$ turns

Rounding off to the nearest next number of turns, the actual inductance for 10 turns can be calculated:

$L\ (\mu h) = 0.0173 \cdot 10^2 \cdot 0.425 = 744$ nanohenries

In an air core inductor the permeability "u" equals unity, therefore the flux density B equals the driving function H.

Output Capacitor

$$Q = \frac{I\ p\text{-}p}{2} \cdot \frac{T\ period}{2} \cdot \frac{I}{2}, \quad \text{Delta } Q = I\ p\text{-}p / 8 \cdot F$$

C = Q / dV where dV (output ripple) equals 0.100 volts.

$C = I\ p\text{-}p / 8 \cdot F \cdot dV = 3 / 8 \cdot 1.5 \cdot 10^6 \cdot 0.10 \approx 2.5\ \mu F$

Three 1 μf caps are used in parallel. With a typical ripple voltage of <50 mv due to ESR, the ESR each (at 1.5 mHz) must be approximately 150 milliohms. The Unitrode ceramic monolithic capacitor series was selected for their excellent high frequency characteristics.

Resonance, and its effect at these frequencies must be taken into account. In this case, the capacitor reaches resonance at 1.5 mHz, and the effective impedance is resistive.

Output Diodes

Schottky diodes were selected for their short reverse recovery times to minimize switching losses, and low forward drop for high DC efficiency. The Unitrode USD 640C is a center-tapped TO-220 type, with ample margin to safely accommodate 40 volt reverse transients and 10 amp DC output currents. Also featured is a 0.65 volt maximum drop across each diode and 1 volt per nanosecond switching rate.

UC3825 PWM CONTROL SECTION

Current Limit / Shutdown

Pulse-by-pulse current limiting is performed by the UC3825 by an input of the primary current waveform to the IC at pin 9. The small RC network of R3 and C8 are used to suppress the leading edge glitch caused by turn-on of the mosfet and transformer parasitics. The input must be below the 1 volt threshold or current limiting will occur. Once reached, an input above the threshold will narrow the pulse width accordingly. When this reaches a 1.4 volts amplitude, shutdown of the outputs will occur, and the UC3825 will initiate a soft start routine.

Ramp

The UC3825 offers the flexibility of both Current Mode Control or conventional duty cycle control via the RAMP input pin. When connected to the timing capacitor, the UC3825 operates as a duty cycle control IC. Connecting the RAMP input to the current waveform changes the control method to Current Mode. In this application, the ramp waveform is tied through a small RC filter network to the primary current waveform. This network is defined in the next section — slope compensation. The dynamic range of this input is 1-3 volts, and is generally used for introducing slope compensation to the PWM.

Slope Compensation

Slope compensation is required to compensate for the peak to average differences in primary current as a function of pulse width. Adding a minimum of 50% of the reflected downslope of the output current waveform to the primary current is required. See UNITRODE APPLICATION NOTE U-93 and U-97 for further information. Empirically, 60-75% should be used to accommodate circuit tolerances and increase stability[5]

Resistors R2 and R4 in this circuit form a voltage divider from the oscillator output to the RAMP input, superimposing the slope compensation on the primary current waveform. Capacitor C6 is an AC coupling capacitor, and allows the 1.8 volt swing of the oscillator to be used without adding offset circuitry. Capacitor C7 has a two-fold purpose. During turn on it filters the leading edge noise of the current waveform, and provides a negative going pulse across R4 to the ramp input at the end of each cycle. This overrides any parasitic capacitance at the ramp input, (pin 7), that would tend to hold it above zero volts. This insures the proper voltage input at the beginning of the next cycle.

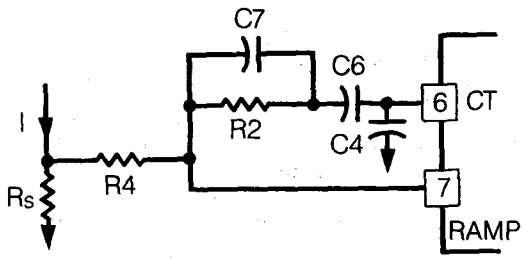

Figure 7.

For the purposes of determining the resistor values, capacitors C4 (timing), C6 (ac coupling) and C7 (filtering) can be removed from the circuit schematic. The simplified model represented in figure 8 is used for the calculations. These calculations can be applied to all Current Mode circuits using a similar scheme.

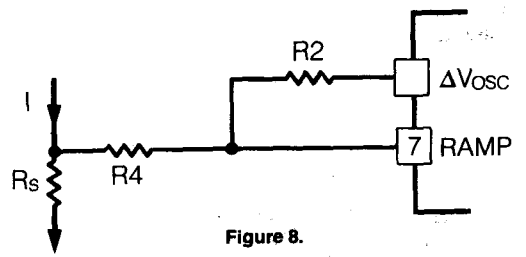

Figure 8.

STEP 1. Calculate Inductor Downslope
$S(L) = di/dt = V\,sec / L = 5.9\,V / .740\,\mu H = 8.0\,A/\mu s$ (1)

STEP 2. Calculate Reflected Downslope to Primary
$S(L)' = S(L) / N\,(turns\ ratio) = 8.0/5 = 1.6\,A/\mu S$ (2)

STEP 3. Calculate Equivalent Ramp Downslope Voltage
$V\,S(L)' = S(L)' \cdot Rsense = 1.6 \cdot 0.375 = 0.600\,V/\mu s$ (3)

STEP 4. Calculate Oscillator Slope
$V\,S\,(osc) = d\,(V\,osc) / T\,on = 1.8\,V / 570\,ns = 3.15\,V/\mu s$ (4)

STEP 5. Generate the Ramp Equations
Using superposition, the circuit can be configured as:

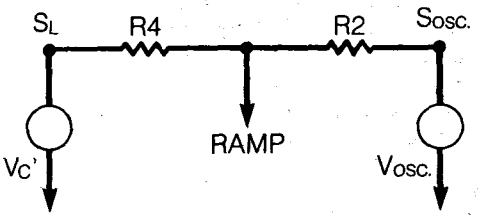

Figure 9.

$$V\,(ramp) = \frac{V\,S\,(L)' \cdot R2}{R2 + R4} = \frac{V\,S\,(osc) \cdot R4}{R2 + R4} \quad (5)$$

SUBSTITUTING,
$$V\,(ramp) = V\,S\,(L)'' + V\,S\,(comp) \quad (6)$$

WHERE
$$V\,S\,(comp) = \frac{V\,S\,(osc) \cdot R4}{R2 + R4}; \quad V\,S\,(L)'' = \frac{V\,S\,(L)' \cdot R2}{R2 + R4}$$

STEP 6. Calculate Slope Compensation
$$V\,S\,(comp) = m \cdot S(L)'' \quad (7)$$

Where m equals the amount of inductor downslope to be introduced. In this example, let m = 75%, or 0.75.

$$\frac{V\,S\,(osc) \cdot R4}{R2 + R4} = \frac{m \cdot V\,S(L)' \cdot R2}{R2 + R4}$$

SOLVING FOR R2:
$$R2 = R4 \cdot \frac{V\,S\,(osc)}{V\,S\,(L)' \cdot m} = R4 \cdot \frac{3.15}{0.600 \cdot 0.75} \quad (9)$$

USING CIRCUIT VALUES,
$R2 = 7.05 \cdot R4$

For simplicity, let R4 equal 1 K ohms and R2 therefore equals 7.05 K. Using the nearest standard value resistor of 6.8 K, the exact amount of downslope is minimally affected. Important, however, is that the series combination of R2 and R4 is high enough in resistance not to load down the oscillator and cause frequency shifting.

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CLOSING THE FEEDBACK LOOP

Error Amplifier

Compensation of the high gain error amplifier in the UC3825 is straight forward. There is a single-pole at approximately 5 hertz. A zero will be introduced in the compensation network to provide gain once the zero db threshold is crossed. Using Current Mode control greatly simplifies the compensation task as the output choke is controlled by the inner current loop, thus making the output section appear as a single pole response with a zero at the ESR frequency[4]

Control to Output Gain

The control to output gain will vary with output loading, and as the load is increased the gain decreases. Output capacitor ESR will determine the frequency at which the zero occurs, thus changing the gain as a function of ESR. To insure stability through all combinations of load and ESR, the amplifier will be compensated to cross zero db at approximately one-fifth of the switching frequency with ample phase margin.

The output filter pole and zero occur at

$F_p = 1/2\,\pi\,R\,(load)\,C\,(output)$

$F_z = 1/2\,\pi\,R\,(esr)\,C\,(output)$

CIRCUIT PARAMETERS:

C (output) = 3 μF; ESR (each) = 0.050 min - 0.300 max

For three capacitors in parallel, ESR = 0.016 - 0.100 ohms

R (output) = 2.5 ohms at 2 A, 0.5 ohms at 10 A

Using the above equations;

$F_p\,(2A) = 1/(2 \cdot 3.14 \cdot 2.5 \cdot 3 \cdot 10^{-6}) = 21.2$ kHz

$F_p\,(10A) = 1/(2 \cdot 3.14 \cdot 0.5 \cdot 3 \cdot 10^{-6}) = 106.1$ kHz

$F_z\,(high) = 1/(2 \cdot 3.14 \cdot 0.016 \cdot 3 \cdot 10^{-6}) = 3.315$ mHz

$F_z\,(low) = 1/(2 \cdot 3.14 \cdot 0.100 \cdot 3 \cdot 10^{-6}) = 530.5$ kHz

GAIN

$$\frac{V\,(output)}{V\,(control)} = K \cdot R_o, \text{ where } K = \frac{Ipri \cdot N_p/N_s}{V\,(control)} = \frac{2 \cdot 5}{0.85} = 11.76$$

Therefore, at 2 amps and 10 amps,

$V_o/V_c = K \cdot ro = 11.76 \cdot 2.5 = 29.4$ db (2A)

$V_o/V_c = K \cdot ro + 11.76 \cdot 0.5 = 15.4$ db (10A)

Error Amplifier Compensation

The control to output gain can be plotted along with the desired zero db crossing point and an estimate of the error amplifier required compensation network can be made. The amp compensation should have a zero at approximately 100 kHz, and a gain of -16 db at this frequency. Resistor R9 has been selected to be 3.3 k ohms based on the output drive capability of the UC3825 amp. Complete specifications are contained in the UC3825 data sheet.

F zero (amp) = $1/(2 \cdot \pi \cdot R9 \cdot C12)$

therefore, $C12 = 1/(2 \cdot \pi \cdot R9 \cdot F\ zero)$

$C12 = 1/(2 \cdot 3.14 \cdot 3300 \cdot 100.000) = 480$ pF (use 560 pF)

R10 / R9 = approx -16 db (0.16),

R10 = R9 / gain = 3.3 K / 0.16 = 20.4 K (use 20 K)

This compensated response can now be plotted, along with the control to output gain and the overall power supply response is a summation of the two curves, as seen in figures 11 and 12. Low frequency gains of 100 db at full load, and 115 db at light load are obtained, with a zero db crossing at approx. 100 kHz for both. Phase margin is generous with approx. 90 degrees for both light and 45 degrees at full load.

GAIN AND PHASE RESPONSE
UC3825 DEMO KIT

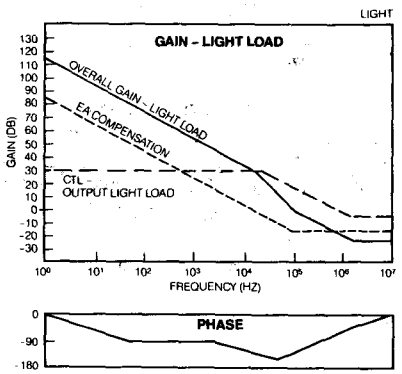

Figure 11.

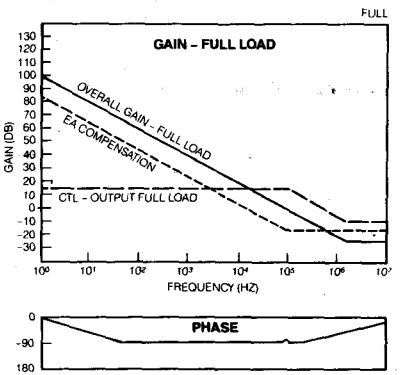

Figure 12.

LIST OF MATERIALS

REFERENCE	DESCRIPTION	
Capacitors		
C1, 2	4.7 μF, 63 VDC Electrolytic	
C3, 5	0.1 μF, 50 VDC Monolithic	
C4	470 pF, VDC Monolithic	
C6	0.01 μF, 50 VDC Monolithic	
C7	120 pF, 50 VDC Monolithic	
C8	15 pF, 50 VDC Monolithic	
C9-11, 17-19	1 μF, 50 VDC Monolithic	
C12	560 pF, 50 VDC Monolithic	
C13, 14	150 pF, 150 VDC Ceramic	
C15, 16	5000 pF, 50 VDC Ceramic	
Diodes		
CR1	1N4465	10 V, 1.5 Watt Zener
CR2, 3	USD1140	40 V, 1 Amp Schottky
CR4, 5	UES1105	150 V, 2.5 Amp Ultrafast
CR6, 7	USD640C	40 V, 12 Amp Schottky
Integrated Circuits		
U1	UC3825	Unitrode High Speed PWM
Transistors		
Q1, 2	UFN633	150 V, 8A Mosfet
Resistors		
R1	1.5 K, 1/2 W, 1%	
R2	6.8 K, 1/2 W, 5%	
R3, 4, 14, 15	1 K, 1/2 W, 5%	
R5-8	1.5 R, 1 W, 5%	
R9	3.3 K, 1/2 W, 5%	
R10	20 K, 1/2 W, 5%	
R11, 12	6.2 R, 1/2 W, 5%	
R13	500 R, 5 W, 10%	
R16-19	200 R, 1/2 W, 5%	
R20-23	24 R, 1/2 W, 5%	
R24	51 R, 1 W, 5%	
Magnetics		
L1	740 nH Wound Coil	
T1	AIE Magnetics Custom Transformer, 5:1 Turns Ratio	
Miscellaneous		
H1	Heatsink—Mosfets (AAALL #5786B)	
H2	Heatsink—Diodes (AAALL #5299B)	

Efficiency Measurements

V (In)	I (In)	P (In)	P (Loss)	Efficiency
42	1.707	71.7	20.2	71.8%
48	1.483	71.2	19.7	72.4%
56	1.331	73.2	21.7	70.4%

V (In) V	Vout (2A)	Vout (5A)	Vout (10A)	Load Reg. MV
42	5.110	5.102	5.093	17
48	5.108	5.101	5.092	16
56	5.108	5.102	5.089	19
Line	2 mv	1 mv	4 mv	

Dynamic Performance

The power supply was pulse loaded from 5 amps to 10 amps at a frequency of 100 kilohertz. Recovery to within 50 mv was less than 2 microseconds with a total excursion of less than 200 millivolts. High speed FETS were used to switch the load current with typical rise/fall times of 50 nanoseconds.

Short Circuit

The short circuit input current is approximately 0.75 amps, or an input power of 36 watts.

Circuit Power Losses

The total circuit losses are approximated using both the calculated and measured losses throughout the power supply.

Power Losses

Current Sense Circuit	1.2 W
Output Diodes	9.8 W
Switching Transistors	3.2 W
Dropping Resistor	3.0 W
Snubber Networks	1.0 W
Transformer Losses	1.0 W
Auxiliary Supply	0.8 W
Miscellaneous	0.2 W
TOTAL LOSSES	20.2 W

If a bootstrapped technique is utilized in the auxiliary supply to the IC and drive circuitry, the dropping resistor losses of three watts can be reduced to 0.1 watts in the bootstrap circuitry. In addition, the lossy resistive current sensing network can be replaced by a small current transformer, lowering the losses by a half-watt. Overall efficiency would then increase to 75%, fairly high for a five volt output application. Noteworthy is that the switching losses at this high of frequency can be minimized, and have little overall effect on circuit efficiency.

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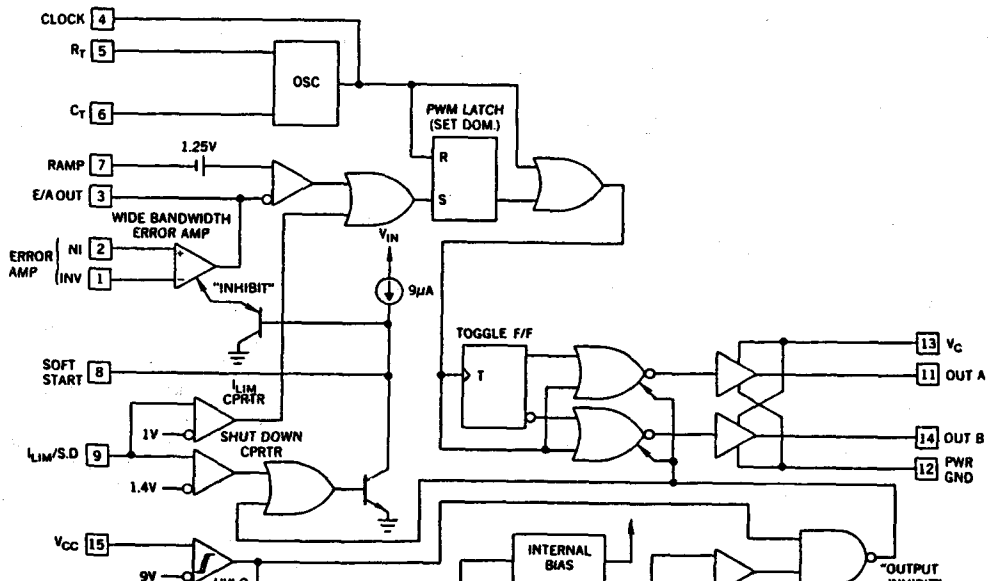
Summary

The demands of higher power densities will undoubtedly throttle many switch-mode power supply designs into and beyond the megahertz region in the near future. Designers will be facing the challenges of selecting switching devices, magnetic materials and IC controllers built exclusively for high efficiency at these frequencies. The thrust from contemporary hundreds of kilohertz designs to megahertz versions is rapidly making progress. This 1.5 MHZ current mode push-pull is an example of what can successfully be accomplished with existing high speed components and technology.

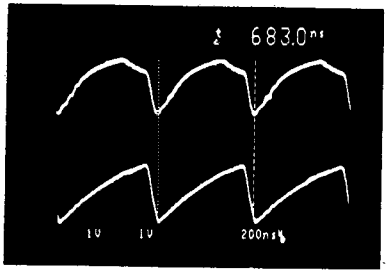
References

1. Woffard, Larry, — "New Pulse Width Modulator Chip Controls, MHZ Switchers" — U-107; Unitrode Applications Handbook 1987/88.
2. Dixon, Lloyd Jr. — "Eddy Current Losses" Section M2-4, Unitrode Power Supply Design Seminar Book, SEM-500.
3. Andreycak, Bill — "1.5 MHZ Current Mode IC Controlled 50 Watt Power Supply," Proceedings of the High Frequency Power Conversion Conference, 1986.
4. Dixon, Lloyd Jr. — "Closing the Feedback Loop" Section C1 — Unitrode Power Supply Design Seminar Book, SEM-500.
5. Andreycak, Bill "Practical Considerations in Current Mode Power Supplies" Topic 1 — Unitrode Power Supply Design Seminar Book, SEM-500.

UC3825 BLOCK DIAGRAM



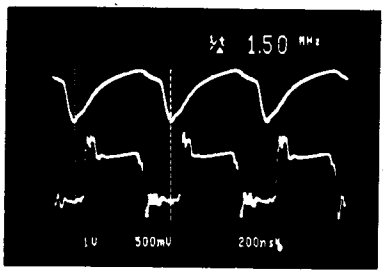
TIMING WAVEFORMS



Top Trace
Ramp Voltage
TP 'H', 1 v/cm

Bottom Trace
CT Waveform,
TP 'D', 1 v/cm

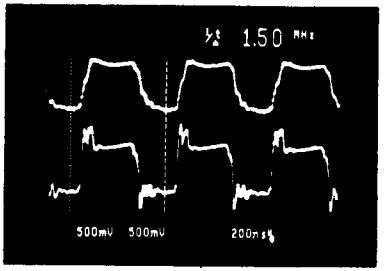
RAMP VOLTAGE



Top Trace
Filtered Ip with
Slope Compensation
TP 'H', 1 v/cm

Bottom Trace
Unfiltered Ip
TP 'P', .5 v/cm

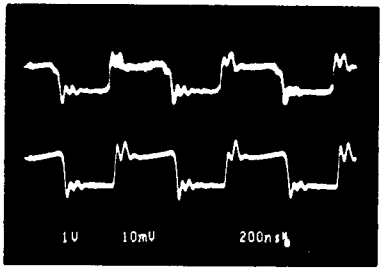
PRIMARY CURRENT



Top Trace
Filtered Ip
TP 'I', .5 v/cm

Bottom Trace
Unfiltered Ip
TP 'P', .5 v/cm

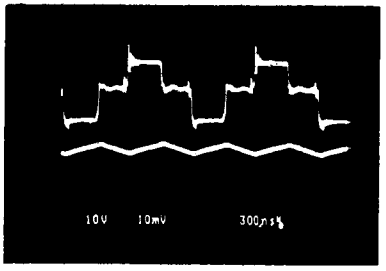
PRIMARY CURRENT



Top Trace
J1, 2 A/cm

Bottom Trace
TP 'P', 1 v/cm

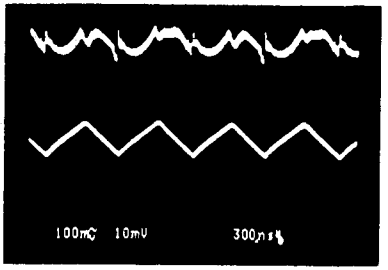
SECONDARY WAVEFORMS



Top Trace
Secondary Voltage
TP 'T', 10 v/cm

Bottom Trace
Secondary Current
J2, 5 A/cm

OUTPUT WAVEFORMS



Top Trace
Output Voltage
Ripple & Noise
TP 'W', 100 mv/cm

Bottom Trace
AC Output Current
J2, 2 A/cm

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