Stability analysis of low-dropout linear regulators with a PMOS pass element

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Low-dropout linear regulators (LDOs) have gained popularity with the growth of battery-powered equipment. Portable electronic equipment including cellular telephones, laptop computers and a variety of handheld electronic devices has increased the need for efficient voltage regulation to prolong battery life. Texas Instruments offers several LDO products designed with PMOS pass transistors with very low dropout voltage. Compared to the NPN linear regulator, the LDO regulator can control its output voltage with much less headroom. The NPN regulator requires about 2 V of headroom while the LDO requires less than half a volt.

Some vendors offer LDO linear regulators designed with PNP pass transistors. For these regulators, the base current for the pass transistor is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). This results in a "quiescent" current that is proportional to load current—wasting more power at high loads. Another disadvantage associated with a PNP pass transistor is its tendency to saturate when the device goes into dropout. The resulting drop in current gain (β) forces an increase in base current (I_B) as the device attempts to maintain the output voltage. This translates into large start-up currents, and systems with limited supply current may even fail to start up. In battery-powered systems, rapid battery discharge can result when the voltage decays below the minimum required for regulation.

TI's PMOS LDO products feature low-dropout voltage, low-power operation, a miniaturized package and low quiescent current when compared to conventional LDO regulators. A combination of new circuit design and process innovation enabled replacing the usual PNP pass transistor with a PMOS pass element. Because the PMOS pass element behaves as a low value resistor near dropout, the dropout voltage is very low—typically 300 mV at 150 mA of load current (for the TI TPS76433). Since the PMOS pass element is a voltage-driven device as opposed to a current-driven device (like a PNP transistor), the quiescent current is very low (140 µA maximum) and remains constant and independent of output loading over the entire range of output load current (0 mA to 150 mA). The low-dropout voltage feature and low-power operation result in a significant increase in system battery operating life.

The increased performance of PMOS LDOs comes with stability concerns with respect to load current and external capacitance. This application note addresses the reasons behind the possibility for an unstable LDO linear regulator. An analysis of the control loop and a discussion of parameters affecting loop stability is presented.

LDO circuit model

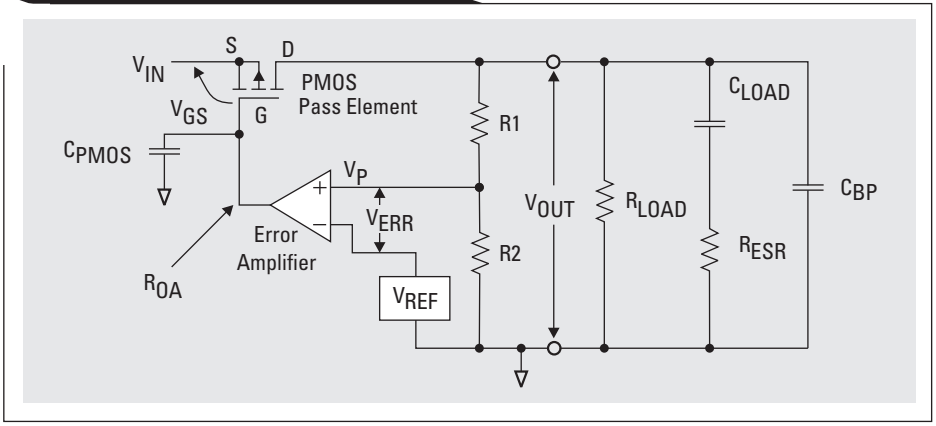
To begin the stability analysis of an LDO linear regulator employing a PMOS pass transistor requires a model that contains all the necessary components to provide sufficient accuracy for the analysis. The circuit shown in Figure 1 contains these components.

The important components for a stability analysis are defined in Table 1.

Stability analysis

Almost all voltage regulators use a feedback loop to maintain a constant output voltage. As with any feedback loop there is phase shift around the loop and the amount of phase shift determines loop stability. To have a stable loop the phase shift around the (open) loop must always be less than 180° (lagging) at the point where the loop has unity gain, or 0 dB. Low-dropout regulators require an output capacitor connected from V_{OUT} to GND to stabilize the internal control loop. Typically, a minimum value of output capacitance is specified. In addition, a range of ESR (equivalent series resistance) is specified. The following stability analysis reveals the reasons for such specific output capacitance requirements. An expression for the open-loop gain of a typical LDO linear regulator is derived that can be plotted using an analysis tool to determine the open-loop UGF (unity gain frequency) and phase margin (ϕ_m). In Figure 1, three poles and one zero can be identified. To simplify the expressions, it is assumed that $C_{BP} << C_{LOAD}$. The first pole ($p1$) is due to the PMOS pass transistor output resistance plus the output capacitance ESR ($R_{O\,PMOS} + R_{ESR}$) and the output capacitance (C_{LOAD}).

Figure 1. Basic PMOS LDO model



$$p1 = \frac{1}{2\pi\,(R_{O\,\mathrm{PMOS}} + R_{\mathrm{ESR}}) \times C_{\mathrm{LOAD}}}$$

The second pole ($p2$) is due to the output capacitance ESR (R_{ESR}) and the estimated bypass capacitance, C_{BP}.

$$p2 = \frac{1}{2\pi \times R_{\mathrm{ESR}} \times C_{BP}}$$

The third pole ($p3$) is due to the error amplifier output resistance (R_{OA}) and the equivalent PMOS capacitance (C_{PMOS}).

$$p3 = \frac{1}{2\pi \times R_{OA} \times C_{\mathrm{PMOS}}}$$

The single zero ($z1$) is derived from the output capacitance ESR (R_{ESR}) and the output capacitance (C_{LOAD}).

$$z1 = \frac{1}{2\pi \times R_{\mathrm{ESR}} \times C_{\mathrm{LOAD}}}$$

The remaining information required is the error amplifier gain, feedback network gain and PMOS pass transistor gain. Values given for the following gains are for illustrative purposes and are reasonable values for 100-mA output LDO linear regulators.

The error amplifier gain (G_{EA}) is assumed to be 35 dB.

$$G_{EA} = 35\ \mathrm{dB} = 56.2$$

The feedback network gain (G_{FB}) is simply the gain of the resistive divider, R1 and R2. For an output voltage of 3.3 V (for example) and a reference voltage of 1.192 V, the feedback network gain is

$$G_{FB} = \frac{V_{\mathrm{REF}}}{V_{\mathrm{OUT}}} = \frac{1.192}{3.3} = 0.36 = -8.8\ \mathrm{dB}.$$

The PMOS pass transistor gain (G_{PMOS}) is assumed to be 8 V/V.

$$G_{\mathrm{PMOS}} = 8 = 18.1\ \mathrm{dB}$$

The resulting expression for open-loop gain is

$$G_{OL}(s) = G_{EA} \times G_{FB} \times G_{\mathrm{PMOS}} \times \frac{1 + \frac{s}{2\pi fz1}}{\left(1 + \frac{s}{2\pi fp1}\right) \times \left(1 + \frac{s}{2\pi fp2}\right) \times \left(1 + \frac{s}{2\pi fp3}\right)}.$$

The following component values are used (for illustrative purposes):

$R_{O\,\mathrm{PMOS}}$ = 65 Ω
R_{ESR} = 2 Ω
C_{LOAD} = 10 µF
C_{BP} = 0.5 µF
R_{OA} = 300 kΩ
C_{PMOS} = 200 pF

For the given component values, the pole and zero locations are:

$fp1$ = 238 Hz
$fp2$ = 159 kHz
$fp3$ = 2.65 kHz
$fz1$ = 7.96 kHz

The DC gain is G_{OL}(DC) = 162 ⇒ 44.2 dB.

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Table 1. Definition of stability analysis components

Reference voltage	This voltage is the basis for the output voltage. The output voltage cannot be more accurate or stable over temperature than the reference voltage. For many of TI's LDOs, this voltage is 1.192 V.
Error amplifier	The function of the error amplifier is to compare a scaled representation of V_{OUT} to the reference voltage and amplify the difference. The error amplifier output then drives the PMOS pass transistor to adjust V_{OUT}. A typical error amplifier DC gain is 25 dB to 45 dB, depending on the particular LDO.
Feedback network	The feedback network is a resistive voltage divider. This network scales V_{OUT} such that the scaled V_{OUT} is equal to the reference voltage when V_{OUT} is at its nominal value. For fixed output LDOs these resistors are internal to the LDO and have a relatively high value in order to minimize current drain.
R_{LOAD}	Load resistance. $R_{\mathrm{LOAD}} = V_{\mathrm{OUT}}/I_{\mathrm{OUT}}$.
C_{LOAD}	The capacitance placed on the output of the LDO for loop stability that is typically specified to be a minimum of 4.7 µF to 10 µF. Depending on the type of capacitor, it may have an internal ESR ranging from 10 Ω to 10 mΩ.
R_{ESR}	The equivalent series resistance of the output capacitor. Depending on the particular output capacitor, this resistance may include an external resistance placed in series with the output capacitor. This resistance is sometimes called the *compensation series resistance*.
C_{BP}	An estimate of the bypass capacitors placed across the power supply leads of the ICs powered by the LDO. These capacitors are usually 0.1-µF ceramics and have very low ESR.
C_{PMOS}	The capacitance connected to the output of the error amplifier. This capacitance is due mainly to the capacitance of the PMOS pass element and is usually in the range of 100 pF to 300 pF.
R_{OA}	The equivalent output resistance of the error amplifier. This parameter is one of the few parameters the LDO designer can choose to insure stability. A typical design value is approximately 300 kΩ.
PMOS pass	The series pass element in the LDO. This transistor operates as a variable resistance connected between the input and the output. The resistance is controlled by the gate-to-source voltage. The output resistance, $R_{O\,\mathrm{PMOS}}$ (different from R_{OA}), is used in the stability analysis.

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Figure 2 shows a gain-phase plot of the above equation using the values given. Also shown in the plot are the pole and zero frequencies. Figure 2 shows a stable system. The UGF is approximately 14 kHz with a phase margin of 66°. Notice that the single zero occurs at a lower frequency than the UGF. This configuration of two poles and one zero below the UGF produces a stable system.

To illustrate the need for a minimum value of R_{ESR}, the gain-phase plot is recalculated with R_{ESR} set to 10 mΩ. Figure 3 is a gain-phase plot of the same system, except with R_{ESR} = 10 mΩ. The UGF is now 10 kHz with an unacceptable phase margin of 16°. With a very low ESR value such as this, pole *p2* and zero *z1* are both at frequencies much higher than the UGF. This leaves two poles below the UGF, producing an unstable system.

To illustrate the need for a minimum value of C_{LOAD}, the gain-phase plot is recalculated with C_{LOAD} set to 1.0 µF.

Figure 2. LDO open-loop response (stable)

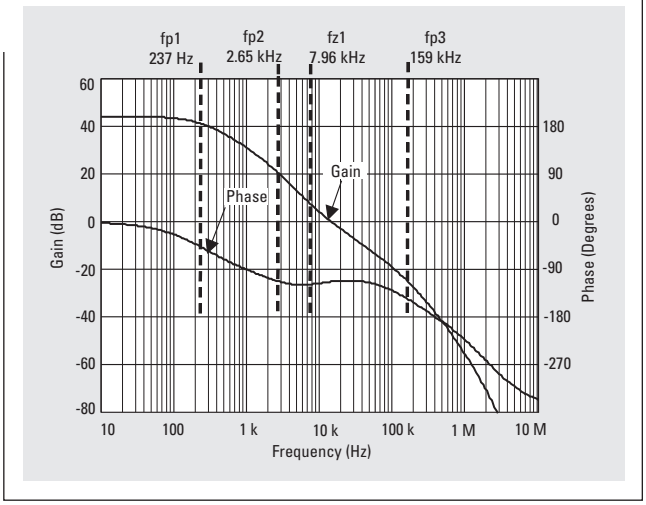

Figure 3. LDO open-loop response (unstable). R_{ESR} = 10 mΩ.

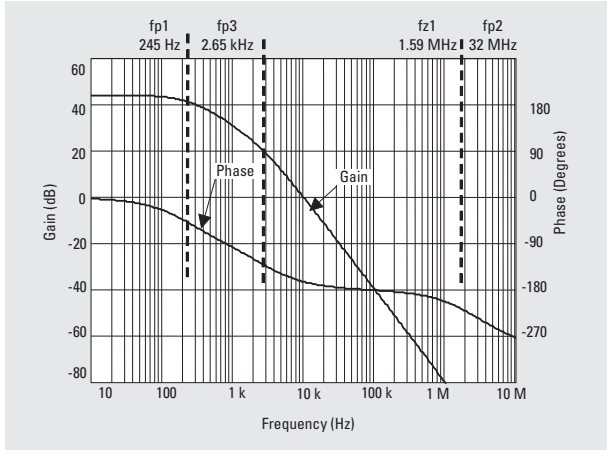

Figure 4. LDO open-loop response (unstable). C_{LOAD} = 1 µF.

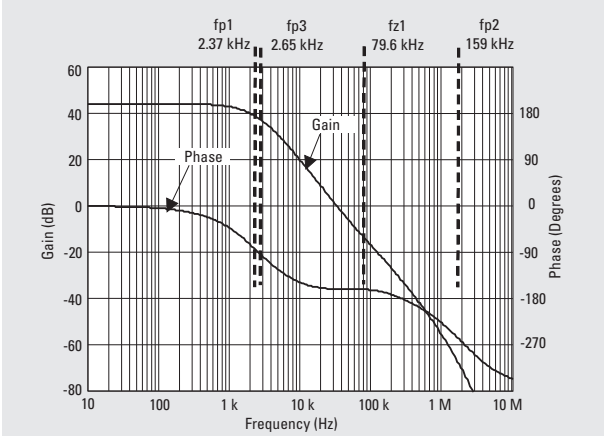

Figure 4 is a gain-phase plot of the same system, except with C_{LOAD} = 1.0 µF. The UGF is now 32.4 kHz with an unacceptable phase margin of 18°. With a low C_{LOAD} value such as this, pole *p2* and zero *z1* are both at frequencies higher than the UGF. This leaves two poles below the UGF, producing an unstable system.

Summary

Low-dropout linear regulators with a PMOS pass element give increased performance over linear regulators employing NPN or PNP pass elements. With this gain in performance comes a concern over control loop stability. This is common to all LDO designs, especially ones using PMOS or PNP pass elements. Selecting the appropriate output capacitor and resistor to place in series with the capacitor easily solves most stability issues. The expression for the (open) control loop gain and phase vs. frequency is derived and an illustrative example is given. The expression for the control loop shows what parameters and/or component values affect stability.

References

1. M. Kay, “Design and Analysis of an LDO Voltage Regulator with a PMOS Power Device,” preliminary paper pending publication, Texas Instruments Inc., Dallas.
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3. G. A. Rincon-Mora and P. E. Allen, “Optimized Frequency-Shaping Circuit Topologies for LDOs,” *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, Vol. 45 (June 1998), pp. 703-708.