A NEW LINEAR REGULATOR FEATURES SWITCH MODE OVERCURRENT PROTECTION

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ABSTRACT

This paper presents a new linear control circuit which, in addition to offering benefits such as low input-out-put differential and a precise reference voltage, features a unique and innovative approach to overload protection. By using duty-ratio, switch-mode protection, this circuit eliminates both the high internal dissipation of constant current limiting and the latch-up tendencies of limiting with current foldback.

THE CURRENT LIMIT PROBLEM

As an opening statement, let us offer as a "given" that all linear power supplies need some form of over-current protection. Traditionally, this protection consists of configuring supply to control current - rather than output voltage - once an established threshold of maximum current has been exceeded. The method of current control can usually be classified as either "constant-current" or "current-foldback" current limiting and, while simple to classify, choosing between these two methods is often less than satisfying.

The protective method most acceptable to the user is constant current limiting with a characteristic as shown in Figure 1. With the knowledge that a power supply will only deliver a maximum current regardless of what he might do to it, the user's job of scaling his cables, switches, connectors, and other components associated with the power inputs to his system is greatly eased. He knows that no matter how non-linear his load may be, he can count on a regulated voltage whenever his current drain is within the supply's rating. Further, he knows that the maximum rated current is always available to meet any demand asked of the supply.

The "benefits" of constant current limiting are another matter to the power supply designer, however. For example, a regulator designed to deliver 12 Volts at a maximum load current of 5 Amps, would probably start with a bulk input voltage of approximately 15 Volts and a constant current limit of 5.5 Amps. Under maximum rated load, the internal dissipation of the regulator is 3V x 5A or 15 watts but with a short to ground, this dissipation jumps to 15V x 5.5A or more than 80 Watts! This means that the thermal management and heat sinking must be sized for the short circuit condition resulting in a massive overkill in terms of volume, complexity, and cost with respect to normal operating conditions.

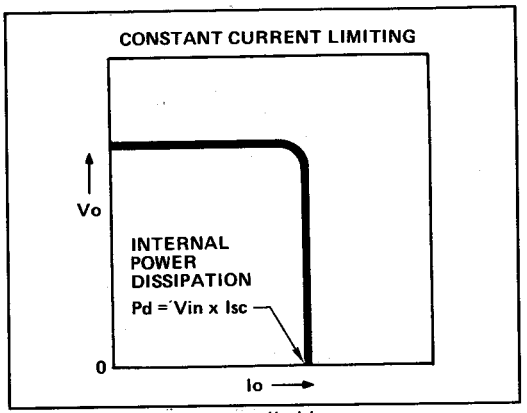

Figure 1: Constant current limiting.

A common solution to this problem is to design a current limiting scheme as illustrated in Figure 2. Here the protection is actuated at 5.5 Amps when the output voltage is at 12 Volts but the allowable current then "folds back" as the output voltage falls due to increasing overload, until it reaches some much lower value - say one Amp in this example - with a shortened output. Now the dissipation with a short circuit is close to the same as it was with rated current and our designer's thermal problems are solved.

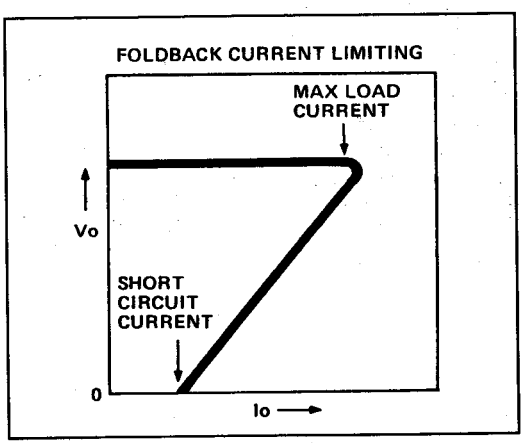

Figure 2: Foldback current limiiting

Minidip package allows the potential for meeting the cost objective (plus the benefit of less PC board area), but in several important ways, also restricts the device's versatility. Recognizing this fact led to the introduction of the same chip in a 14-pin package with a UC1832 designation. The block diagram of this device, in a uA723-type application, is shown in Figure 8.

The characteristics of the UC1832 include all the performance features of the UC1833 plus the following:

1. Separating the +Vin line from the CS+ terminal so that the controller could be supplied from a higher potential, low-current, auxiliary voltage while sensing current from the main supply.

2. Separating the Reference from the Error Amplifier (+) input and making both accessible to the user. Among other things, this allows phase reversal, an external or divided-down reference, and a convenient access point for soft-start.

3. Providing a separate input to the Driver's local current limiter allows considerable flexibility in setting that limit either higher or lower than the 300 mA (typical) defined by the internal 2.4 ohm resistor.

4. A separate logic-level digital shutdown function has been added to give more programming options such as accepting a shutdown command from an over-voltage sensor or implementing a turn-on delay. This input is fail-safe as it must be pulled low to allow the regulator to turn on.

5. Allowing the input offset of the current sense amplifier to be programed with an external voltage on the V_{ADJ} terminal, normally provided by a voltage divider form V_{REF}. With V_{ADJ} high or open, the offset is 130 ON V, equivalent to the UC1833. When V_{ADJ} = 0, the offset is increased to 300mV, allowing a much higher current limit level. A capacitor on this pin can be used to provide higher peak currents at turn on but lower levels for faults which occur later.

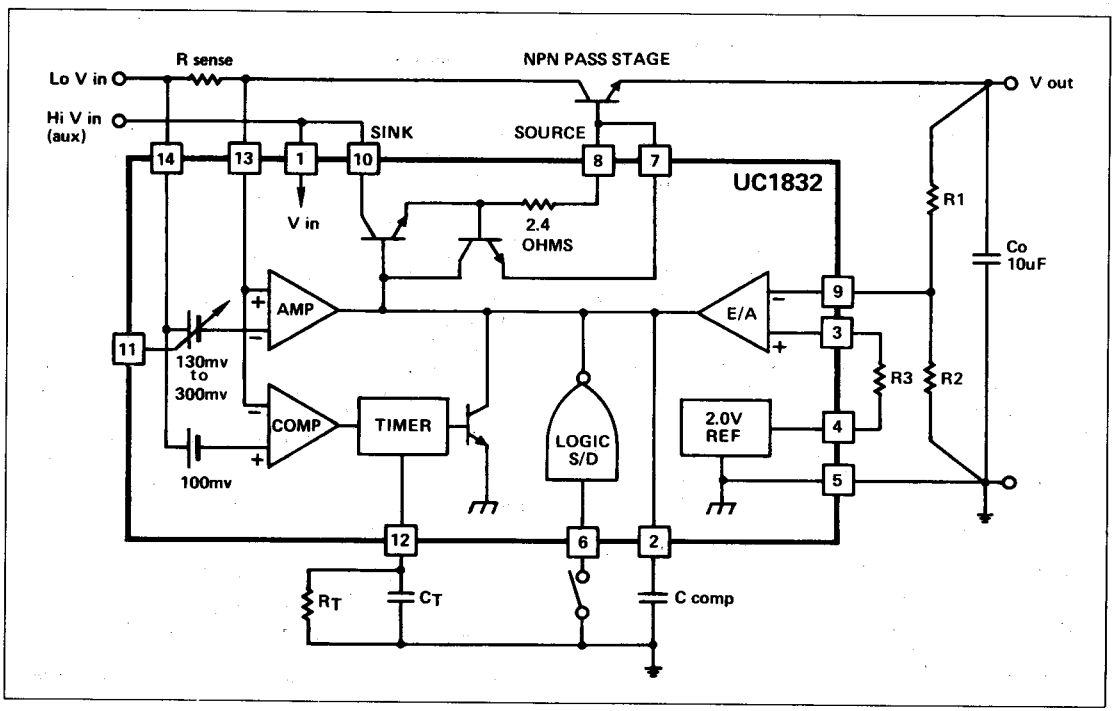

Figure 8: A 14-pin version, designated UC1832 / UC3832, offers enhanced versatility.

Timing waveforms during an overload cycle are shown in Figure 7 where the upper graph shows the output current from the regulator, the center one plots the voltage on the timing components, and the regulator's output voltage is shown in the lower graph. Following the sequence of events as drawn in the figure, when the load current ramps up and crosses the 100 mV Comparator threshold, the initial ON time begins. This initial period is about twice the duration of successive ON-times as the timing capacitor starts its charge from zero initially, while subsequent ramps begin from the lower Comparator threshold. While the timing capacitor is charging, the regulator current is limited by the action of the Current-sense Amplifier to maintain a level of 130 mV across the sense resistor. While in current limiting, the regulator's output voltage falls to whatever value that current will allow across the faulted load impedance.

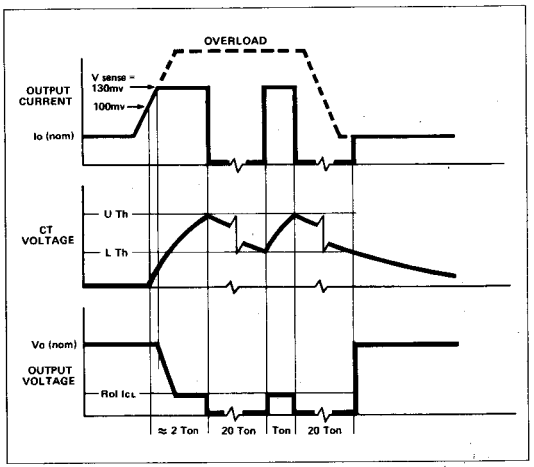

Figure 7: Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.

The ON-time continues until the internal 10k resistor charges the timing capacitor to the upper Timer threshold. At this point, both the ON-time of the regulator and the charging of the timing capacitor are terminated, and the capacitor now discharges through RT, while the regulator is held OFF until the voltage on CT reaches the lower threshold, at which point the cycle repeats. If the load fault is removed during an ON-time, the Timer is immeadiatly disabled allowing the regulator to recover and the timing capacitor to discharge back to zero. If the fault is removed during an OFF-time, the Timer must complete that cycle of capacitor discharge before allowing the regulator to turn back on. In special applications requiring an extended ON-time, the correspondingly long recovery may be accelerated by interrupting the input voltage, as the falling internal 5 V source will discharge CT through D1 and an equivalent 1k impedance.

Duty-ratio protection has greatly eased the problem of heat sinking created with a constant-current solution since the area of the heat sink, or its thermal resistance, need only remove the average power as reduced by the duty ratio. Heat sinks for the internal power devices must now only have adequate thermal mass to absorb the high peak power of the initial ON period.

REMAINING CONTROL CIRCUITRY

Other blocks within the UC1833 include a 2.0 Volt band-gap reference internally trimmed to 1% and a low input-offset Operational Transconductance Amplifier (OTA) to serve as the error sensing and amplifying circuitry. The OTA Error Amplifier has a gm of about 4 millimho and an output current capability of +/- 300 uA. This form of amplifier can usually be compensated with a simple network - often a single capacitor - from its output to ground; but more commonly, an R-C pole-zero pair is also added to compensate for an external PNP pass transistor's gain characteristics.

The Error Amplifier is followed by a unity-gain Buffer Amplifier which controls the Driver Stage consisting of a Darlington transistor pair with local current limiting. This Driver can either source or sink current, allowing its use as a driver for either NPN or PNP pass transistors. The Pullup and Pulldown current-sources shown at the Sink and Source terminals of Figure 6 are to provide turn-off bias to the pass transistor during duty-ratio switching so that it is not turned off into a BV_{CEO} condition.

Not shown on the schematic are two additional forms of protection built into the UC1833: Thermal Shutdown (TSD), and Under Voltage Lockout (UVLO). While it could be argued that thermal protection on the control chip does nothing to protect the pass transistor, the fact that the Driver can conduct up to at least 100 mA with a large portion of the input supply voltage across it, can result in more than acceptable internal heating of the UC1833. A good practice, when voltage levels permit, is the addition of an external resistor in series with either the Source or Sink outputs of the Driver to remove some of the voltage - and therefore some of the dissipation - from the controller.

Under Voltage Lockout keeps the Error Amplifier output low until the supply voltage reaches approximately 4 Volts insuring that all internal circuits - particularly current limiting functions - are intelligent before allowing the pass transistor to turn on. The UVLO function also disables the Pullup current feeding into the Sink terminal, for low input voltages, so that the pass transistor cannot be driven in the reverse direction should the input supply fall with a charged capacitor or other energy source on the output. The Source Pulldown current source is also disabled with UVLO but this terminal also has a two-diode path from the Source to the Compensation terminals. This is to allow any shutdown function which pulls the Comp pin low to discharge capacitance at the regulator's output without reverse-biasing the Driver's emitter-base junction.

THE UC1832 14-PIN CONTROLLER

An important objective in the design of the UC1833 was that in addition to providing significant operating benefits over the omnipresent uA723, the resulting product should be cost-competitive with that device. Committing the UC1833 to an 8-pin

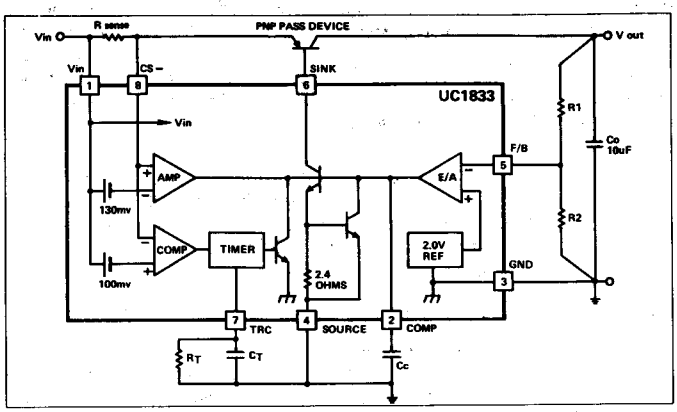

Figure 5: The new UC1833 / UC3833 linear regulator.

The current sensing portion of this circuit is to the left of this figure where the current-sense Comparator and Amplifier are shown sharing the same input sense pins. Note that their offset voltages are derived by a constant current through R1 and R2 in series rather than independently as shown in the more simplified earlier block diagram. By adding 30 mV to the 100 mV offset of the Comparator, the Amplifier's offset will more accurately track that of the Comparator should any variations occur, and the criteria to have the Comparator always activate first is assured.

A characteristic important to current protection is the accuracy of its threshold as any tolerance represents a window of undefined operation which works to the disadvantage of both designer and user of the power supply. Recognizing this, the UC1833's thresholds are derived from its precision reference resulting in a Timer activation threshold guaranteed to 5 percent over all operating conditions.

The Amplifier part of the current sense circuitry has an input threshold of 130 mV and overrides the output of the Error Amplifier to control the driver - when enabled by the ON-time of the timer - to regulate the supply's output current to a maximum amount determined by 130 mV divided by the value of the sense resistor. The 30 mV differential between the thresholds of the Amplifier and Comparator insures that current limiting can never occur without prior initiation of the timer.

OVERLOAD PROTECTION CIRCUITRY

The operation of the overload protection circuitry can be better understood by referring to the simplified schematic of Figure 6.

The output of the Current Amplifier connects into the output stage of the Error Amplifier where it can easily take command when activated. The compensation capacitor must compensate both the voltage and current feedback loops, and since the current loop must override the voltage control, its gain will be higher making the current loop the more difficult to stabilize. To evaluate the current loop, grounding the Timing pin will disable the Timer and allow continuous constant current operation. This can be useful either as a temporary measure while designing the current compensation network, or permanently to implement a constant-current limited power supply.

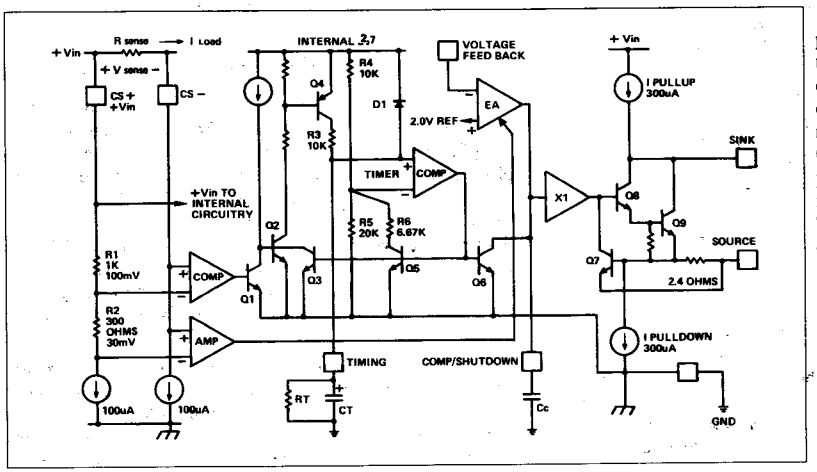

Figure 6: A simplified schematic of the UC1833 control circuitry.

The Current Sense Comparator is phased such that its activation turns off Q1 which turns on Q2 and Q4 to start the timing cycle. The timer is a gated astable relaxation oscillator with ON and OFF times independently programmed using an external resistor and capacitor, RT and CT. The external components work in conjunction with an internally switched 10k timing resistor shown in the schematic as R3. With RT much greater than 10k, the ON time is defined by R3 and CT, while RT and CT determine the OFF time. The thresholds for the Timing Comparator are set at 1/3 and 2/3 of the internally regulated 2.7V source by the values of R4, R5, and R6.

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But what about his customer? His load may be complex, nonlinear, and often not even well understood. Figure 3 shows typical load characteristics for digital and analog circuitry but an actual system may include all of these plus motors which need to be started and capacitors which need to be charged. Any protection scheme which allows the static load line to intersect the foldback current curve as shown in Figure 4 is potentially subject to latch up because the load draws more current than the regulator can supply at the voltage where the curves cross.

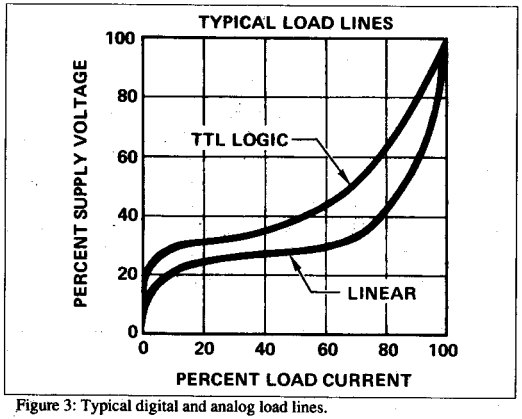


Figure 3: Typical digital and analog load lines.

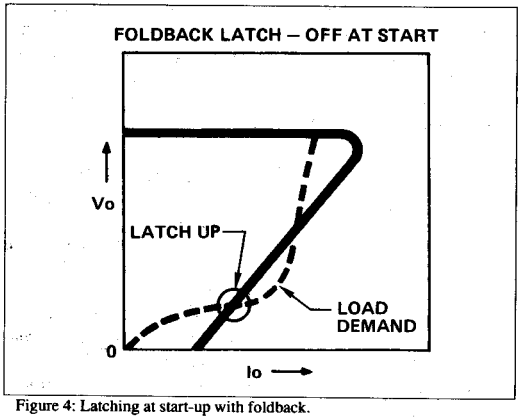


Figure 4: Latching at start-up with foldback.

An application particularly susceptible to latch up due to foldback current limiting occurs when two supplies are used to provide positive and negative voltages to a load where there is a path for "rail-to-rail" loading. As the regulators turn on, their output capacitors are charged at rates determined by the values of the capacitors and the amount of current each regulator can provide as its output rises up the foldback curve. Since these curves are unlikely to be perfectly matched, one output will dominate the other. As the faster one's output voltage increases, it provides more current through the common load. This forces the slower one back down the foldback curve where it provides less current, compounding the problem and ultimately latching when its output is driven past zero to a reversed polarity. Thus a foldback-limited regulator, which might be stable when used by itself, may latch when used as one-half of a dual-polarity system due to this "turn-on slew rate" phenomenon.

So what we have concluded is that while the power supply designer needs to incorporate foldback current limiting to reduce power dissipation, his customer needs constant-current limiting to insure reliable starting. It is the contention of this paper that what they both really need is duty-ratio protection.

DUTY-RATIO OVERCURRENT PROTECTION

Duty-ratio protection can be simply described as a constant current limiting regulator with a timer. The timer's function is to turn the regulator's power stage OFF and ON with an established duty cycle ratio such that the high internal power dissipation of constant current limiting is reduced by the duty ratio to a much more manageable average value.

Referring back to our earlier example of a 12V, 5A regulator, consider setting the constant current limit at 5.5 amps but additionally establish a duty ratio for the timer at 1 to 20 for "ON" to "OFF". If we set the "ON" time sufficiently long to charge whatever capacitance might be on the output, the regulator will power up with the constant current characteristic, insuring start-up regardless of the loading. In the event of an overload or short circuit (defined in this device as remaining in current limiting for a period of approximately 2 x Ton), the regulator will periodically shut down for a time equal to 20 x Ton and then continue to cycle in a 1 to 20 duty cycle until the fault is removed. Although the peak power during Ton might be 80 Watts, the average fault dissipation at this duty ratio is only 4 Watts - less than the normal 15 watt operating power loss, and we have thereby satisfied both the designer and his customer.

INTRODUCING THE UC1833 / UC3833

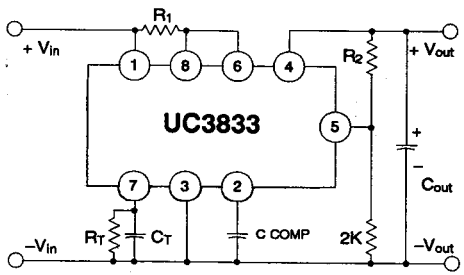
The block diagram of this new linear regulator control IC is shown in Figure 5. This circuit can be used in many different ways but its primary intent is as a high-efficiency regulator implemented with an external PNP pass transistor as shown in the figure. The circuitry in the right half of the UC1833 block generates the voltage error signal used to activate an NPN Darlington driver which, in turn, drives the base of the PNP pass device. This common-emitter pass transistor configuration allows this type of regulator to operate with a minimum input-output differential of well less than one Volt, even at high loads.

Duty-cycle current limiting is accomplished with the circuitry on the left half of the block diagram, where an Amplifier and a Comparator are seen, both monitoring the voltage drop across a single current sense resistor. The Comparator has an input threshold of 100 mV and, when activated, initiates a timer to alternately clamp and release the base of the driver to ground thereby switching the output of the regulator from Vout to Zero with a low duty ratio.

UC3833 Typical Applications

See appendix for component selection

LOW CURRENT APPLICATION
using the UC3833 internal drive transistor

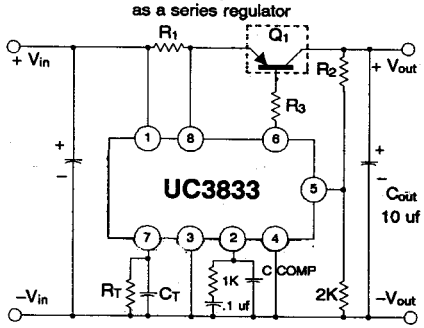


TYPICAL OUTPUT CURRENT vs. V_{in} and V_{out}
of the UC3833 internal drive transistor
for P_{diss} = 0.5 W (approx.)

		V_{in}					
	Volts	5	9	12	15	18	24
V_{out}	2	150	60	40	30	20	12
	5		105	55	35	25	15
	9			130	60	35	20
	12				120	55	25
	15	Current in mA				110	30

Fig. 3

LINEAR REGULATOR
using an external power transistor
as a series regulator



P CHANNEL POWER MOSFETs
can also be used as the series pass transistor Q_1

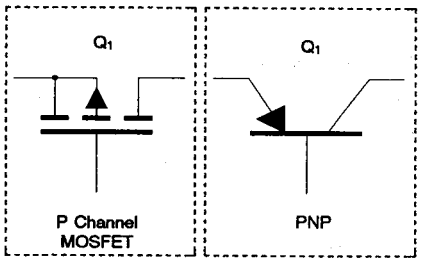
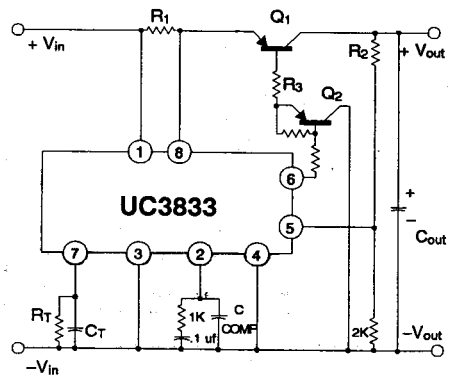


Fig. 4

HIGH CURRENT REGULATOR
using drive transistor Q_2 to increase Q_1 base drive
and reduce UC3833 power dissipation



PARALLEL PASS TRANSISTORS
can be added for high current
or high power dissipation applications

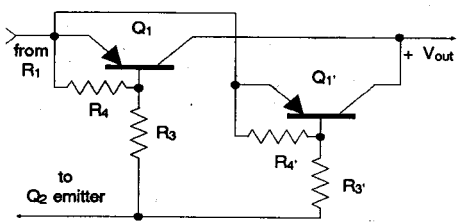


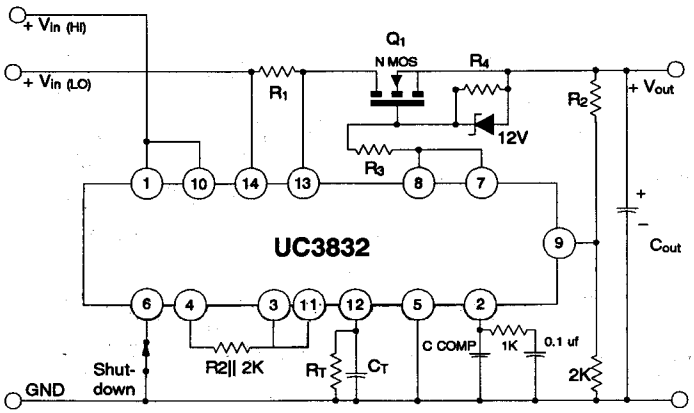
Fig.5

UC3832 Applications

See appendix for component selection

LOW DROPOUT REGULATOR

The UC3832 features a seperate supply input for operation from an auxiliary power source. Useful in low dropout applications.

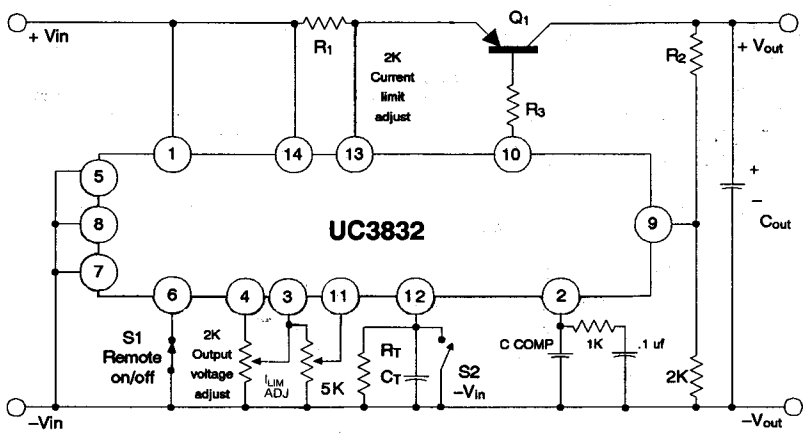


S1 - Closed: Normal operation
Open: Output disable

Fig. 6

PRECISION LABORATORY POWER SUPPLY

featuring adjustable voltage and current limiting



S1 - Closed: Normal operation
Open: Output disable

S2 - Open: Duty ratio current limit
Closed: Constant current output or I_{MAX} adjust.

Fig. 7

APPENDIX

Design Equations and Component Selection

R_1 - Current Sense Resistor

R1 = 0.135 V/I_{OUT} (max) UC1833 AND 1832 WITH V_{ADJ} = 2.5V

LOW CURRENT	
I_{OUT} mA	R_1 ohms
10	13
20	6.5
30	4.3
40	3.3
50	2.7
60	2.2
70	1.8
80	1.6
90	1.5

GENERAL USE	
I_{OUT} A	R_1 ohms
0.10	1.30
0.25	0.52
0.50	0.27
0.75	0.17
1.0	0.13
2.0	0.065
3.0	0.043
4.0	0.032
5.0	0.026

HIGH CURRENT	
I_{OUT} A	R_1 mohm
5	26
6	21
7	18
8	16
9	14
10	13
15	8.6
20	6.5
25	5.2

R_2 - Output Voltage Divider Resistor

$R_2 = (V_{OUT} - 2.0V)/1mA$

FIXED	
V_{OUT}	R_2
5.0	3.0K
9.0	7.0K
12.0	10K
15.0	13K
18.0	16K
24.0	22K

ADJUSTABLE	
$V_{OUT(MAX)}$	R_2
7.0	5K POT
12	10K POT
22	20K POT

R_3 - Drive Current Limit Resistor

$R_3 = ((V_{in} - V_{BE} - V_{sat}) * \text{Beta (min)})/I_{OUT}$ (max)

I_{OUT}	V_{in}		
A	9V	15V	24V
0.10	1.8K	3.2K	5.6K
0.25	680	1.2K	2.2K
0.50	330	650	1.1K
0.75	220	430	750
1.0	180	330	560
2.0	82	160	270
3.0	57	100	180
4.0	43	82	120

For circuit diagram of Fig. 4,
Beta (min) = 25, V_{BE} = 0.7V, V_{SAT} = 1.5V

I_{OUT}	V_{in}		
A	9V	15V	24V
1.0	200	350	560
2.0	100	175	270
4.0	50	87	140
5.0	40	70	110
7.5	27	47	75
10.0	20	35	57
15.0	13	24	38
20.0	10	17	27

For circuit diagram of Fig. 5,
Beta (min) = 25, V_{BE} = 0.7V,
$V_{SAT} \approx V_{BE}(Q_2) + V_{SAT}$ (UC3833)$\approx$ 1.5V

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R_T and C_T - Timer Duty Duration and Ratio Resistor and Capacitor

$T_{on} = 0.693 * 10K * C_T$

$T_{off} = 0.693 * R_T * C_T$

Duty Ratio = $T_{on}/(T_{on}+ T_{off}) = 10K/(10K+ R_T)$

NOTE: Typical duty ratios are between 0.5% and 5%

Duty Ratio	R_T ohms
5%	180K
4%	240K
3%	330K
2%	470K
1%	1 MEG
0.5%	2 MEG

T_{on} msec	C_T* uf
1	0.15
2	0.30
5	0.68
10	0.15
20	3.0
50	6.8
75	10
100	15

T_{on} sec	C_T* uf
0.1	15
0.2	30
0.5	68
1.0	150
2.0	300
5.0	680
7.5	1000
10.0	1500

* Timing capacitor C_T should have extremely low leakage current.

Q1 - Pass Transistor

I_{OUT} A	PNP Transistor	P Channel MOSFET	N Channel MOSFET
< 1.0	TIP30 D41D4	IRF9511 RFP5P12	IRF511
2.5	TIP32,34 D45C2	IRF9521 RFP6P08	IRF521
5.0	D45H5,8 MJE6040	IRF9531 RFP12P08	IRF531 IRFZ10
7.5	TIP36 2N6666*	IRF9541	IRF541 IRFZ20
10.0	TIP36,145* 2N6648*	IRF9541 RFK25P08	IRF540 IRFZ20
15.0		IRF9Z30 RFK25P08	IRFZ30
20.0	2N6285*	RFK25P08	IRFZ40

* Darlington transistor

A higher power application is shown in the schematic of Figure 10 which was designed to supply 5 Volts at 5 Amps. The UC3833, configured as shown, will meet this requirement with an input voltage as low as 6 Volts due to the low saturation voltage of the paralleled 2N6489 transistors and the fact that the maximum non-fault voltage on the sense resistor is less than 100 mV. Actually, a little more sense voltage was sacrificed in the interests of selecting a standard resistor value, with the excess divided down by the 56/100 ohm divider. The additional BD438 drive transistor was added to boost the UC3833 drive current and keep the internal power dissipation low.

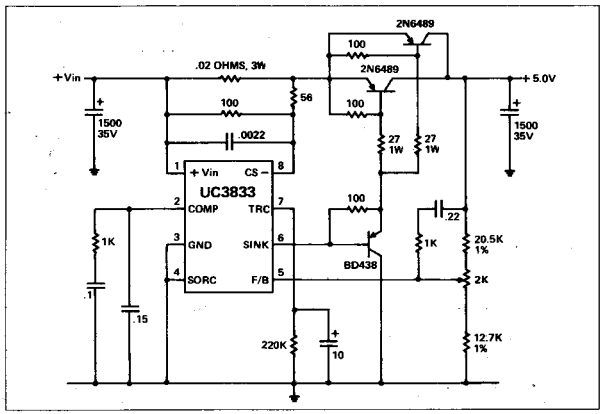

Figure 10: A high-efficiency configuration with added current boost will deliver 5V at 5A from a 6V source.

A third application of the UC3833 is one which took particular benefit from duty-cycle current limiting. This was for a disk drive power supply which required considerable current at turn-on to accelerate the disk. The circuit schematic is the same as that shown in Figure 10 with the voltage sense resistors selected for a 12 Volt output. The power requirements dictated a peak start current of 5 Amps decaying to 3 Amps in 30 seconds as the motor reached operating velocity. The current sense resistor was chosen to give a Timer initiation at 4.75 A and a constant current limit of 6.1 Amps. The timing capacitor value was set at 3300 uF yielding an ON-time of approximately 20 seconds, with 40 seconds for the initial turn on period - during which time the motor current will decrease to less than the lower threshold. With a duty-ratio of 20:1, when a fault does occur, the OFF-time will now be greater than 6 minutes, but, if this is excessive, recycling the input voltage to the regulator will reset the timing capacitor.

CONCLUSION

While no one can deny the long-term success of the uA723 as a general-purpose linear regulator controller, there has also long been a call for a device to improve its many limitations. While other products have been marketed offering some parametric improvements, the UC1833 - and its companion UC1832 - are the first to offer an innovative solution to a very basic problem. By combining switch-mode protection with linear regulation, these devices answer the question of which form of protection is best for whom, with a solution that is best for everyone.

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