VERSATILE UC1834 OPTIMIZES LINEAR REGULATOR EFFICIENCY

Linear voltage regulators have long been an important resource to power supply designers. Three terminal, fixed-voltage linear regulators find extensive use as "spot" regulators and as post-regulation stages fed by switched-mode supplies. However, while inexpensive and simple to use, these devices have several performance limitations.

First, three terminal regulators are inefficient power converters. Power dissipation in a linear regulator is given by the relation:

$$P = I_O \cdot (V_{IN} - V_{OUT}).$$

Most monolithic regulators now available require an input-to-output voltage differential of at least 2 to 3V. This requirement can result in substantial inefficiency, particularly in low voltage supplies. As switched-mode power technology matures, power losses incurred in linear post-regulation stages are becoming more significant in terms of overall system efficiency.

Second, fixed-voltage regulators, with fixed maximum output currents, lack versatility. The use of these devices requires that OEMs maintain large, diverse inventories in order to support a broad range of power supply requirements.

Third, fixed three-terminal devices lack the capability of remote voltage sensing, and therefore can exhibit poor load regulation.

Finally, the most common failure mechanism for linear regulators is a shorted pass transistor. All critical loads, therefore, require over-voltage protection not provided by three-terminal regulators.

IMPROVED PERFORMANCE WITH UC1834

The UC1834 is a programmable linear regulator control IC which, with an external pass transistor, forms a complete linear power supply. This IC provides solutions to all the above-mentioned drawbacks of three-terminal devices.

Figure 1 shows the basic elements of positive and negative regulators implemented with the UC1834. An error amplifier monitors the output voltage and provides appropriate bias to the pass transistor (Q1) through a driver stage. This high-gain error amplifier (E/A) allows good dynamic regulation while allowing Q1 to operate near saturation in the common-emitter mode. The circuits can achieve high efficiency by maintaining output regulation with an input-to-output voltage differential as low as 0.5V (at 5A).

The UC1834 has both positive and negative reference voltage outputs, as well as a sink-or-source driver stage, as shown in Figure 1. These features allow implementation of either positive or negative regulators with this single IC, as shown. Output voltages from 1.5V to nearly 40V can be programmed by appropriate choice of remote sensing divider elements. Remote sensing also allows improved DC and dynamic load regulation.

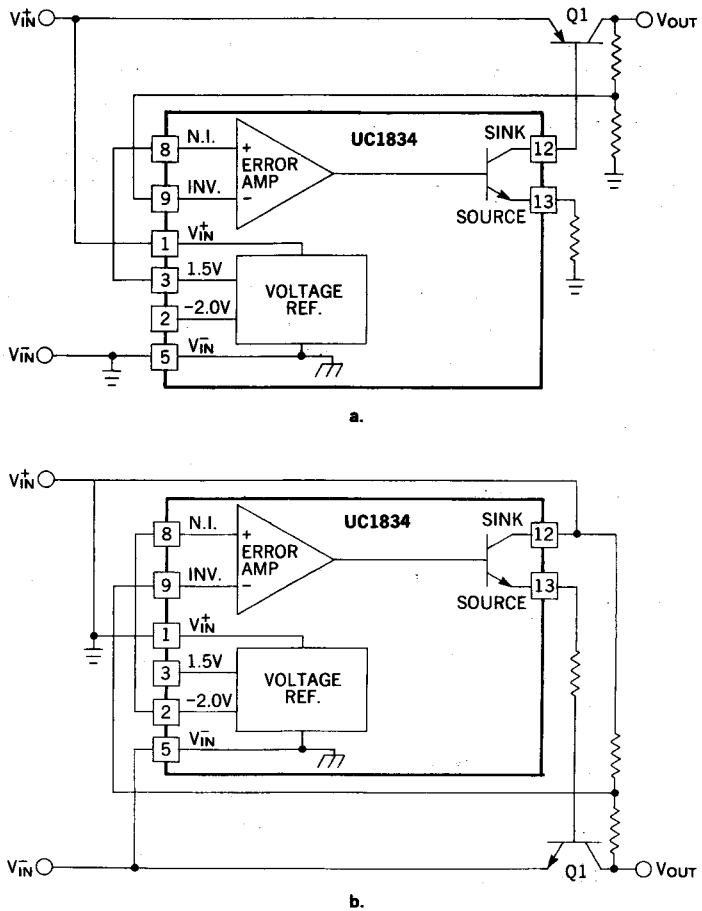

Figure 1. Basic Elements of (a.) Positive and (b.) Negative Regulators implemented with a UC1834

The UC1834 is intended to provide a complete linear regulation system. Therefore, many auxiliary features are included on this IC which eliminate the need for additional circuit elements. Figure 2 shows a more complete block diagram including on-chip provisions for current sensing, fault monitoring, remote voltage sensing, and thermal protection.

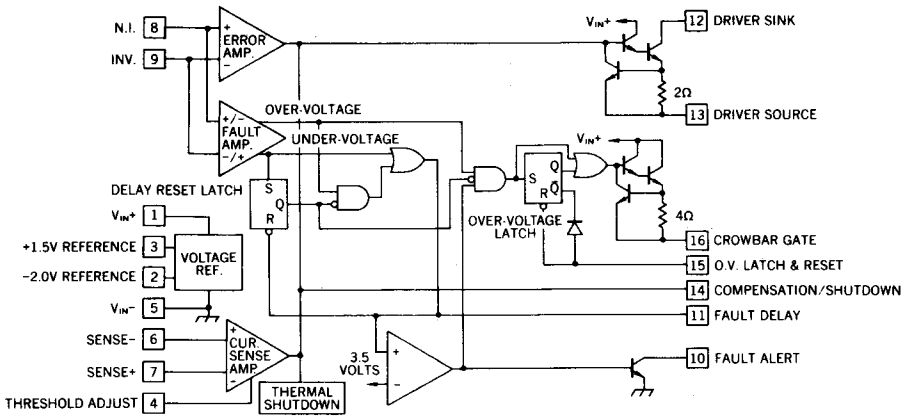

Figure 2. UC1834 Block Diagram

DRIVING THE PASS TRANSISTOR

Figure 3 shows suggested pass transistor configurations for implementing either positive or negative regulators with the UC1834. For those low current (≤200mA) applications in which efficiency is not extremely critical, the UC1834 output transistor can serve as the pass element, resulting in the simple configurations of Figure 3a. An external pass transistor is needed for output currents greater than 200mA. With the circuits of Figure 3c, the UC1834 can maintain regulation while operating the pass transistor near saturation. Operation at very high output currents (to ~30A) is possible with the Darlington pass elements of Figure 3d.

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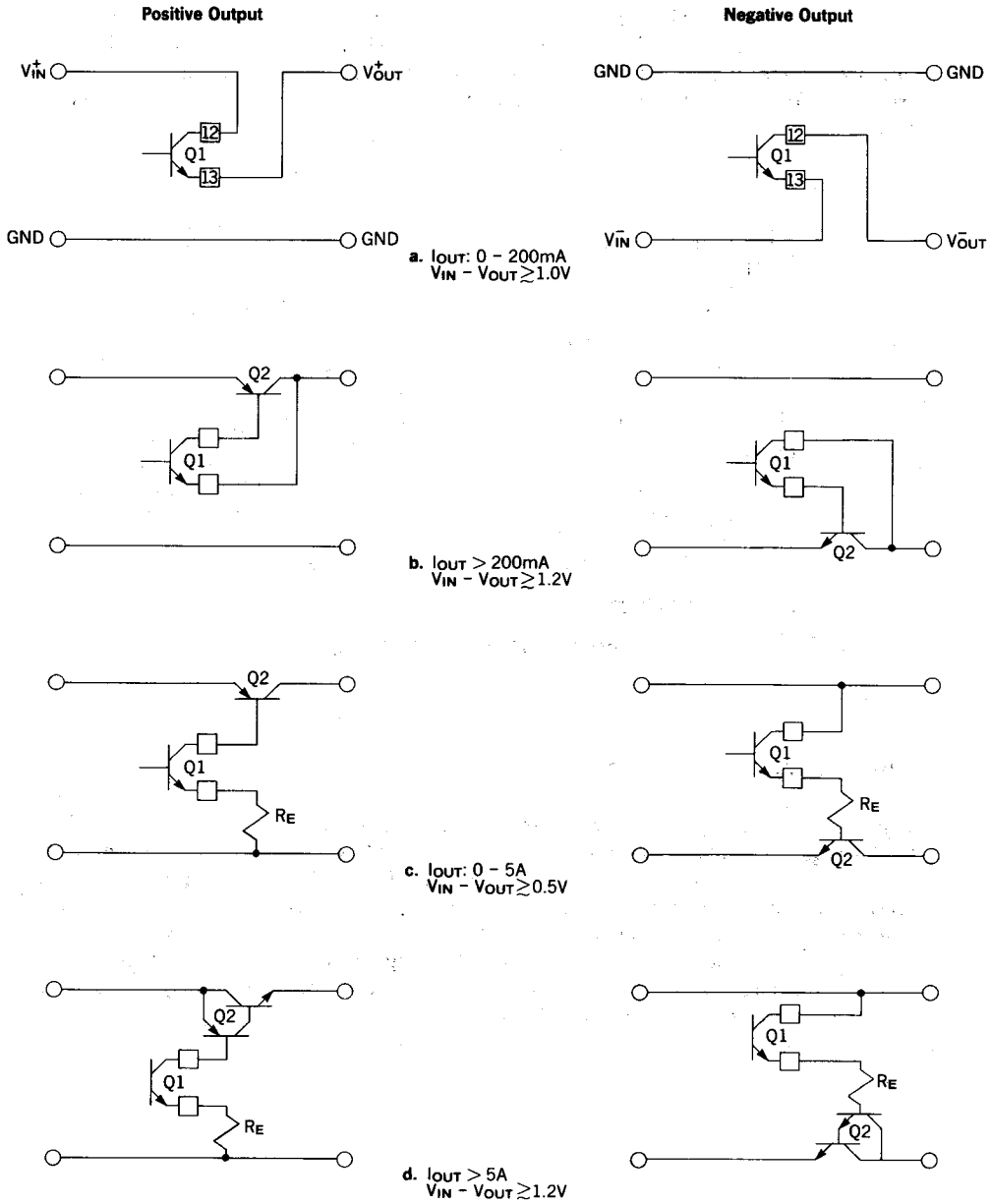


Figure 3. Pass Transistor Configurations

Current in the UC1834 output transistor is self-limiting, for improved reliability. This limiting is achieved by Q3 and R1 in Figure 4a. The resulting maximum output current is a function of temperature as shown in Figure 4b.

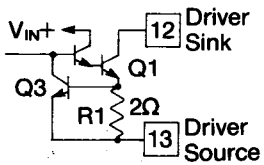
A resistor (R_E) is shown in series with the drive transistor in Figures 3c, d. This resistor shares base-drive power with the transistor, allowing cooler, more reliable operation of the IC. R_E should be as large as possible while still supporting adequate pass transistor base current under worst-case conditions of low input voltage and maximum output current:

$$V_{R_E(min)} = V_{IN(min)} - V_{BE(max)(Q2)} - V_{CE(sat)(max)(Q1)}$$
$$I_{B(max)(Q2)} = I_{O(max)} / \beta_{(min)(Q2)}$$
$$R_{E(opt)} = V_{R_E(min)} / I_{B(max)(Q2)}$$

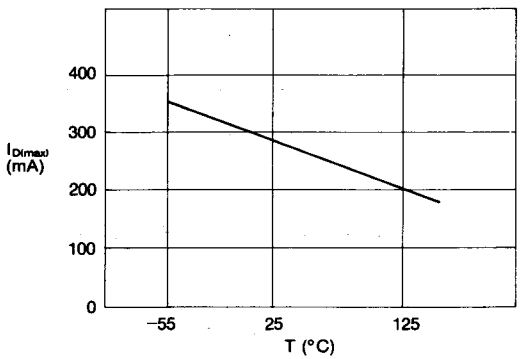
where: $V_{R_E(min)}$ is minimum voltage available to R_E
$I_{B(max)\ (Q2)}$ is maximum required base drive to Q2
$R_{E(opt)}$ is optimum value of R_E.

R_E also enhances stability by allowing operation of Q1 as an emitter-follower, thereby eliminating β_{Q1} from the loop transfer function:

$$I_{C(Q1)} \approx I_{E(Q1)} = (V_{E/A\,out} - V_{BE(Q1)} - V_{BE(Q2)}) / R_E \quad (\beta \text{ independent}).$$



a.



b.

Figure 4 a. Driver Current Limiting Circuit
b. Resulting Maximum Current vs Temperature

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CURRENT SENSING

In order to protect the pass transistor from damage due to overheating, one must sense its emitter current (I_E) and then decrease the base drive if I_E is excessive. The UC1834 current sense amplifier (CS/A) accomplishes these tasks.

The UC1834 CS/A has a common mode range which includes both input supply "rails". This extended range is made possible by introducing matched voltage offsets in the differential input paths, as shown in Figure 5. Internal current sources bias the offset diodes in their appropriate direction. Which bias source (+ or -) is active is determined by whether the CS/A positive (+) input is greater or less than $V_{IN}/2$. Therefore, it is advisable to configure the sensing circuit such that the voltage at CS/A(+) will not cross $V_{IN}/2$ during operation. This precludes sensing in series with the load for most applications.

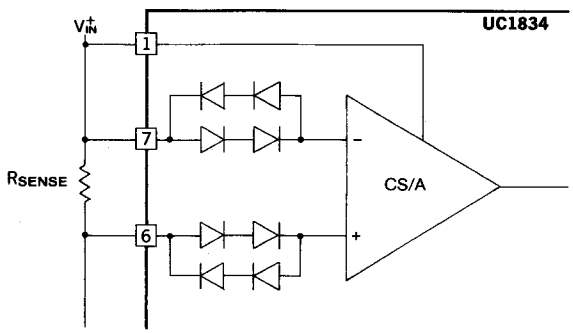

Figure 5. Two Diode-Drop Offset Allows Current Sensing at Supply Rail

The CS/A has a programmable current limit threshold which can be set between 0mV and 150mV. Programming is achieved by setting the voltage at the "Threshold Adjust" terminal (pin 4) to $10 \cdot V_{TH(desired)}$. The factor of 10 provides good noise immunity at pin 4 while allowing low power dissipation in the current sensing resistor. Figure 6 shows the guaranteed relationship between V_{PIN4} and the actual resulting threshold across the CS/A inputs. Note that the threshold is clamped at 150mV if pin 4 is open or if $V_{PIN4} > 1.5V$. The "Threshold Adjust" input is high impedance (bias current is less than $10\mu A$), allowing simple programming through a voltage divider from the 1.5V reference output. However, loading the 1.5V reference will affect the regulation of the -2.0V reference. Figure 7 shows how to compensate for this loading with a single resistor when the -2.0V reference is needed.

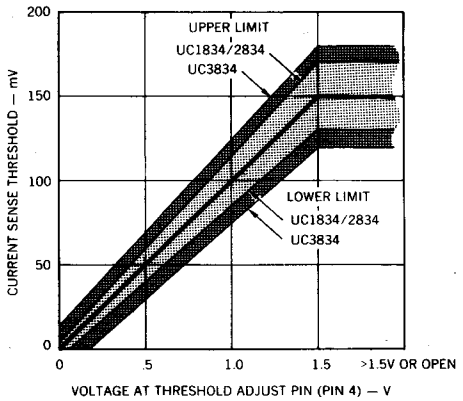

Figure 6. Guaranteed Tolerances on C/S Threshold Adjustment

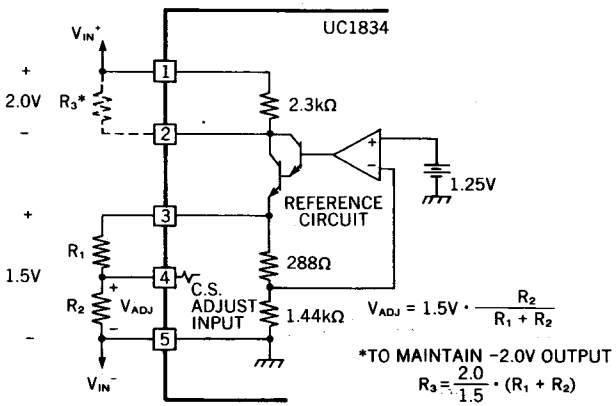

Figure 7. Setting the Current Threshold and Compensating the −2.0V Reference

The CS/A functions by pulling the E/A output low, turning off the output driver (Figure 8). As current approaches the threshold value, the E/A attempts to correct for the CS/A output, resulting in an E/A input offset voltage. The supply output voltage can decrease a proportional amount. When the CS/A input voltage differential reaches the current sense threshold, then the pass transistor is totally controlled by the CS/A. The combined CS/A and E/A gains and output configurations result in the current limit knee characteristic of Figure 9.

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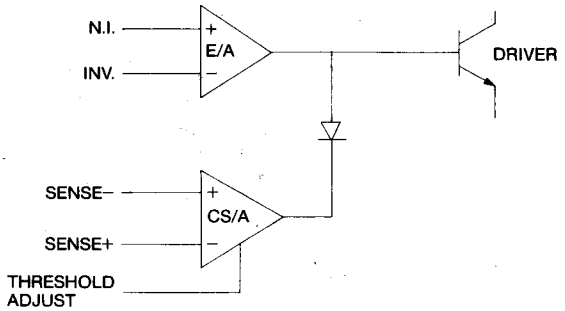

Figure 8. Current Sense Tied to E/A Output

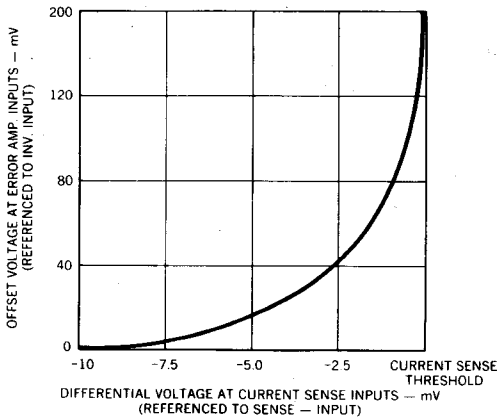

Figure 9. Current Limiting Knee Characteristic

FOLDBACK CURRENT LIMITING

It is desirable to put an upper limit on pass transistor power dissipation in order to protect that device. Ideally, for a constant power limit:

$$I_{E(max)} \cdot V_{CE} \simeq K \quad \text{where K is a constant}$$

or: $$I_{E(max)} \simeq K/(V_{IN} - V_{OUT}) \quad \text{(ignoring the sense resistor voltage drop).}$$

As the input-to-out voltage differential increases, it is necessary to "fold back" the maximum allowable current. This ideal foldback characteristic is shown in Figure 10, along with a practical characteristic achievable with the circuit of Figure 11.

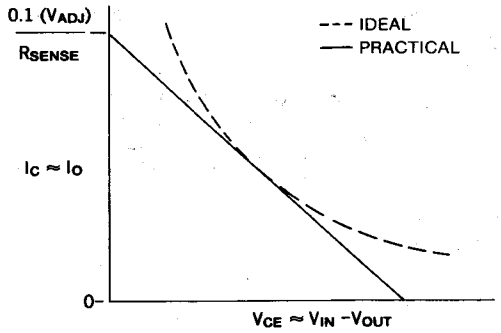

Figure 10. Ideal (Dashed Line) and Practical (Solid Line) Foldback Current Limiting Characteristics

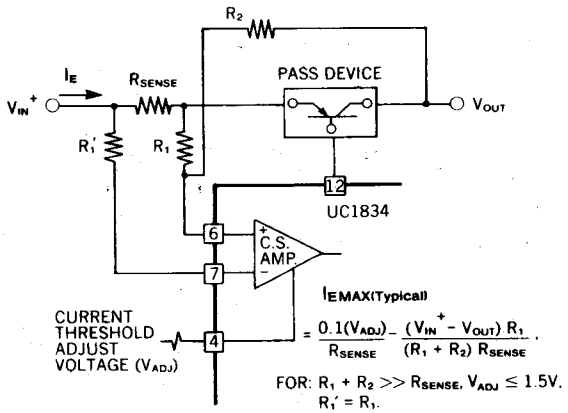

Figure 11. Foldback Current Limiting — Responds to Changes in V_{IN} or V_{OUT}

This circuit responds to changes in either V_{IN} or V_{OUT}. The voltage differential V_{IN} - V_{OUT} causes proportional current flow through R_1 and R_2. The additional drop across R_1 is interpreted by the CS/A as additional load current. The result is that the real current limit decreases linearly with V_{IN} - V_{OUT}:

$$I_{E(max)} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}}$$

for: $R_1 + R_2 \gg R_{SENSE}$
$V_{ADJ} \leq 1.5V$
$R_1' = R_1$.

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This technique can be susceptible to "latch-off". If a momentary short at the supply output causes I_E to drop to zero (pass transistor cut off), then V_{OUT} cannot recover when the short is subsequentially removed. To prevent this undesirable operation, one must ensure that $I_{E(max)} > 0$ when $V_{OUT} = 0$ and V_{IN} is at its minimum:

$$I_{E(max)} \Big|_{\substack{V_{OUT}=0 \\ V_{IN(min)}}} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}} > 0$$

$$\frac{0.1(V_{ADJ})}{V_{IN(min)}} > \frac{R_1}{R_1 + R_2}$$

$$R_2 > \frac{V_{IN(min)}\,R_1}{0.1\,(V_{ADJ})}\left(1 - \frac{0.1\,(V_{ADJ})}{V_{IN(min)}}\right)$$

Figure 12 shows an alternative foldback current limiting scheme which responds to decreased V_{OUT} only. This circuit gives the output characteristics of Figure 13, defined by the following relation:

$$I_{E(max)} = \frac{0.1}{R_{SENSE}} \cdot \left(\frac{R_1R_2\,V_{OUT} + R_2R_3\,V_{REF}}{R_1R_2 + R_1R_3 + R_2R_3}\right)$$

This technique is immune to "latch-off" because the minimum current limit is always non-zero.

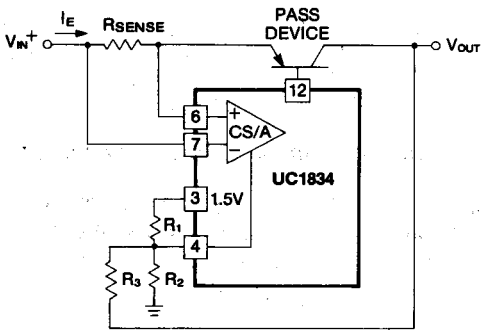

Figure 12. Foldback Current Limiting — Responds to Changes in V_{OUT} Only

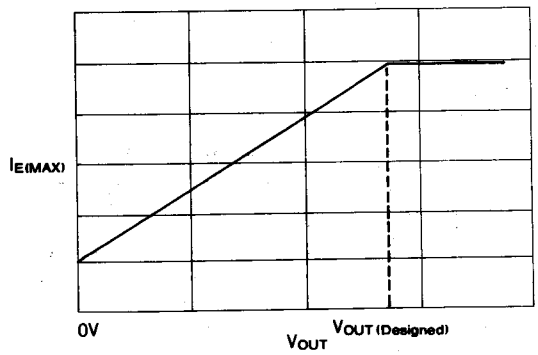

Figure 13. Foldback Current Limiting Characteristic

FAULT CIRCUITRY AND SYSTEM INTERFACING

In order to minimize the need for additional components, the UC1834 has on-chip provisions for fault detection and logic interfacing. These features are particularly useful when the linear regulator is part of a larger power supply system.

As shown in Figure 14, an internal comparator monitors the UC1834 E/A inputs. This comparator has two thresholds, for over- and under-voltage detection. Comparator thresholds are fixed at $|V_{N.I.} - V_{INV.}| = 150mV$. The resulting output voltage windows for non-fault operation are:

$$\frac{\pm .150V}{1.5V} = \pm 10\% \text{ for positive (+) supplies}$$

$$\frac{\pm .150V}{2V} = \pm 7.5\% \text{ for negative (-) supplies.}$$

A fault delay circuit prevents transient over- or under-voltage conditions (due to a rapidly changing load) being defined as faults. The delay time is programmable. An external capacitor at pin 11 is charged from an internal 75μA source. The delay period ends when the capacitor voltage reaches ~3.5V. The delay time is therefore ~47ms/μF. The fault alert output (pin 10) becomes an active low if an out-of-tolerance condition persists after the delay period. When no fault exists, this output is an open collector.

An over-voltage fault activates a 100mA crowbar gate drive output (pin 16) which can be used to switch on a shunt SCR. Such a fault also sets an over-voltage latch if the reset voltage (pin 15) is above the latch reset threshold (typically 0.4V). When the latch is set its $\overline{Q}$ output will pull pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents $\overline{Q}$ from pulling pin 15 below the reset threshold. However, pin 15 is pulled low enough to disable the driver outputs if pins 15 and 14 are tied together. With pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

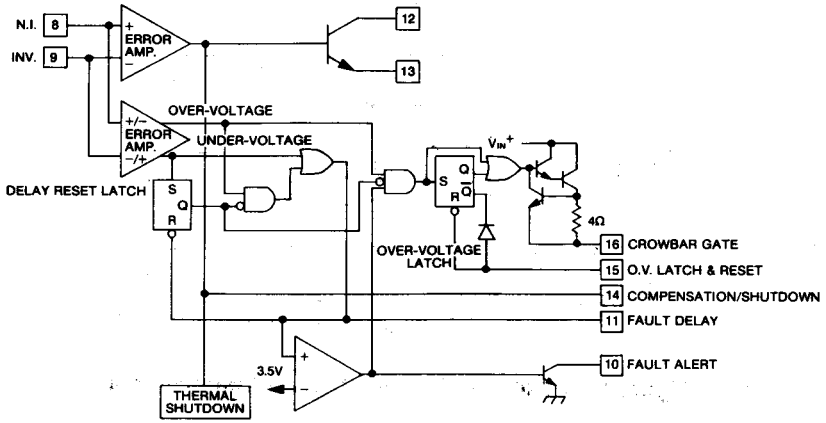

Figure 14. Fault Circuitry

An internal "delay reset latch" prevents crowbar turn-on when an under-voltage condition is immediately followed by a transient over-voltage condition. Such a situation could arise from a momentary short circuit at the supply output.

A thermal shutdown circuit pulls the E/A output low when junction temperatures reach 165°C, in order to protect the IC from excessive power dissipation in the drive transistor.

COMPENSATING THE FEEDBACK LOOP

A reliable design for any feedback system must yield a closed-loop frequency response which ensures unconditional stability. An optimum power supply response provides this stability while maximizing broadband gain for good dynamic voltage regulation with changing loads. Figure 15 illustrates such a response. The 0dB crossover frequency (f_C) should be as high as possible while maintaining phase margin above -360° at all lower frequencies (Nyquist stability criterion). In practice, this criterion dictates a single-pole response below f_C.

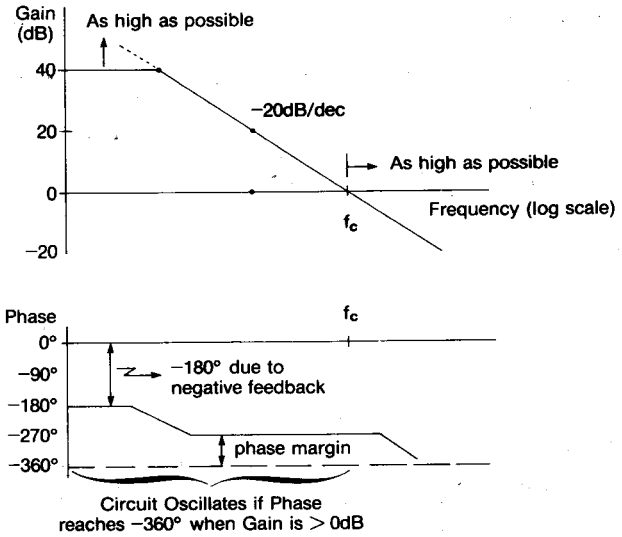

Figure 15. Desired Closed-Loop Response

Linear supplies using the UC1834 will usually have a current limiting loop in addition to the voltage control loop, as illustrated for two basic configurations* in Figure 16. Both loops must be stabilized for reliable operation. This is accomplished by appropriately compensating the E/A and CS/A at their common output (pin 14). Design of the compensation networks will often require an iterative procedure, since the compensation for one loop will affect the response of the other. A straightforward approach is outlined below:

1). Determine the frequency response of all voltage loop elements excluding the E/A. Appendix I offers guidelines for this step.

2). Design E/A compensation giving a frequency response which , when added to the response calculated in step 1, will yield a total loop characteristic consistent with the objectives outlined above. (Appendix II.)

3). Calculate the current loop response and determine whether it satisfies the Nyquist stability criterion. (Appendix III.) If not, add additional compensation and then recalculate the voltage loop response.

4). Iterate if necessary.

*All other configurations of Figure 3 are variants of these two, and can be treated in essentially the same ways.

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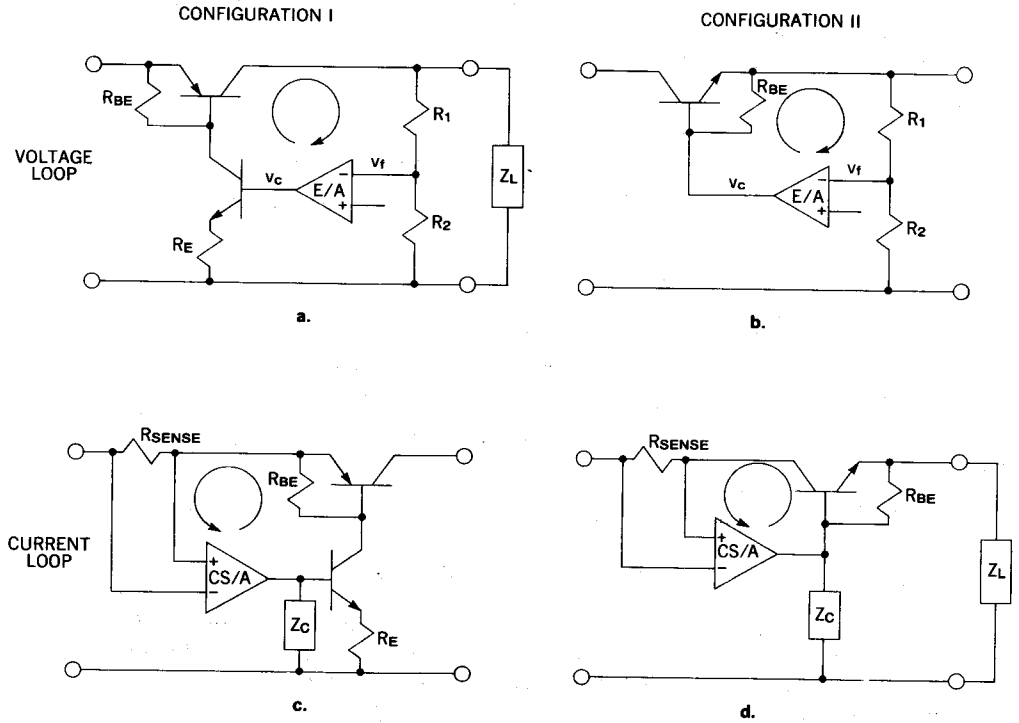

Figure 16. Voltage and Current Loops for Two Basic Configurations

EXAMPLE

Figure 17 shows a 5V, 5A (positive output) supply of the class shown in Figures 16a, c. This circuit tends toward instability when it is lightly loaded because of the high gain (β = 200) of the pass transistor at low currents. Output capacitor C_2 is needed to introduce a pole which rolls off the gain of the voltage loop to 0dB at 100kHz, avoiding instability due to the additional phase shift of a transistor pole at:

$$f = \frac{f_T}{\beta} = \frac{50MHz}{200} = 250kHz$$

Assuming a minimum load of 1A (R_L = 5Ω), the low frequency voltage loop gain, excluding the E/A, is (from Appendix I):

$$A_V = \frac{1}{15\Omega} \cdot 200 \cdot 5\Omega \cdot \frac{0.51k\Omega}{(1.7 + 0.51)\ k\Omega} = 20 = 26dB.$$

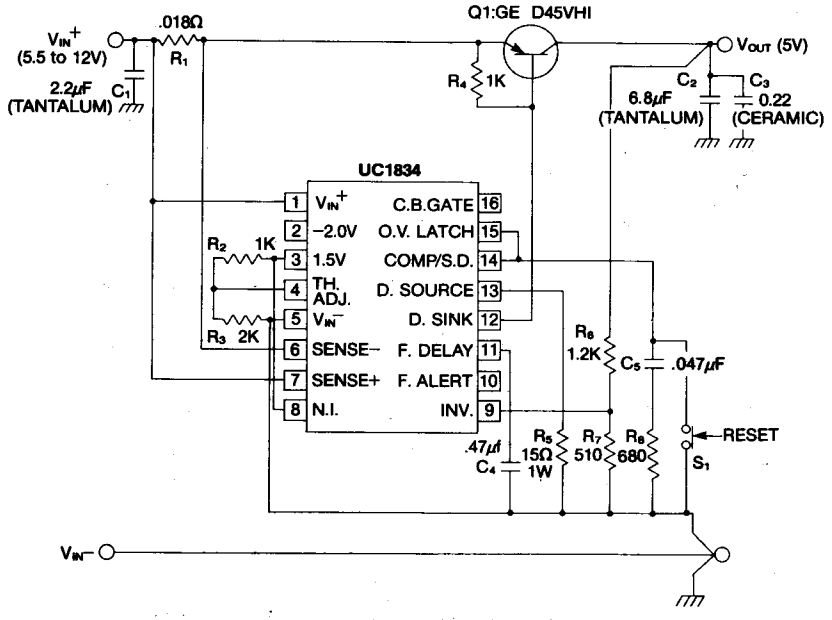

Figure 17. 0.5V Input-Output Differential 5A Positive Regulator

A pole at 5kHz is required in order to roll off from 26dB to 0dB at 100kHz. The required value of C_2 is therefore given by:

$$C_2 = \frac{1}{2\pi \cdot R_L \cdot f_p} = \frac{1}{2\pi \cdot 5\Omega \cdot 5kHz} = 6.4\mu F \text{ (6.8}\mu F \text{ used).}$$

The dashed curves of Figure 18a show the resulting voltage loop response, excluded the compensated E/A. Notice that the 5kHz pole (just added) itself introduces undesirable phase lag. This can be corrected by positioning the compensation zero (see Appendix II) at the same frequency. With $R_8 = 680\Omega$ (providing ~0dB E/A gain above 5kHz), then:

$$C_5 = \frac{1}{2\pi \cdot 680\Omega \cdot 5kHz} = .047\mu F.$$

The gain and phase of the compensated E/A (dotted lines) and complete voltage loop (solid lines) are also shown in Figure 18a.

The resulting current loop response (Figure 18b) is seen to meet the stability criterion. Gain above 5kHz is given by (from Appendix III):

$$A_I = \frac{1}{70\Omega} \cdot 680\Omega \cdot \frac{1}{15\Omega} \cdot 200 \cdot 0.018\Omega = 2.3 = 7.4dB.$$

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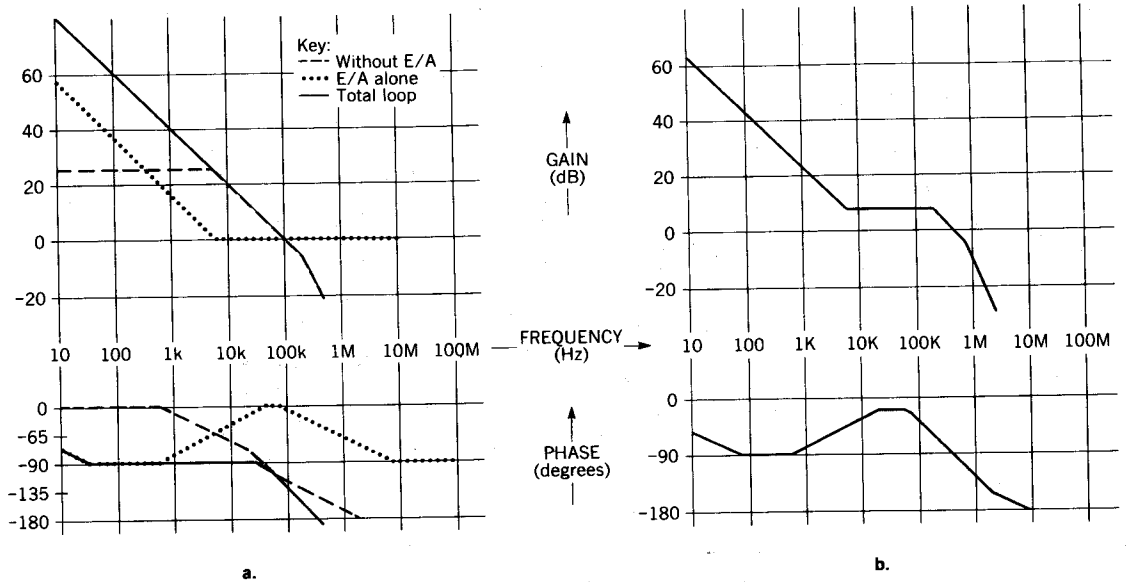


Figure 18. Loop Responses for Circuit of Figure 17
a. Voltage Loop
b. Current Loop

Reasonable phase margin (~40°) is maintained as the transistor and CS/A poles roll off this small gain to 0dB.

Figure 19 shows the UC1834 used to implement a negative output supply. A Darlington pass element provides adequate gain for operation at output current levels up to 10A.

CONCLUSION

Ever-increasing requirements for improved power supply economy and efficiency have produced a need for a versatile control IC capable of minimizing power losses in linear regulators. The UC1834 meets this need while also supporting all the auxilliary functions required of such supplies. This control circuit provides for optimized performance in a broad range of linear regulators, and in fact extends the range of applications for which such regulators are appropriate.

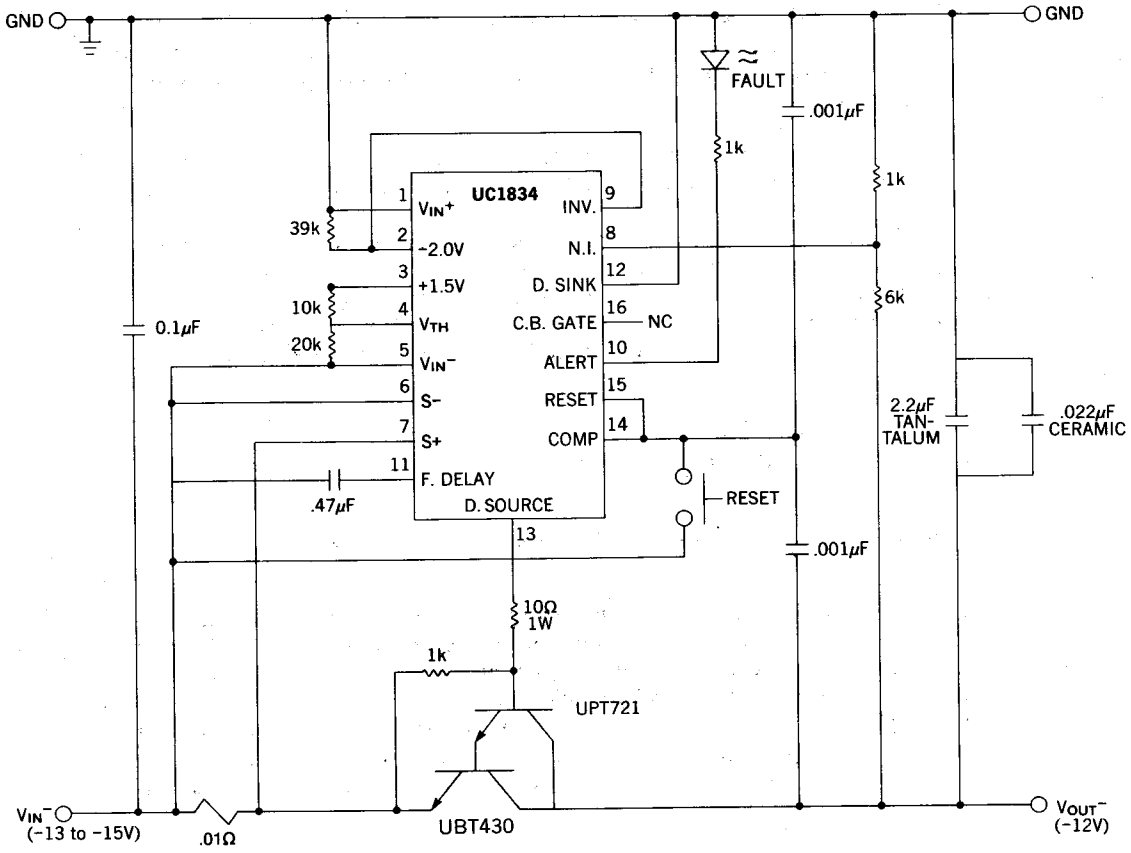


Figure 19. −12V, −10A Negative Regulator

APPENDIX I - FREQUENCY RESPONSE OF VOLTAGE LOOP ELEMENTS

A. The configuration of Figure 16a has, in addition to the compensated E/A, the following loop elements:

- **Drive Transistor** - R_E allows operation of the driver as an emitter follower. Together these elements have an effective small signal AC conductance of $1/R_E$.

- **Pass Transistor** - Low frequency gain (β) and unity-gain frequency (f_T) are usually specified. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/\beta$. Therefore, in order to maintain phase margin at low frequencies, the best choice for a pass device is often a high frequency, low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor (R_{BE} in Figure 16a) which increases the pole frequency to:

$$f_p = \frac{f_T}{\beta}\left(1 + \frac{\beta \cdot r_e}{R_{BE}}\right)$$

where: $r_e = \frac{kT}{qI_C} = \frac{0.026mV}{I_C}$ (at T = 300K).

- **Load Impedance** - Load characteristics vary greatly with application and operating conditions. The most commonly used models and their respective (s domain) transfer functions are given in Table 1. Note that there are no poles in the transfer functions of those loads which lack shunt capacitance. This can result in a loop transfer function which cannot be rolled off to 0dB at a suitably low frequency using simple E/A compensation networks. For this reason a shunt output capacitor is often added to supplies which must drive loads having low or indeterminant capacitance.

- **Voltage Divider** - The output sensing network introduces a gain of $R_2/(R_1 + R_2)$.

- **Total Loop Gain,** excluding the E/A, is therefore given by:

$$A_V = \frac{v_c}{v_f} = \frac{1}{R_E} \cdot \beta_{PASS} \cdot Z_L \cdot \frac{R_2}{R_1 + R_2} \qquad \text{for } f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right).$$

B. The circuit of Figure 16b has a more straightforward response, since the only element (other than the E/A) which introduces any gain is the voltage divider:

$$A_V = \frac{R_2}{R_1 + R_2}$$

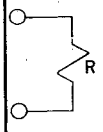
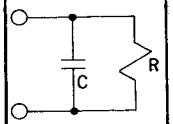
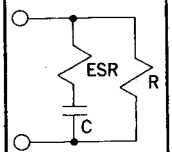
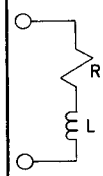
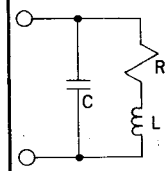
Load Model	Transfer Function	Poles @ f =	Zeros @ f =
	$Z_L(s) = R$	———	———
	$Z_L(s) = \frac{R}{1 + sRC}$	$\frac{1}{2\pi RC}$	———
	$Z_L(s) = \frac{R(1 + s(ESR)C)}{1 + s(R + ESR)C}$	$\frac{1}{2\pi(R + ESR)C}$	$\frac{1}{2\pi(ESR)C}$
	$Z_L(s) = R + sL$	———	$\frac{R}{2\pi L}$
	$Z_L(s) = \frac{s\left(s + \frac{R}{L}\right)}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$	$\frac{-R/L \pm \sqrt{R^2/L^2 - 4/LC}}{4\pi}$	$0, \frac{R}{2\pi L}$

Table 1. Load Models and their Transfer Functions

APPENDIX II - ERROR AMPLIFIER RESPONSE

Figure 20 shows the open-loop gain and phase response of the UC1834 E/A when lightly loaded. The gain curve represents an upper limit on the gain available from the compensated amplifier. Note that a second-order pole occurs near 800kHz. Stable circuits will require a 0dB crossover well below this frequency ($f_C \lesssim 500kHz$).

The E/A can be compensated with or without the use of local feedback. When operated without such feedback (Figure 21a) the transconductance properties of the E/A become evident; i.e. the voltage gain in given by:

$$A_{V(E/A)} = g_M Z_C \qquad (f \lesssim 500kHz)$$

where: $g_M \approx \frac{1}{700\Omega} = 1.4mS$

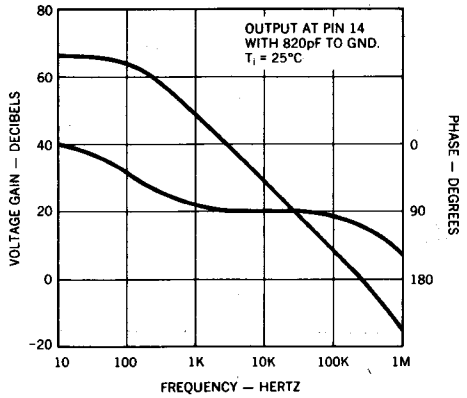


Figure 20. Error Amplifier Gain and Phase Frequency Response

When the E/A has local feedback (Figure 21b), its gain is, to a first approximation, independent of transconductance:

$$A_{V(E/A)} = \frac{Z_F}{Z_{IN}} \qquad (f \lesssim 500kHz)$$

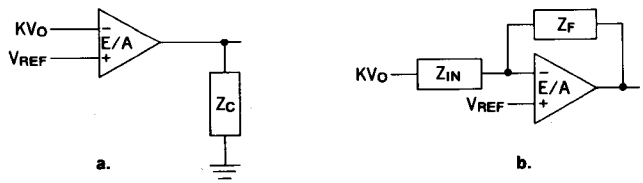


Figure 21. E/A Compensation (a.) Without and (b.) With Local Feedback

However, the use of local feedback creates an additional loop which must be independently stable. The UC1834 has no internal compensation to ensure this stability, so additional external compensation is usually required. An 820pF capacitor from the E/A output to ground will stabilize this inner voltage loop while also enhancing current loop stability.

An additional drawback to the use of local feedback is that Z_F places a DC load on the E/A output. With a transconductance amplifier this results in additional input offset voltage:

$$\Delta V_{IO} = \frac{I_{E/A\,OUT}}{g_M}$$

This offset results in degradation of DC regulation. The problem can be averted by taking local feedback from the emitter of the drive transistor if the driver is configured as an emitter-follower.

Whatever the compensation scheme, the UC1834 E/A output can sink or source a maximum of 100μA.

Table 2 shows two typical compensation schemes and the resulting E/A transfer functions. The first of these circuits is most widely used.

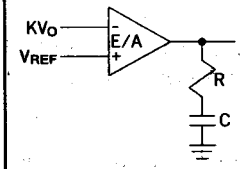
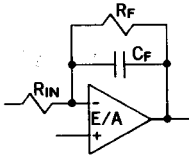
Compensation Circuit	E/A Gain ($A_{V(E/A)}(s)$)	Poles @ f =	Zeros @ f =
	$A_V = \frac{g_M(1 + sRC)}{sC}$	0	$\frac{1}{2\pi RC}$
	$A_V = \frac{R_F}{R_{IN}(1 + s\,R_F C_F)}$	$\frac{1}{2\pi\,R_F C_F}$	———

Table 2. E/A Compensation Circuits and Gain Response

APPENDIX III - FREQUENCY RESPONSE OF THE CURRENT LOOP

- **CS/A** - Figure 22 shows the open-loop gain and phase response of the UC1834 CS/A. This is also a transconductance amplifier, having $g_M \approx 1/70\Omega = 14mS$. The voltage gain is analogous to that of the E/A. The E/A compensation impedance (Z_C or $Z_{F(E/A)}$) is also seen by the CS/A output. For purposes of small signal AC analysis, the CS/A will always see this impedance as being returned to $V_{\overline{IN}}$ (as shown in Figures 16c, d) when the E/A is compensated by either of the methods shown in Table 2.

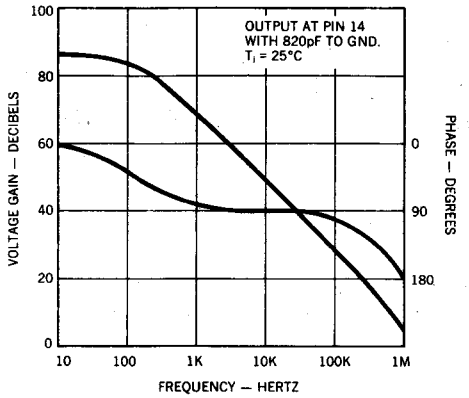


Figure 22. Current Sense Amplifier Gain and Phase Frequency Response

- **Pass Transistor** - Introduces current gain β to the loop transfer of both basic configurations (Figures 16c, d).Considerations outlined in Appendix I also apply here.

- **Sense Resistor** - Resistance value R_{SENSE} appears in transfer function for both configurations.

- **Drive Transistor** - In the circuit of Figure 16c, R_E allows operation of the driver as an emitter-follower. Effective conductance is $1/R_E$.

Closed-loop responses are given by the following:

for circuit of Figure 16c:

$$A_I = g_M \cdot Z_C \cdot \frac{1}{R_E} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

for circuit of Figure 16d:

$$A_I = g_M \cdot \frac{Z_C}{Z_C + \beta Z_L} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right).$$

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