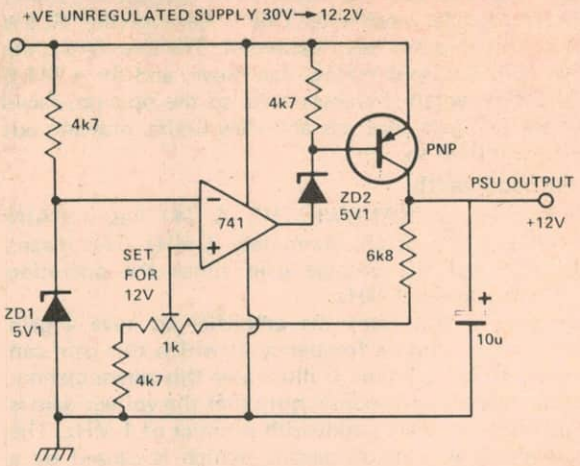
12 V REGULATED POWER SUPPLY

The large open loop voltage gain of an op-amp is very useful in providing a regulated low output impedance power supply. A 5V1 voltage reference is generated by a zener diode ZD1 (this voltage reference could be made more stable by running it at constant current). A PNP transistor is used as a series regulator. However, this transistor inverts the signal from the op-amp output, and so, in order to get negative feedback, the feedback is taken to the non-inverting input! The operations is as follows. The inverting input is held at 5V1. If the 'PSU OUTPUT' tries to fall, the voltage at the non-inverting input falls. Therefore the op-amp's output will also fall, thus turning on the PNP transistor which then pulls up the 'PSU OUTPUT'. Thus the output voltage is stabilised. Also, the output impedance is very low, due to this negative feedback. The output impedance at high frequencies (where the op-amp gain is low) is further reduced by the 10 μ capacitor. To squeeze the last drop of voltage out of the system, before a collapsing unregulated supply rail causes the regulated supply to drop out, a 5V1 zener diode (ZD2) has been included. This allows the op-amp output to work at about 7 volts below the unregulated supply rail. Thus, a regulated output is maintained until the PNP transistor saturates. This means that the unregulated rail can fall to within about 200 mV of the regulated rail!



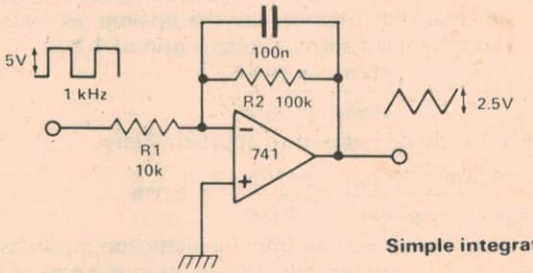
SIMPLE INTEGRATOR

An op-amp and a capacitor can be used to implement, to a high degree of accuracy, the mathematical process of integration. In this case, current is summed over a period of time and the resultant voltage generated is the integral of that current as a function of time. What this means that if a constant voltage is inputted to the circuit, a ramp with a constant slope is generated at the output. When the input is positive, the output of the op-amp ramps negative.

In doing so it pulls the inverting terminal negative so as to maintain a 'virtual earth' condition. In fact the input current (Vin/R1) is being equalled by the current flowing through the capacitor, thus equilibrium is maintained. The equation governing the behaviour of a capacitor is C x dV/dt = i, where dV/dt is the rate of change of voltage across the capacitor.

Therefore $\frac{dV}{dt} \quad \frac{i}{C}$ Thus $\frac{dV}{dt} \quad \frac{Vin}{R1C}$

So, when a square wave is applied to the circuit in Fig. 10, triangle waveforms are generated. R2 was added to provide DC stability. Its inclusion does slightly corrupt the mathematical processes, but not enormously. A good point about this integrator design is that it has a very low output impedance. You can put a load on the output and the op-amp will still generate the same waveform – that's what is so nice about negative feedback.



Simple integrator.

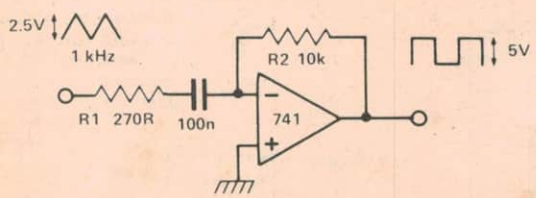


Fig. 11. Simple differentiator.

SIMPLE DIFFERENTIATOR

Mathematically, differentiation is the reverse process to integration. Thus, in the differentiator circuit the C and the R are reversed with respect to the integrator circuit.

The input waveform is a triangle with a constant rise and fall slope. This constant slope, when presented to a capacitor will generate a constant current. When the slope direction reverses, then so will the current flow. This current when passed through a resistor (R1), will then generate a square wave.