design ideas

Edited by Bill Travis

Scheme adds sequencing and shutdown control to regulator

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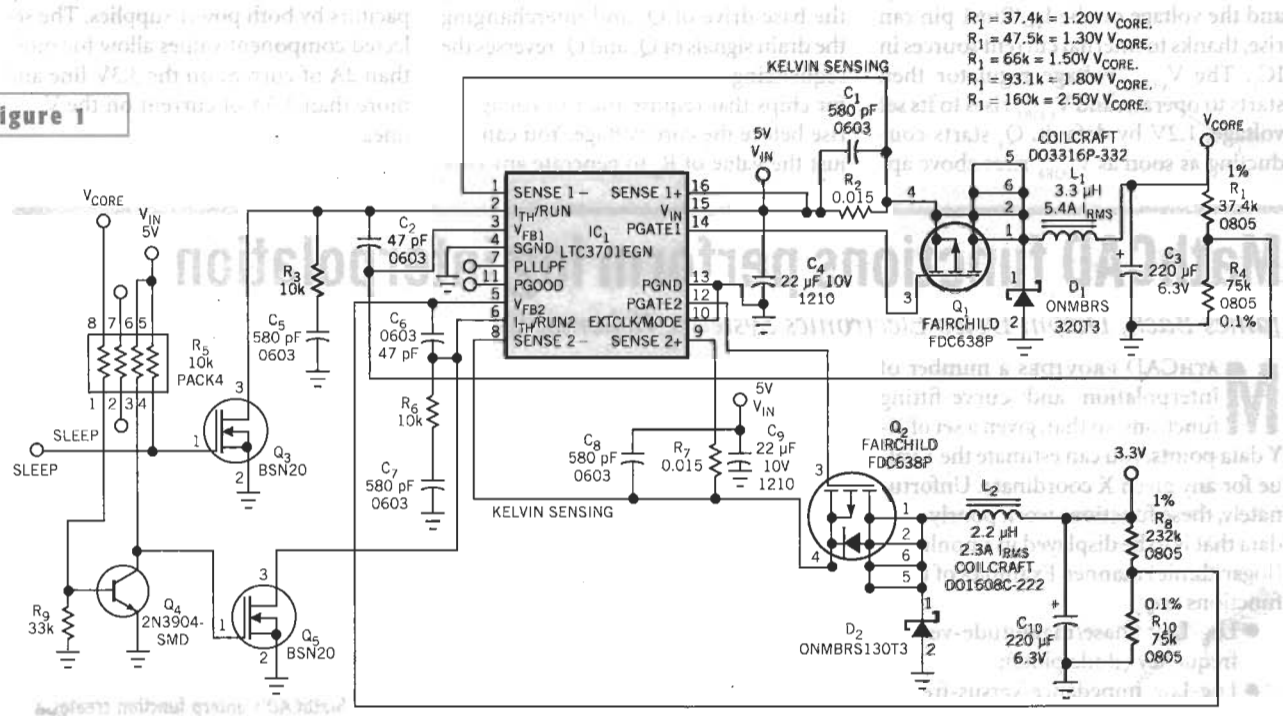
Modern microprocessor- or FPGA-based circuits require separate and independent power-supply voltages for the core and the I/O circuits. Some devices require stringent control of the turn-on characteristics and sequencing of these multiple power supplies to avoid internal parasitic current flows and consequent latch-ups. Although regulators exist with specific soft-start and shutdown inputs, it may be more cost-effective to use regulators that do not inherently provide these features and to add these features with external discrete devices. This Design Idea shows how to use an inexpensive Linear Technology (www.linear.com) LTC3701 dual switching regulator to provide a sequenced, and standby-controlled, power supply for an Equator Technologies (www.equator.com) broadband-signal processor. You can also adjust the circuit for FPGA or generic microprocessor applications. The features of the circuit in **Figure 1** increase the regulator's stability beyond what you can achieve with the standard Linear Technology application-note circuit.

The LTC3701 switching regulator, IC_1, provides two independently adjustable output voltages with very high voltage accuracy at a cost compatible with consumer-type applications. Because of cost constraints, it does not provide the soft-start or shutdown features present in other switching regulators. This design adds three discrete transistors to the conventional regulator circuitry to provide both arbitrary power-on-sequencing control and a simultaneous-shutdown feature. Q_3, Q_4, and Q_5 are inexpensive discrete

Figure 1



Adding a few transistors to a switching regulator adds power-sequencing and shutdown control to a power supply.

devices that control the voltage on the regulator's I_{TH}/Run pins. The I_{TH}/Run pins of IC_1 provide an external compensation to the internal feedback loops; they can also serve to shut down the device when you pull them to ground. A microprocessor's TTL/CMOS-compatible input signal (Sleep) controls the power state of the circuit. You can put the circuit into shutdown mode by either letting the Sleep pin float high or pulling it higher than approximately 1.5V. Q_3 then connects the I_{TH}/Run1 pin to ground, which causes the V_{CORE} core-voltage supply to shut off. The V_{CORE} voltage then drops toward ground, and Q_4 stops conducting when V_{CORE} falls below approximately 0.8V. The gate of Q_5 pulls to the 5V unregulated input voltage, and Q_5 shorts the I_{TH}/Run2 pin to ground, which turns off the 3.3V regulator. The circuit is now in standby mode, and both power supplies are off.

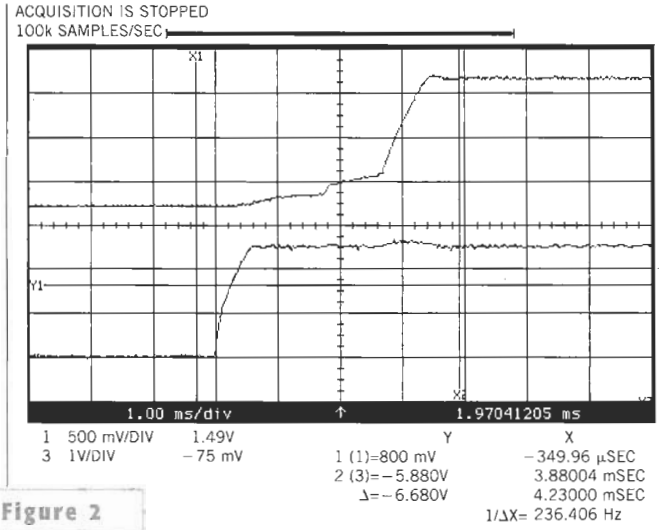


Figure 2

The 3.3V supply turns on several milliseconds after V_{CORE} attains an established level.

Pulling the Sleep pin lower than approximately 0.8V turns on the power supply and sequences the voltages in the following manner: Q_3 stops conducting, and the voltage on the I_{TH}/Run1 pin can rise, thanks to internal current sources in IC_1. The V_{CORE} voltage regulator then starts to operate, and V_{CORE} rises to its set voltage, 1.2V by default. Q_4 starts conducting as soon as V_{CORE} rises above approximately 0.8V. This action turns off Q_5 and allows the I_{TH}/Run2 pin voltage to start rising. The 3.3V power supply thus turns on. The combined effect of driving Q_4 and Q_5 from the V_{CORE} voltage is that the 3.3V I/O voltage always turns on only after the V_{CORE} voltage attains an established level. The end result is to sequence the power supplies over a period of 4 msec (**Figure 2**).

The circuit is symmetric, and changing the base drive of Q_4 and interchanging the drain signals of Q_3 and Q_5 reverses the sequencing order of the power supplies for chips that require the I/O voltage to rise before the core voltage. You can adjust the value of R_1 to generate any core voltage above approximately 1V. You may need to adjust the value of R_9 if your design requires core voltages below approximately 1V. You can replace Q_3 and Q_5 by potentially cheaper industry-standard 2N2007 devices at the expense of slightly higher capacitive loading on the I_{TH}/Run pins of IC_1. C_2 and C_6 are compensation capacitors that the Linear Technology literature does not mention but that are highly effective in preventing subharmonic oscillation arising from dynamic current loading on the outputs. (See the Linear Technology Web site for information on subharmonic oscillation.)

The gate-drain-source capacitance of Q_3 and Q_5 also add to the stability of the loop filter. Note that sequencing the turn-on ramps of the power supplies also has the benefit of reducing the inrush current into the power supply by staggering this current and preventing simultaneous current loading of the primary bypass capacitors by both power supplies. The selected component values allow for more than 2A of current on the 3.3V line and more than 3.5A of current on the V_{CORE} line.□