SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

OPTIMISED POWER STAGES FOR HIGH FREQUENCY 380/440VAC MEDIUM POWER SWITCH MODE SUPPLIES

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ABSTRACT

This paper presents the elements necessary to make the optimum choice of power semiconductors (for the transistors and secondary diodes) and the power stage configurations for medium power SMPS (from 1kVA to 15kVA).

The power stage practically realized comprises of an asymmetrical bridge forward converter. An optimised power switch combining bipolar and MOSFET technologies is developed. It is capable of switching in excess of 50A at 25kHz on the 380/440VAC rectified three phase mains.

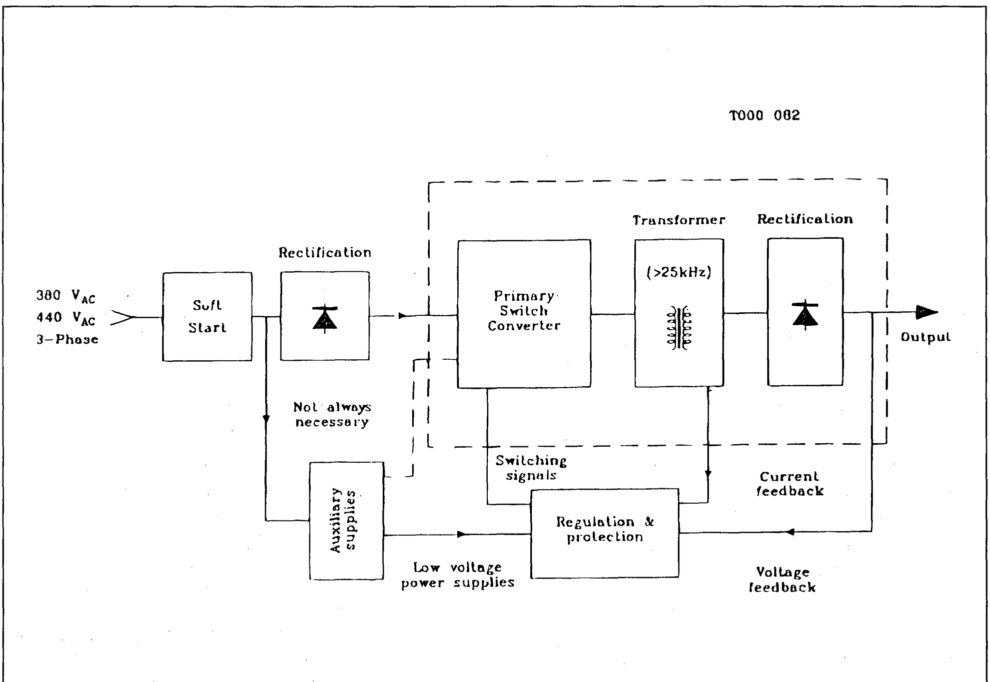
Secondary diode choice depends largely on the transformer ratio and the desired output D.C. voltage. Conduction losses at 25kHz govern the choice of secondary diodes.

INTRODUCTION

System designers of switch-mode solutions for electric welders, battery chargers and computer power supplies need to choose the power-stage configuration, power semiconductors and regulation best suited for their application. This paper provides data necessary to make this choice.

Figure 1 illustrates a system block diagram of a typical medium power SMPS with the primary operating directly on the 380/440VAC rectified mains. The paper limits the discussion to the power-stage of the SMPS. Power stage configurations such as asymmetrical bridge, full-bridge and half-bridge converters are compared. Bipolar and MOSFET technologies are compared. Schottky and fast recovery epitaxial diodes are considered for the secondary rectification.

Figure 1 : Block Diagram of a Medium Power SMPS.

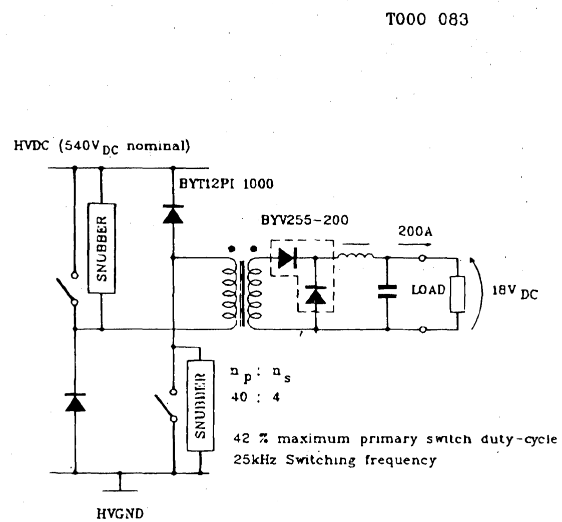


POWER STAGE CONFIGURATIONS

For medium power applications (1kVA to 15kVA), the choice of the converter on the 3-phase industrial mains is between the asymmetrical bridge, capacitor-split half-bridge and full-bridge converters [1]. The half-bridge and full-bridge converters are symmetrical converters and thus require smaller input filtering than asymmetrical bridge converters. However, it is possible to combine two asymmetrical bridge converters operating in antiphase in order to obtain a power stage, which viewed from its input and output current waveforms, appears to be a symmetrical full-bridge converter.

The asymmetrical bridge converter (figure 2) comprises of two power switches in series with the load connected between the two switches. Simultaneous conduction of these power switches when a fault condition exists on the secondary of the transformer is not catastrophic as there is at least the leakage inductance of the transformer limiting the rate of rise of primary switch currents. The controlled rate of rise of primary current enables low-cost feedback protection circuits to react to the fault condition and turn-off the primary switches.

Figure 2 : Asymmetrical Bridge Converter - The Developed Power Stage.



The use of turn-off switching-aid-networks (snubbers) does not pose a problem in asymmetrical bridges. In half-bridge and full-bridge converters, the use of turn-off snubbers generally necessitates the use of turn-on snubbers required to limit the rate of rise of primary switch currents [2].

The developed power stage utilizes the asymmetrical bridge converter because of these reasons.

For very high output power capability (in excess of 10kVA), the full-bridge converter can be the optimum choice provided the circuitry necessary to maintain volts-seconds symmetry can be easily implemented. The full-bridge operates the transformer in two magnetic quadrants. Consequently the size of the transformer can be reduced. Figure 3 illustrates a full-bridge converter which incorporates the advantages of the asymmetrical bridge structure (no catastrophic simultaneous conduction of transistors and easy snubber networks) with the advantages of the symmetrical converter of reduced transformer size.

TECHNOLOGY CHOICE

Bipolar and MOSFET technologies are best adapted for high frequency (greater than 20kHz) medium power SMPS. Figure 4 illustrates the on-state resistance for 1mm^2 of silicon surface versus blocking voltage for high voltage power MOSFETs. The resistance of the epitaxial layer required to withstand blocking voltage V_{DS} (in excess of 250V) is approximately proportional to $V_{DS}^{2.5}$. Consequently, even if this theoretical limit is approached, the on-state resistance increases rapidly as blocking voltage V_{DS} increases for high voltage power MOSFETs.

Figure 3 : A Quasi-asymmetrical Full-bridge Converter.
– Transformer provides inductance between two switches in series.

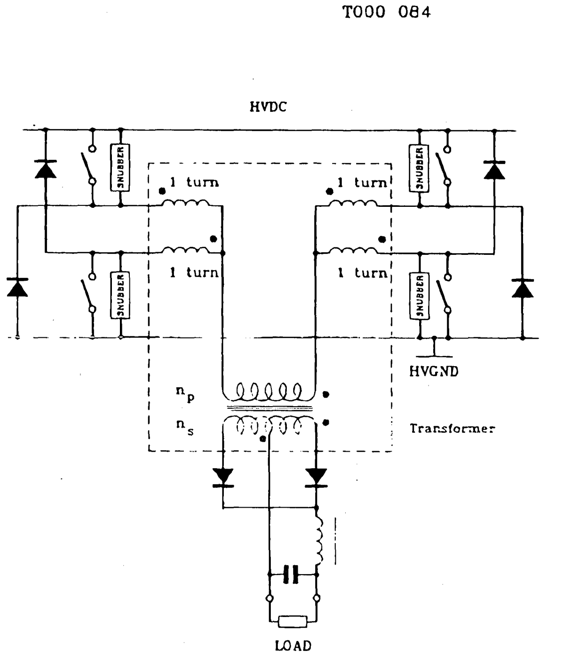
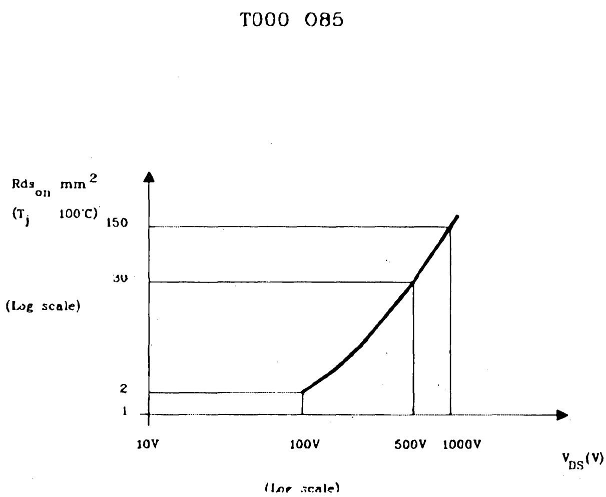


Figure 4 : MOSFET Blocking Voltage versus on-state Resistance/mm^2.



The current density for a 1000V bipolar transistor, such as a BUF410A is in the region of $0.4A/mm^2$ when conducting a nominal current of 10A with an on-state collector-emitter voltage of 2V maximum at 100°C junction temperature. The equivalent on-state resistance for a 1000V bipolar is thus approximately 5 Ohm/mm^2 whereas for a 1000V Power MOSFET is 100 Ohm/mm^2. For an application specifying only nominal switching current capability, the Power MOSFET solution requires 30 times more silicon than the equivalent bipolar solution (not considering the drive requirements) resulting in substantially higher power transistor cost.

Even though higher current density is achieved with bipolar transistors, the Power MOSFET has the clear advantage of a larger safe operating area at turn-off, larger peak current capability and easy voltage controlled gate drive. The 1000V bipolar transistor has the disadvantage of longer turn-off delay time (due to its storage time) and high drive current requirements. A cost comparison of a Power MOSFET based solution with a bipolar based solution should thus be based on cost of the switch together with its drive, protection and auxiliary power supply circuits.

Quantitative comparison is complicated by the very different operational characteristics of Power MOSFETs and bipolar transistors. However, qualitative comparison leads the authors to conclude the following :

1) In medium power SMPS, where bipolar and Power MOSFET technologies can be used, the technology comparison must be based on cost evaluation of solutions meeting the specification both for PEAK transistor switching current as well as AVERAGE/RMS transistor switching current.
2) Generally the Power MOSFET is sized for the RMS transistor switching current, whilst verifying that the peak current capability of the device meets the specification.
3) The bipolar solution is sized on the peak transistor switching current specified in the application.

THE DEVELOPED POWER STAGE

The developed power-stage has the characteristic listed in table 1. The asymmetrical bridge forward converter was used with the maximum duty cycle limited to approximately 40%. The continuous rated primary current was 20A (for 40% duty cycle). The peak primary switch current capability was 50A. The transformer design (provided in appendix I) had a primary to secondary turns ratio of 10 to 1. Consequently the continuous rated secondary output current was 200A at a secondary output voltage of approximately 18V. The secondary output peak current was 500A when primary switch current was 50A.

Table 1 : Developed Power Stage Characteristic.

Comments	Value
Input Supply Voltage	$380/415/440V_{AC}$
Continuous Primary Current	20A
Peak Primary Current	50A
Maximum Duty Cycle	40%
Switching Frequency	25kHz
Continuous Secondary Current	200A
Peak Secondary Current	500A
Secondary Voltage (nominal)	18V

THE ASYMMETRICAL BRIDGE CONVERTER

A solution for the converter, based on bipolar and Power MOSFET technologies, encompassing the advantages of high switching current density and voltage controlled drive, was developed : this converter for the power stage was based on the CASCODE switch [3]. Due to the relatively large nominal primary switch current (20A), a bipolar based solution was necessary. The CASCODE switch required a simple voltage controlled drive signal. No floating auxiliary supplies were required as the base current for the bipolar transistor was provided by a proportional current transformer. Figure 5 illustrates the primary CASCODE switch (based on bipolar and MOSFET technologies) which is used in the asymmetrical bridge converter.

The switch comprises of a BUV298A bipolar transistor (B1) in ISOTOP package and a high density 50V (23 mOhm at 25°C) Power MOSFET STHVD90 (F1) connected in CASCODE. A 1000V Power MOSFET STHV102 (F2) provides the initial base current. A 50V Power MOSFET BUZ11 (F3) turns-on when the STHVD90 CASCODE MOSFET (F1) is turned-off. Consequently the collector current is extracted via the base through Power MOSFET F3. A turn-off snubber (comprising of R1, D1 and C1) maintains the turn-off within the reverse bias safe operating area (RBSOA) of the bipolar BUV298A.

The primary switch conduction losses (at nominal 20A current for 40% duty cycle) are approximately 30W at a 100°C junction temperature for the CASCODE switch. The primary switch could be based purely on 1000 volts Power MOSFETs (STHV102, 3.5 ohm at 25°C) in parallel. However, for 10 of these Power MOSFETs in parallel, under the same operating condition, the conduction losses would be approximately 90W.

Figure 6 illustrates a pulse transformer gate drive used with the primary switches. This gate drive provides positive and negative bias of the Power MOSFETs in the CASCODE switch. The pulse transformer also provides the isolation between the primary switches and the control logic. With this gate drive, the asymmetrical bridge converter requires no auxiliary power supplies.

Figure 5 : The Developed CASCODE Asymmetrical Bridge Converter.

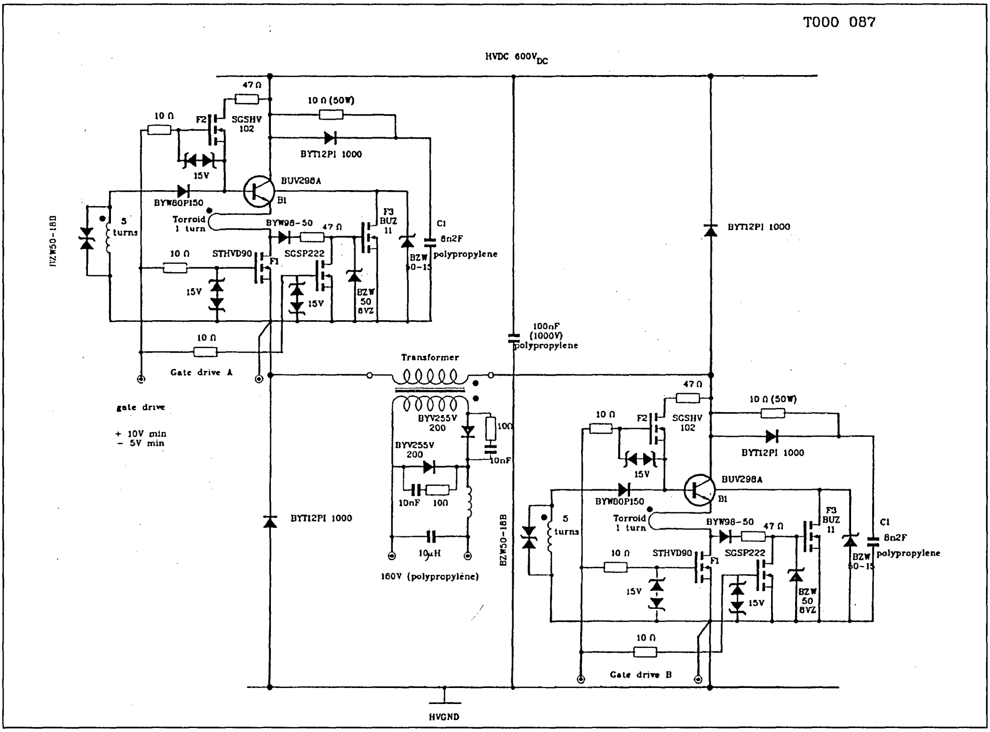
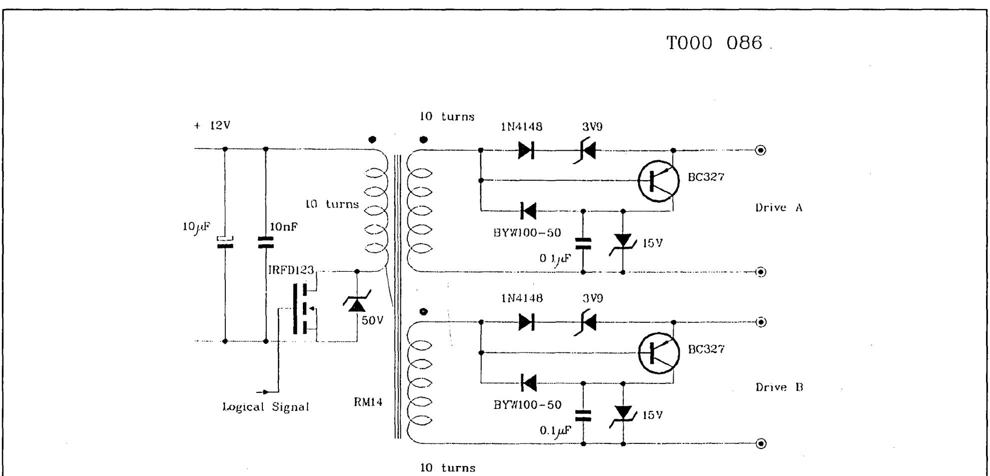


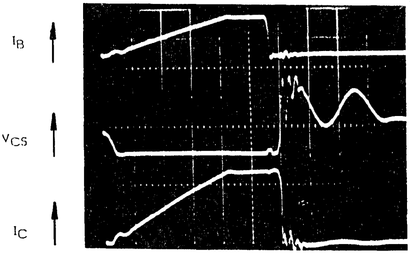
Figure 6 : Isolated Pulse Transformer based Gate Drives for Power Stage.



ASYMMETRICAL BRIDGE OPERATION

Figure 7 illustrates the extremely fast switching and short (less than 500ns) storage time at turn-off obtained using this CASCODE switch. The primary switch was tested with a bridge high voltage DC rail of $600V_{DC}$, primary current of 50A at 25kHz switching frequency.

Figure 7 : CASCODE Primary Switch Commutation – (I_{PEAK} = 50A).



t = 1µs/div
I_B = 10A/div
V_{CS} = 200V/div
I_C = 20A/div

SECONDARY RECTIFYING DIODES

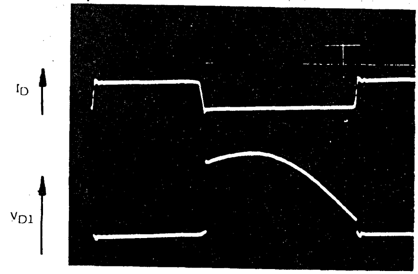
The transformer had a primary to secondary turns ratio of 10 to 1. Consequently the voltage experienced by the secondary diodes at $600V_{DC}$ HVDC was 60V in addition to any overvoltage due to parasitic inductances.

Schottky diodes which have extremely low conduction voltage (approximately 0.4V) can not be used for this application as they are limited in blocking voltage to approximately 50V. If the secondary output voltage was 5V (for example, computer applications), the transformer ratio would have been higher thus permitting the use of Schottky diodes.

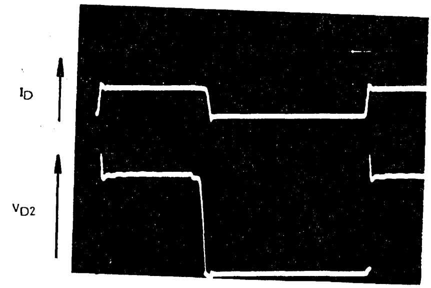
The diodes best suited for the specified secondary output are fast recovery epitaxial diodes ('FRED'). FRED diodes BYV255V200 were used in the circuit having conduction voltages of approximately 0.85V at rated current and at 125°C junction temperature. Figure 8 illustrates the blocking voltage experienced by the secondary diodes with resistor/capacitor snubber networks.

At continuous rated output power, each secondary diode conducts for approximately 50% of the time an average current of 100A. Assuming a junction temperature of 125°C, the instantaneous forward voltage drop is 0.85V at approximately 100A. Hence diode conduction losses are approximately 85W ; (0.85Vx100A = 85W).

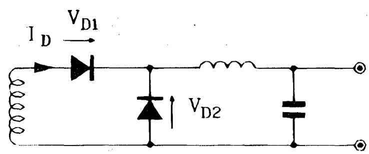
Figure 8 : Secondary Diode Switching Waveforms.



5µs/div
V_{D1} = 20V/div
I_D = 50A/div



5µs/div
V_{D1} = 20V/div
I_D = 50A/div



The leakage inductance between primary and secondary of the transformer is generally large such that the rate of decay of current in these diodes is controlled. Hence the reverse recovery is not critical. Thus at 25kHz switching frequency conduction losses are the prime criteria for the choice of the secondary diodes.

CONCLUSION

Bridge converters for medium power SMPS (1kVA to 15kVA) have been discussed. Turn-off snubbers and low-cost protection circuitry can be used with asymmetrical converters. A quasi-asymmetrical full-bridge converter has been proposed for high power SMPS which operate the transformer in two magnetic quadrants.

The 1000V Power MOSFET is a well adapted choice for low continuous power SMPS especially when high pulse current capability is specified for the primary switch. Bipolar transistors have high current density and are better adapted for medium power SMPS.

The choice of secondary diodes at 25kHz switching frequency is based primarily on conduction losses.

The developed power stage utilized the CASCODE configuration for the primary switch. This solution had the advantages of both the bipolar and Power MOSFET technologies. Fast epitaxial rectifying diodes (FRED) have been used in this power stage.

REFERENCES

1. SGS-THOMSON Microelectronics, 1984, "Transistor and Diodes in Power Processing", 187-198.
2. SGS-THOMSON Microelectronics, 1978, "The Power Transistor in its Environment", Chapter 8, 181-206.
3. Robinson F. and Williams B.W., 1987, "Emitter Switching High-Power Transistors", EPE Conference, 55-59.

ANNEX I

TRANSFORMER DESIGN

The transformer design parameters for the developed asymmetrical bridge forward converter are :

$V_{MIN} = 500V_{DC}$	$V_{MAX} = 600V_{DC}$
$V_{OUTPUT} = 18V$	$I_{OUTPUT} = 200A$
Duty cycle = 0.4 (MAX)	Freq. (f) = 25kHz

For forward converter operation equation [1] provides an approximate practical method of calculating the ferrite cross-sectional area.

$$S = K\sqrt{V_{OUTPUT}.I_{OUTPUT}} = 900mm^2 \qquad [1]$$

S = cross-sectional area in mm^2

V_{OUTPUT} = Output secondary voltage

I_{OUTPUT} = Output secondary current

K = 15 (for B50 ferrite material).

Two GER65/33/27 (LCC) E shape B50 ferrites were sandwiched together to form a ferrite core cross-sectional area (S) of $1064mm^2$.

Minimum number of primary turns (N_p) can be calculated using equation [2].

$$N_P > \frac{V_{MAX}.\text{Duty cycle}}{B_{MAX}.S.f} > 36 \qquad [2]$$

N_P was made equal to 40.

The number of secondary turns can be calculated using equation [3].

$$N_S = \frac{V_{OUTPUT}.N_P}{V_{MIN}.\text{Duty cycle}} > 3.6 \qquad [3]$$

N_S was made equal to 4. Hence the primary to secondary turns ratio was 10 to 1. Consequently peak primary current (20A) was one tenth of 200A secondary current.

The primary RMS current can be calculated using equation [4].

$$I_{RMS} = I_{PEAK}.\sqrt{\text{Duty cycle}} = 20\ \sqrt{0.4} = 12.5A \qquad [4]$$

Using a current density of $5A/mm^2$, the primary was wound using two wires in parallel of 1.25mm diameter.

The secondary wire cross-sectional area was $20mm^2$ calculated in a similar manner as for the primary wire.

MEASURED PARAMETERS

Leakage inductance = 90µH

(secondary short-circuited)

Primary inductance = 17.5mH

Insulation material used between primary and secondary was capable of supporting $1500V_{AC}$ at 50Hz. Three pieces of 0.65mm plastic film were used for this isolation.