POWER FACTOR CORRECTION WITH THE UC3854

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POWER FACTOR: WHAT CAN BE DONE TO IMPROVE IT

In an electric power distribution line, the power factor is the ratio of real power (watts) to apparent power (volt-amperes). The optimum value for this ratio is unity, a value that is obtained only when the line current is sinusoidal and in phase with the line voltage — assuming, of course, that the line voltage is itself sinusoidal. This means that any current component in quadrature with the fundamental, and any components at frequencies other than the fundamental (harmonics), cannot carry any power to the load. However, these components contribute to total line losses, and because they add to the current actually required by the user, they mandate the use of heavier wiring and circuit breakers, which means increased installation costs.

In the past, the main cause of low power factor was phase lag, caused by the inductive characteristic of the electric motors which accounted for a large portion of the overall load serviced by the electric power companies. In this case, the power factor is equal to the cosine of the phase angle — unity when the angle is zero. Phase lag can be corrected by simply adding the right amount of capacitance in shunt with the offending machinery, as has been done for many years.

With the advent of the electronics industry during the post-war decades and, more recently, the enormous increase in the number of computers and other equipment incorporating line rectifiers followed by capacitor-input filters, the nature of the problem has changed. The current drawn by these circuits is distinctly non-sinusoidal, as shown in Fig.1, The distorted current waveform in the figure is the sum of many components of different frequencies, the one at the fundamental line frequency being the only useful one. The resulting power factor may be as low as 50% under these conditions, and if the power involved is higher than several hundred watts, cost considerations alone make it imperative for equipment manufacturers to search for some means of improvement. In addition, there are environments — aboard submarines, for example — where the allowable percentage of harmonics in the line current is extremely low. In these systems, the use of an advanced form of power factor correction is a basic requirement.

With Unitrode's UC3854 High Power Factor Preregulator, the task of reducing the amount of distortion in the line current waveform becomes easy and cost-effective. This monolithic integrated circuit contains all the active control devices required to obtain power factors approaching unity, with only a handful of additional components needed to tailor the overall circuit to specific requirements. Furthermore, the device makes possible the design of a preregulator capable of operating over a wide range of power line voltages without any component or wiring changes. This means that the equipment can be plugged into any commercial power outlet in the world, regardless of the local voltage or frequency.

HOW THE UC3854 IMPROVES THE POWER FACTOR

In a simple power supply, such as the one shown in Fig. 1, the DC load draws current as needed from the "bulk" capacitor, while the full-wave rectifier replenishes the capacitor at each half-cycle with bursts of current that occur briefly at each voltage peak. The output voltage Vo is essentially constant, while the input AC current is badly distorted, as shown. We can eliminate this distortion with a high power factor PWM preregulator which, working between the rectifier and the bulk capacitor, forces the replenishing current to have the same waveshape as that of the line voltage. The same PWM circuit can be used to sense and to some extent regulate the output DC voltage.

Two independent feedback loops are involved. The inner current control loop must have a bandwidth wide enough to follow accurately the waveshape of the full-wave rectified line voltage. This waveshape is the sum of the following components:

	average DC value----------63.7% of Vpk
+	2nd harmonic----------42.4%
+	4th harmonic----------8.5%
+	6th harmonic----------3.6%
+	8th harmonic----------2.0%
+	10th harmonic----------1.3%
+	higher harmonics.

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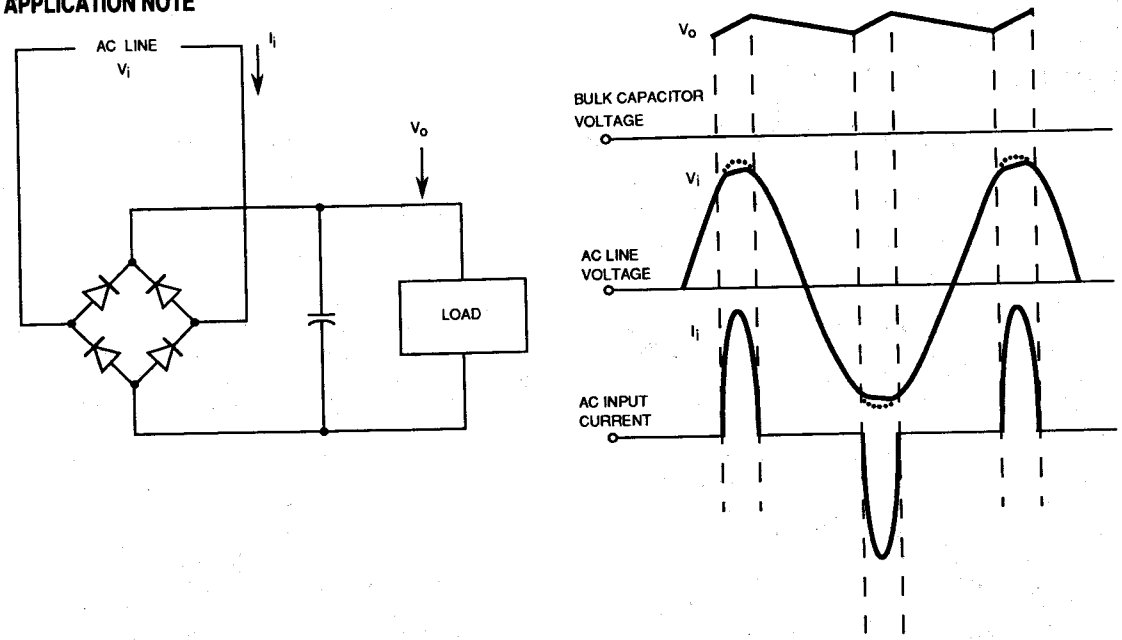

Figure 1. Voltage and current waveforms found in conventional capacitor filtered rectifiers.

Fig. 2 shows the first three of these components to scale. Because the amplitude of the 16th harmonic (960Hz for a 60Hz line) is only 0.5% of the input line voltage, with higher components becoming progressively smaller, a current loop bandwidth of a few kilohertz is adequate to accommodate all of the significant signal components. The PWM switching frequency must be well above the unity gain crossover frequency of the loop.

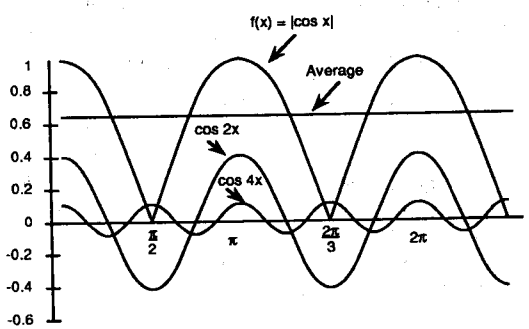

Figure 2. Rectified cosine wave f(x) = |cos x|, with average (DC value), second, and fourth harmonics shown. (Higher harmonics have been left out for clarity.

By sensing and controlling the average current value — rather than peak, as is done in some schemes — we maintain the same extremely low level of distortion in line current over the full range of current values, even though the required boost inductor value is quite low. This means that the mode boundary (between continuous and discontinuous modes), that is inevitable at some low current value, is of no concern to us, since the loop knows and controls the right thing: the average value of current.

Because load current varies, a voltage control loop is also required. (See Fig. 3). This outer loop senses the bulk capacitor voltage and keeps it constant by regulating the line current as required by the changing load. Unlike the current control loop, this feedback circuit must have a narrow bandwidth to prevent the voltage ripple (at twice the line frequency) from distorting the current waveform. Any interference of this type will defeat the main objective, which is to minimize the harmonic content of the line current.

Besides these two main functions, the UC3854 incorporates line voltage feedforward. This stabilizes the voltage control loop gain which would otherwise vary with the square of the line voltage. It provides fast constant power control when the line voltage varies, which also accounts for the wide range of

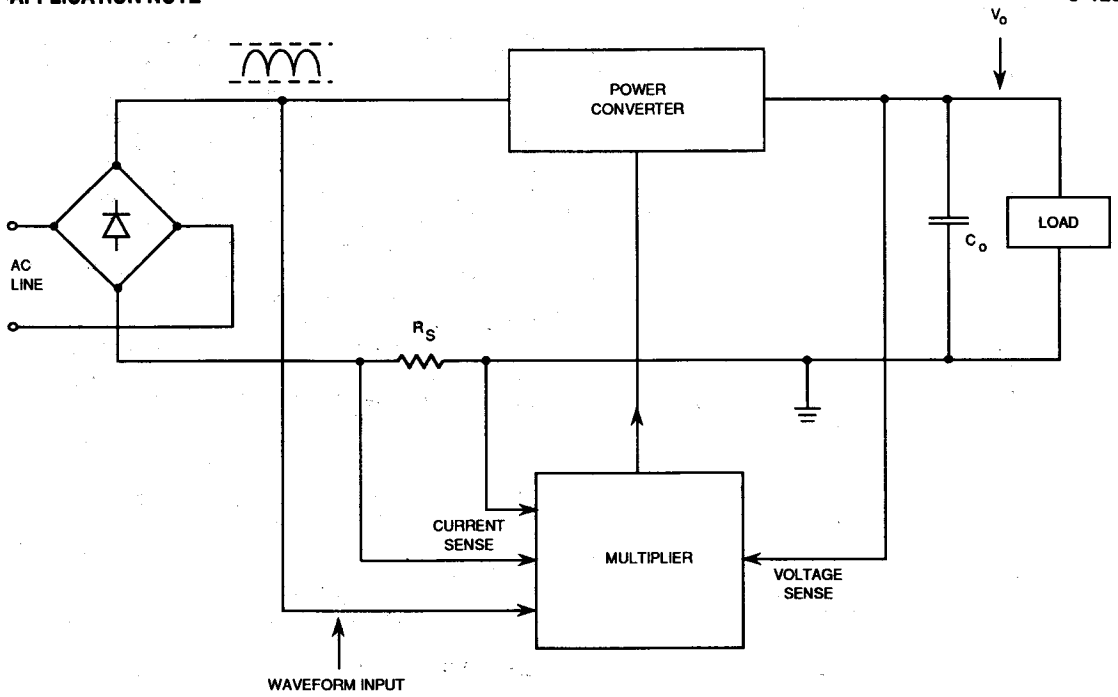

Figure 3. Basic configuration of high power factor control circuit, showing inner current loop and outer voltage loop.

input voltages that the preregulator can accomodate without any adjustments. (See Ref. 1 for an excellent treatment of this subject).

THE POWER OUTPUT CONVERTER

For the power stage, we have the choice of either a flyback, a buck, or a boost configuration (see Fig. 4). We will concentrate on the boost topology here, because it offers the most significant advantages. Its main characteristics are that the input current is not chopped, and that the output voltage must be higher than the highest input voltage peak. The benefits are:

1. Energy is more efficiently stored in the bulk capacitor at high voltage, allowing use of smaller capacitor.

2. Longer hold-up time due to high voltage.

3. Lower RFI/EMI in line.

4. The input inductor helps block fast line transients.

5. Control can be maintained over full swing of line voltage, including zero volts.

6. Inductor current IS input current, facilitating use of current-mode control.

7. The switch voltage is no greater than the output voltage.

8. Easy to drive PWM switch at ground level.

The switching diode of the boost stage (see Fig. 4) requires the output voltage Vo to have a value higher than the line peak value. To accomodate input line voltages up to 270Vrms, the value of Vo must be at least 380VDC.

By operating the boost converter in the continuous mode, we can minimize the noise injected into the line and reduce the peak current in the boost transistor and diode. In this mode, the inductor current flows during the entire PWM period, with a finite amount of ripple present. The required inductance L can be calculated using the simple design rule (see Ref. 1),

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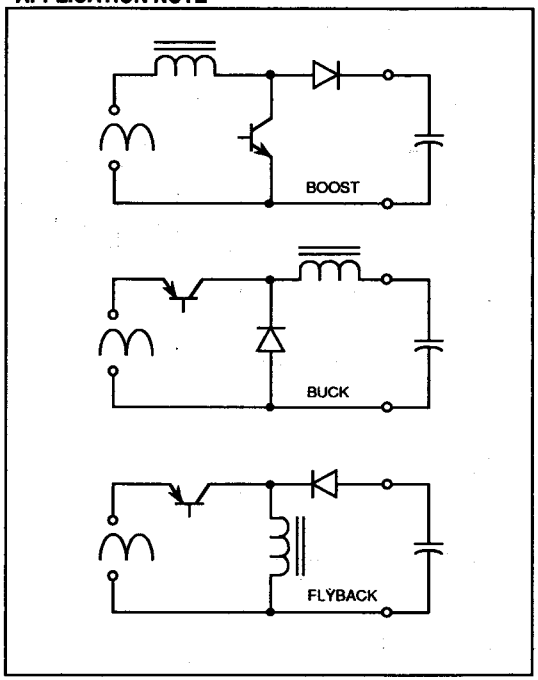

Figure 4. Basic converter topologies which can be used to implement the preregulator.

1) $$L = \frac{25{,}000}{f_s \cdot P_{in}}$$ henries.

where f is the PWM frequency, and Pin is the input power. For a 100Kz system, this simplifies to

2) $$L = \frac{0.25}{P_{in}}$$ henries.

This value of inductance will result in 20%p-p current ripple at the peak of the current waveform at full load and low line. Thus, if the peak value of current at low line is 5A, the maximum instantaneous current will be only 5.5A. At high line and low load, operation will become discontinuous, but with average current sensing, accuracy is preserved even if the percentage ripple is higher.

The bulk capacitor value C_o is often calculated in terms of the energy that must be supplied by the capacitor during a line dropout. If the output voltage is to drop from V_o to not less than V_{min} during the dropout period t_d, then

3) $$P_o \cdot t_d = 0.5 \cdot C_o \cdot (V_o^2 \cdot V_{min}^2)$$ joules.

If V_o = 380V, 1μF/watt will provide holdup to 335 volts for 20ms, and 2μF/watt will hold 363V for 20ms, or to 335V for 40ms. With the larger capacitor there will be less voltage ripple (second harmonic) present at the output, making it easier to achieve the desired low power factor with low distortion. Where low line current distortion is the overriding requirement, the capacitor size must be determined on that basis. The current that the boost stage delivers to the capacitor and load has an average value equal to the DC load current I_o, plus a single-frequency alternating component at 120Hz. The peak value of this AC component is equal to I_o, since the current swings from zero to $2I_o$. As this current flows through the capacitor only, we can calculate the ripple voltage V_{or} for a given capacitor C_o:

4) $$V_{or} = \frac{P_o}{2\pi \cdot 120 \cdot V_o \cdot C_o}$$ volts peak

where P_o is the output power and V_o is the output DC voltage. The effect of this ripple on the line current distortion is discussed in Section (K) below.

Gain of the Power Stage

The gain G_b of the boost stage is the incremental change in line current that results from an incremental change in duty cycle. Since the input current is equal to the 100KHz averaged inductor current in the continuous mode, and since the effect of duty cycle on the voltage appearing across the inductor is directly proportional to the output voltage V_o, it follows that

5) $$G_b = \frac{V_o}{sL}$$ amperes

where s is $(j \cdot 2\pi \cdot f_s)$, and f_s is the PWM frequency.

Inside and Around the UC3854

Refer to Fig. 8 for this section. Here we will discuss each of the various functions incorporated in the device, and explain its function and setup procedure. All values given are typical, unless otherwise indicated. Also, the component symbols used in this section correspond to those of Fig. 8.

(A) V_{CC} Supply, Pin 15: The recommended supply voltage to the chip is between 18V and 30V. Note that on power-up, the device does not become active until V_{CC} reaches 16V (provided that the enable input ENA is high). The current drawn before the turn-on threshold is reached will not exceed 2mA. At turn-on, this current increases to 10mA (20mA max) and

remains fairly constant thereafter. The V_{CC} turn-off threshold is set at 10V. These values permit the use of a simple and inexpensive V_{CC} supply.

(B) ENA, Pin 10: If the ENABLE input is low, the UC3854 will remain inactive even if V_{CC} is above 16V. This TTL compatible input provides an ideal on/off switch for the preregulator. Note that the REFERENCE voltage turns off when this input is low.

(C) R_{set}, Pin 12: The value of R_{set} determines the maximum value of PWM controlled line current by setting the peak current that the multiplier can deliver. If we denote the multiplier output current by I_m,

$$6) \qquad I_m\,(max) = \frac{-3.75}{R_{set}} \quad \text{amperes}$$

The negative sign indicates that this current flows out of Pin 5. If a resistor R_2 is placed between Pin 5 and the current sense resistor R_S, the peak line current will be limited to

$$7) \qquad I_i\,(max) = \frac{3.75 \cdot R_2}{R_{set} \cdot R_S} \quad \text{amperes}$$

(D) C_t, Pin 14: The capacitor C_t, together with resistor R_{set}, determines the PWM frequency:

$$8) \qquad f_S = \frac{1.25}{C_t \cdot R_{set}} \quad \text{hertz}$$

The saw-tooth waveform generated by the oscillator has a linear, positive slope, with an amplitude of 5.5Vp-p. The maximum usable frequency is in excess of 200KHz.

(E) REF, Pin 9: The enabled chip delivers a precise voltage V_{ref} of 7.5 volts at Pin 9, capable of -10mA with excellent regulation, and current-limited to -30mA.

(F) GT DRV, Pin 16: This output can drive a power MOSFET gate with an instantaneous peak current of 1A, allowing switching times of less than 100ns. Peak output voltage is internally limited to 16V. A peak current limiting resistor of about 20 ohms is recommended in series with the MOSFET gate. Note also that a maximum duty-cycle of 97% is specified.

The output duty cycle varies over its full range as the current amplifier output changes by 5.5V, which is the sawtooth peak-to-peak voltage. It follows that we can include the internal PWM control gain as part of the power stage gain G_b. To do this, we combine equation 5 above with the chip's PWM gain and get

$$9) \qquad G_{pwm} = \frac{V_o}{5.5 \cdot sL} \quad \text{siemens, or}$$

$$10) \qquad G_{pwm} = \frac{R_S\ V_o}{5.5 \cdot sL} \quad \text{volts per volt.}$$

Equation 10 gives the overall PWM/boost power stage gain in terms of the small signal voltage across the current sense resistor Rs divided by the small signal voltage at the current amplifier output, Pin 3.

(G) I SENSE, Pins 3, 4, and 5: The voltage across the current sense resistor R_S is applied to Pins 4 and 5, the input terminals of the current amplifier, with two equal resistors R_2 and R_3 (see Eq. 7). For average current sensing, the feedback components required between Pins 3 and 5 are as shown in Fig. 5. This amplifier's response is also shown in the figure, with the critical points labeled. Note that the phase response deviates from -90 degrees in the vicinity of the zero and pole, reaching a value of only -35 degrees if the two break points are separated by a factor of ten ($p = 10 \cdot z$). This fact will be important later, when we combine this amplifier with the power stage in a closed loop (see Eq. 10 above) because the boost converter introduces an additional phase lag of 90 degrees.

(H) MULTIPLIER and SQUARER, Pins 5, 6, 7, and 8: These blocks compute the quantity

$$11) \qquad I_m = \frac{K_m \cdot (V_a - 1) \cdot I_{ac}}{V_{rms}^2} \quad \text{amperes}$$

where I_m is the current IMULTOUT,
K_m is the multiplier constant,
V_a is the voltage amplifier output,
I_{ac} is the current into Pin 6,
V_{rms} is the voltage at Pin 8.

The voltage VAOUT directly controls power. The range of control is from 1V (zero power) to 5.6V (peak power). If we pick the value 5V to correspond to the maximum power required in a given design, we will have a sufficient margin above that value before limiting occurs. Thus, we can select values for V_{ac} and V_{rms} such that at low line voltage and full load the voltage V_a will be 5V. For the line voltage range from 75V to 275V, the setup shown in Fig. 8 will give very good results.

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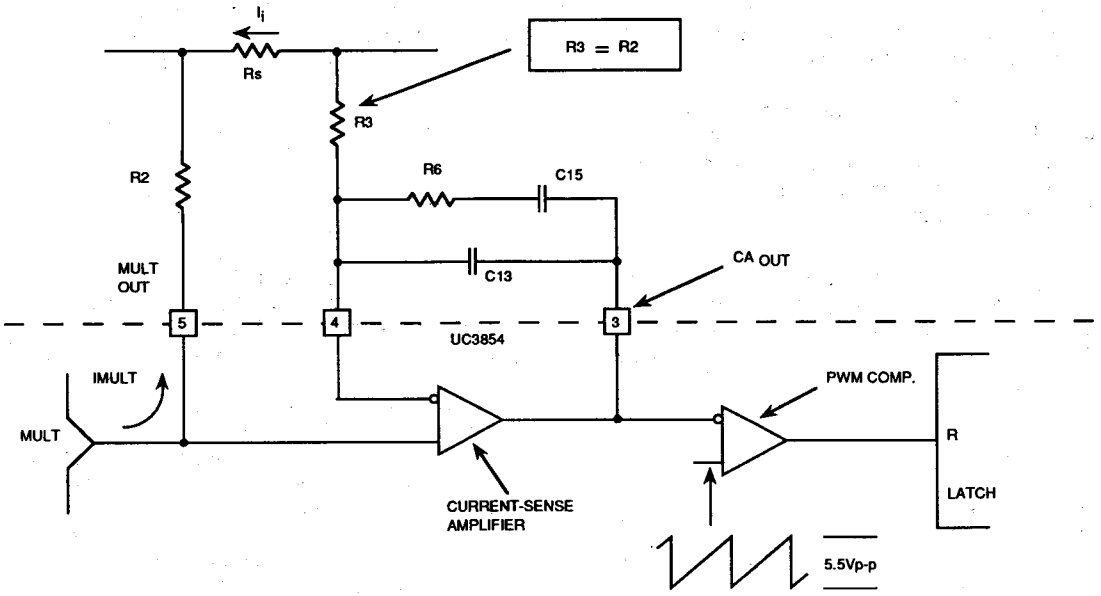

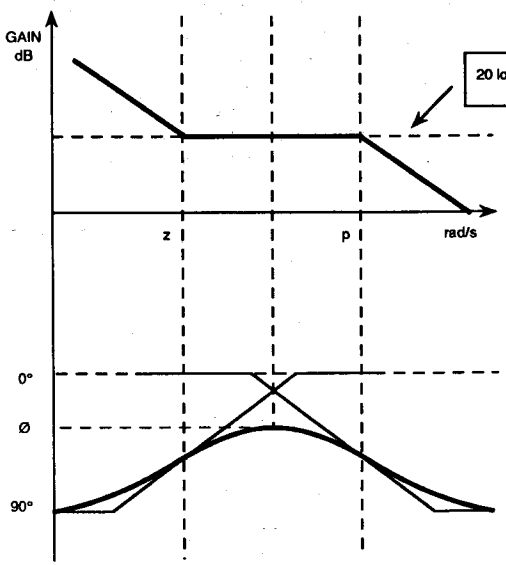

$$z = \frac{1}{R_6 C_{15}}$$

$$p = \frac{1}{R_6 C} \cdot C = \frac{C_{13} C_{15}}{C_{13} + C_{15}}$$

If $\frac{p}{z} = 10$,

$$\phi \approx -35° \text{ @ } \omega = \sqrt{zp}$$

Figure 5A. Current-sense amplifier compensation. By setting the pole p at a frequency ten times higher than z, you can reduce the phase lag to -35° at the geometrical midpoint.

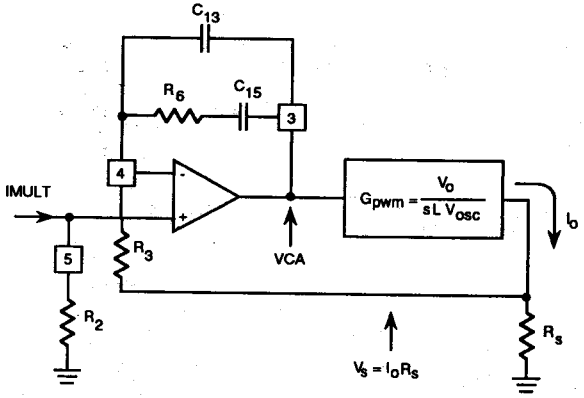

Figure 5B. Current control loop. The open-loop gain G_{CLO} is:

$$G_{CLO} = \frac{V_o R_s}{L V_{osc} R_6 C_{15}} \cdot \left[\frac{(s+z)}{s^2(s+p)}\right]$$

where $z = \frac{1}{R_6 C_{15}}$ (rad/s)

$$p = \frac{C_{13} + C_{15}}{R_6 C_{13} C_{15}} \text{ (rad/s)}$$

The constant K_m is the multiplier constant, approximately equal to -1, the negative sign indicating that the current I_m flows out of Pin 5. The voltage V_m that appears at Pin 5 depends on the value of R_2. (See above).

(I) I_{ac}, Pin 6: This current supplies to the UC3854 a sample of the rectified line waveform, which is needed to shape the line current. The output of the power rectifier supplies this small current through a large-value resistor, R_8. But because there is a potential of 6V present at Pin 6, and the full-wave rectified signal swings all the way to zero volts, a compensating resistor, R_{11}, is needed from Pin 6 to Pin 9, the REF output:

12) $R_{11} = 0.25 \cdot R_8$ ohms.

I_{ac} should be in the range from zero to 1mA. Therefore, for line voltages that can be as high as $275V_{rms}$, R_8 should be 500K or greater.

(J) VRMS, Pin 8: Ideally, this should be a DC voltage proportional to the rms value of the line voltage. Since the line waveshape does not change significantly, the average value will do just as well, and a good circuit for the purpose is shown in Fig. 6. This two-pole filter gives excellent attenuation of the various harmonics present, without introducing

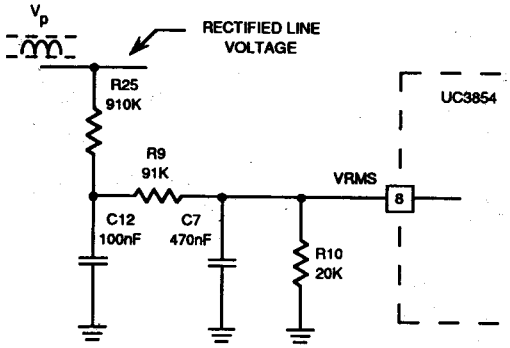

Figure 6. Two-pole filter for the V_{rms} input has a response of -34dB at DC, -67dB at 120Hz, and -79dB at 240Hz.

excessive delay in the DC output. This results in low output distortion and good transient response. The voltage applied to Pin 8 should be kept in the range from 1V to 5V. The values given in the circuit will meet this requirement for an input range from 75Vrms to 275Vrms.

Note that for each 1% of second harmonic ripple at Pin 8 there will be a contribution of 1% to the third harmonic content of the line current. This effect is

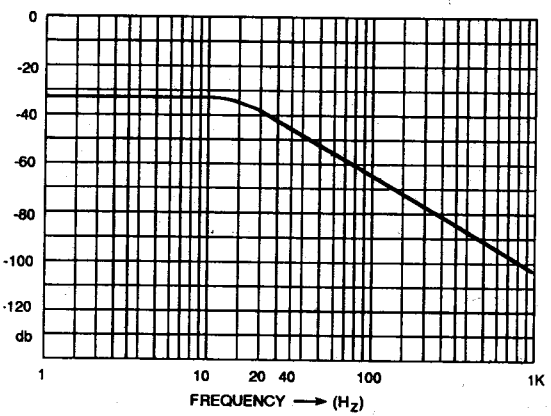

Figure 6A. Frequency response of the 2-pole RC filter of Figure 6.

additive with the contribution due to second harmonic ripple in Vo discussed below,

K) V SENSE, Pins 7 and 11: Except during soft-start, the non-inverting input to the voltage error amplifier is internally biased at 7.5V. The 50nA input bias current makes it possible to use high value resistors in the required biasing network, a valuable feature in view of the high voltages involved.

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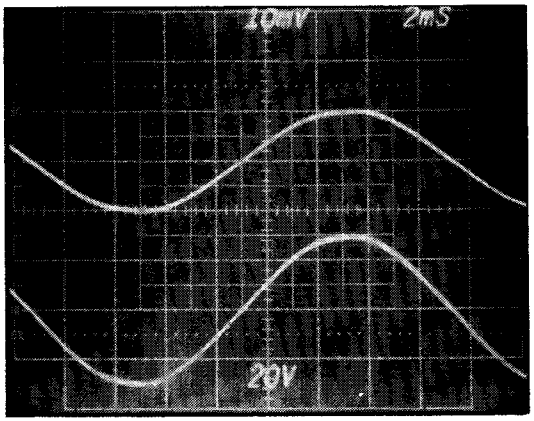
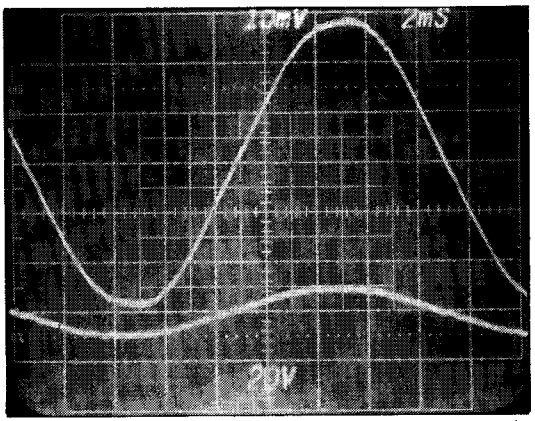


Top Trace: Line Voltage, $85V_{rms}$.
Bottom Trace: Line current, 2A per division.



Top Trace: Line Voltage, $250V_{rms}$.
Bottom Trace: Line current, 2A per division.

Figure 9. Line voltage and current waveforms obtained with the circuit of Figure 8.

(L) PK LIM, Pin 2: This comparator has an input threshold of zero volts. If its input (Pin 2) is driven below ground, the comparator instantly stops the PWM action, with the PWM drive (Pin 16) held low. The components R_4 and R_5 (1.6K and 10K respectively), shown in the complete schematic of Fig. 8, will provide peak limiting at about 4.8A. Capacitor C_3 can be added for noise filtering.

(M) SS (Soft Start), Pin 13: It has already been mentioned that in a circuit utilizing the boost topology, the output voltage cannot be less than the peak line voltage. In such a system, the soft start feature can only be effective in the output voltage range above that value. It is mainly with buck and flyback converter applications that the SS feature becomes fully operational.

POWERING THE UC3854

The UC3854 can be powered with a simple circuit such as the one shown in Fig. 8. Start-up power is supplied through resistor R_{22} and transistor Q_2. Since the maximum start-up current is only 2mA, the power dissipated in the resistor is only about 2.6 watts. After start-up, the secondary winding on the boost inductor begins to transfer energy through the full-wave rectifier bridge D_6, to supply the 20mA maximum current needed to sustain operation.

A 250W APPLICATION

Fig. 8 shows the complete diagram of a high efficiency power supply capable of delivering 250 watts with a power factor in excess of 0.999 and less than 3% harmonic distortion. The input current is limited at approximately 4A, which means that the inductor L_1 must be designed to handle that current. The rectifier D_2 must have very short recovery time rating to handle the high PWM frequency of 100KHz. Note the Schottky diode added from Pin 16 to ground, a precaution that is sometimes necessary to prevent conduction in the chip's substrate diode. Inrush current protection is included by the addition of a thermistor in series with the power line. See Fig. 9 for voltage and current waveforms obtained with the circuit of Fig. 8.

REFERENCES:

(1) Lloyd Dixon, Jr. , "High Power Factor Preregulators for Off-Line Power Supplies", Unitrode Power Supply Seminar Handbook, SEM-600A, 1988.

(2) R. Mammano and R. Neidorff, "Improving Input Power Factor - A New Active Controller Simplifies the Task", Proceedings of the 19th International PCIM Conference, 1989.

(3) Unitrode Power Supply Seminar Handbook for 1990, (in preparation).

The amplifier can be set up to operate at full DC gain, if tight regulation of the output voltage is desired, but at the cost of somewhat slower dynamics (recovery from sudden input voltage or load changes). For the intended application of the

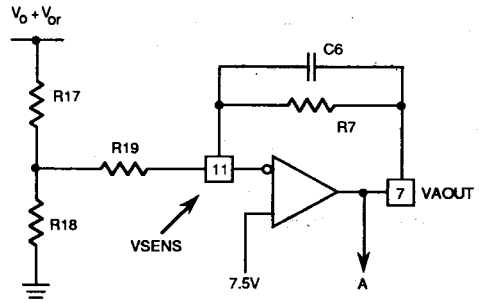


Figure 7. Voltage sensing circuit. The output voltage at Pin 7 is limited to the range from 1V at no load, to 5.6V at full load.

UC3854 as a preregulator, with high power factor as the primary concern, it is best to configure this section as shown in Fig. 7.

The transfer function of the voltage amplifier feedback circuit must be carefully suited to the characteristics of the remaining components of the feedback loop if the given distortion specifications and loop dynamics requirements are to be met. The amount of distortion in the line current depends on the amount of second harmonic ripple introduced into the multiplier by the Vrms signal and by the error amplifier output. The latter's contribution amounts to 0.5% third harmonic distortion in line current for each 1% second harmonic present at Pin 7, calculated in terms of the nominal 4V voltage swing at Pin 7 with $K_m = -1$.

This allows us to calculate the maximum ripple voltage that can be tolerated at Pin 7, as in the following example.

EXAMPLE:

Assume $P_O = 250W$, $V_O = 385V$; then $I_O = 0.625A$.

The 100KHz average current delivered through the boost rectifier to the capacitor and load has a frequency of 120Hz, and an average value of 0.625A at full power. It swings between zero and 1.25A, and we can calculate the ripple voltage V_{or} present in the capacitor voltage V_O:

a) $$V_{or} = \frac{0.625}{2\pi \cdot 120 \cdot C_O} \quad \text{volts peak}$$

Assuming that C_O was chosen at about 2μF per watt (see above), we have,

$C_O = 450\mu F$, and
$V_{or} = 1.84Vpk$.

Vo is attenuated from 385V to 7.5V, the amplifier's reference voltage, by divider R_{17} and R_{18}: V_{or} will necessarily be reduced by the same factor:

b) $$V_{or} = \frac{1.84 \cdot 7.5}{385} = 0.036V$$

With the multiplier set up properly, a 4V change (from 1V to 5V) in the voltage amplifier output changes the line current from zero to full load. A ripple voltage V_{or} at the amplifier's output, equal to 2.5% of 4V (0.1V), will contribute 1.25% third harmonic distortion to the line current. Then, the product $R_{19} \cdot C_6$ must be such that with an input of 0.036V at 120Hz, the output is 0.1V. In other words, the gain at 120Hz must be;

c) $G_{120} = \frac{0.1}{0.036} = 2.8$ V/V @ 120Hz, with $K_m = -1$.

NOTE: A few advance samples of the UC3854, manufactured in 1989, had a K_m value of about -6. Those devices required a gain G_{120} equal to 1/6 the value calculated above.
The integrator constant is:

13) $$R_{19} \cdot C_6 = \frac{1}{2\pi \cdot 120 \cdot G_{120}} \text{ seconds, or}$$

d) $$R_{19} \cdot C_6 = \frac{1}{2\pi \cdot 120 \cdot 2.8} = 470\mu s.$$

The reciprocal of the integrator constant $R_{19} \cdot C_6$ is the frequency (in rad/s) at which the gain is one. Any combination of values of R_{19} and C_6 whose product is equal to 370μs will provide the required gain of 3.2 at 120Hz.

Note that this result was determined based on distortion requirements alone, and that we have not yet considered R_7 which will have to be added in shunt with C_6. Without this resistor, the voltage feedback loop will surely be unstable, since there are two -90 degree contributions; one from the output capacitor, and another from the voltage amplifier

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(with R_{19} and C6 only). By adding the resistor R_7 to the feedback path, we can make sure that the net phase lag at unity gain crossover is at least 45 degrees less than 180, thus guaranteeing stability. For 45 degrees of phase margin, the best value for this resistor is that which will place a pole in the voltage control open loop response at the unity-gain frequency f_c, given by Eq. 14:

$$14)\quad f_c = \frac{1}{2\pi} \cdot \sqrt{\frac{P_o \cdot V_{ref}}{V_o^2 \cdot V_a \cdot C_o \cdot R_{19} \cdot C_6}} \quad \text{Hz}$$

P_o = output power, watts
V_{ref} = reference voltage
V_o = DC output voltage
V_a = output range of voltage amplifier, volts
C_o = bulk capacitor, farads

For P_o=250W, V_{ref}=7.5V, V_a=4V, V_o=400V, C_o =500µF, R_{19}=10K, and C_6=47nF (for $R_{19} \cdot C_6$=470µs), we get f_c = 20 Hz.

We can now find a value for R_7:

$$15)\quad R_7 = \frac{1}{2\pi \cdot f_c \cdot C_6} \quad \text{ohms.}$$

For the example above, R7=174K.

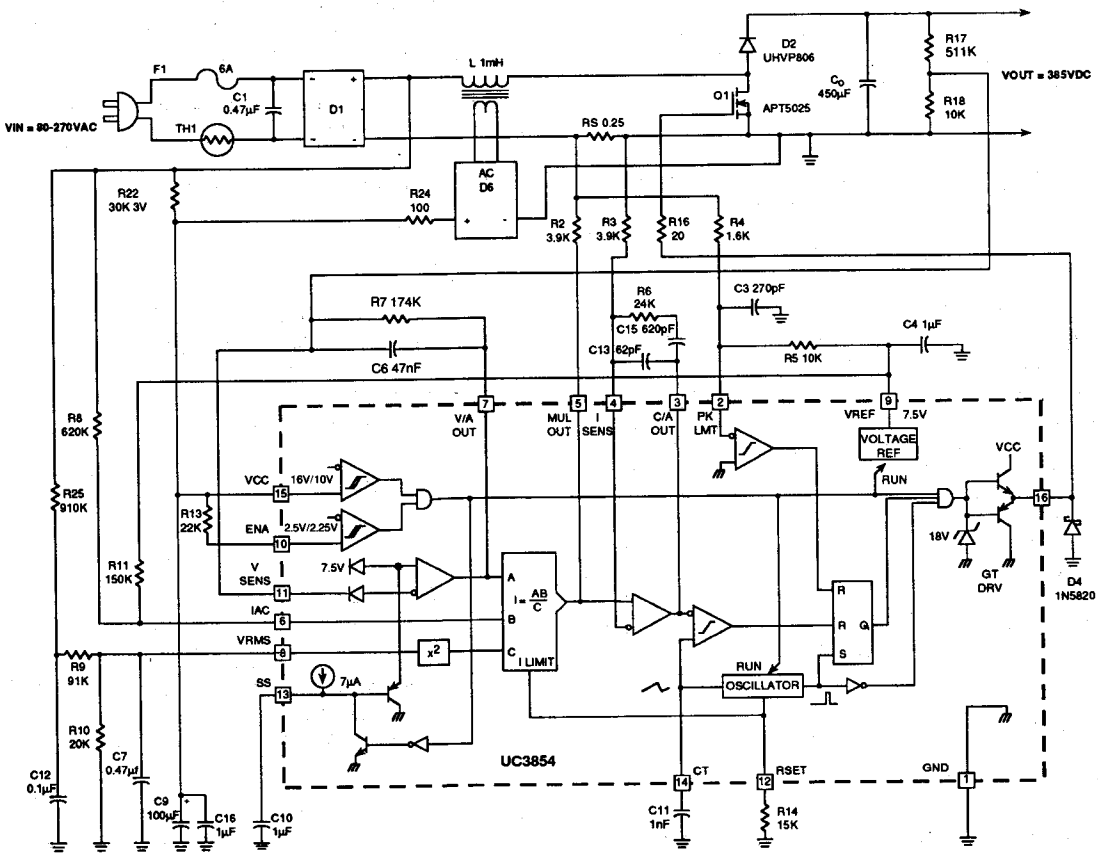

Figure 8. Complete schematic of 250W high power factor preregulator.