PFC Circuit Halts Inrush Currents

By John Bottrill, Senior Applications Engineer,
Texas Instruments, Manchester, N.H.

An alternative to passive overcurrent protection, this power-factor correction stage more accurately limits the inrush current at start-up and minimizes power dissipation.

The use of power-factor correction (PFC) is becoming more common in the design of power converters. Their use is now being mandated by some countries and will continue to expand as line power-carrying capabilities become more and more critical. Additionally, the new ENERGY STAR efficiency category of converters will push this topology. This will cause many engineers to try designing PFCs for the first time.

Powering up a converter that's plugged into a live ac line and uses a PFC front end brings with it design challenges. When power is first applied to a circuit, there is usually a large transient current surge that warrants careful considerations, particularly for first-time designers.

Most PFC circuits consist of a boost front end that takes the universal ac line voltage and transforms it into a higher dc voltage at the output of the PFC stage. From there it is down-converted to the voltages that are needed by the unit being powered.

The key power components of a boost converter before the activation of the PFC control are the series-connected PFC inductor L1, a diode and the PFC capacitor C1. The effects of the input filter can be ignored because they are insignificant as compared to L1 and C1.

In a 500-W system, L1 will be on the order of 1 mH, and C1 will be on the order of 400 µF. When power is first applied, the output capacitor is charged by current that flows through L1 into C1.

If the ac voltage being applied is at a zero crossing of the ac line voltage when the connection is made, the output capacitor will charge within a quarter cycle and not overshoot because the resonant frequency of the LC, defined as

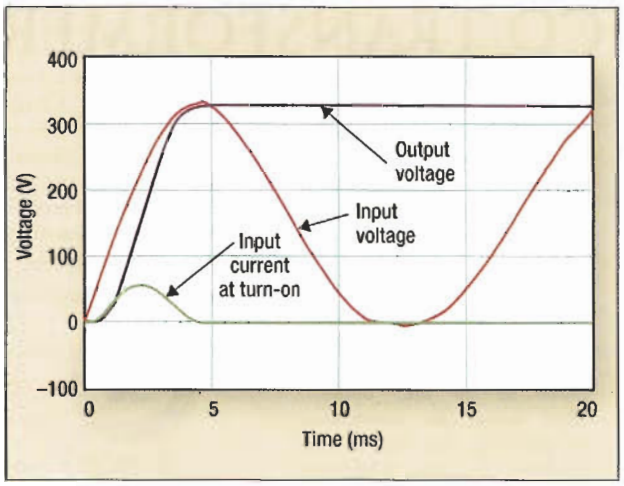


Fig. 1. *In a basic boost converter, the charging level of the converter's capacitor using a rectified 60-Hz sine wave is much lower than the resonant frequency of the converter's LC circuit.*

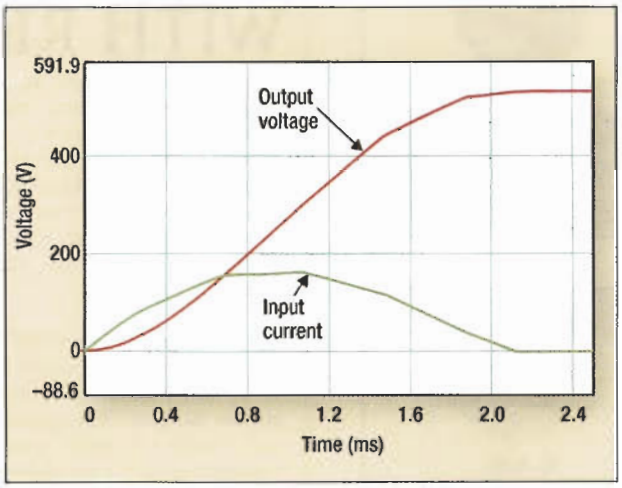


Fig. 2. *Because a basic boost converter is limited by the resonance of its LC combo, the output voltage will overshoot potentially twice the input voltage and the peak charge current will increase significantly.*

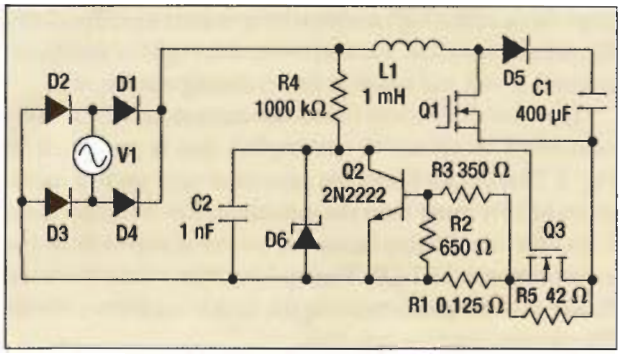


Fig. 3. *This circuit limits the inrush current at turn-on to a maximum of 10% more than the maximum ac line operation limit.*

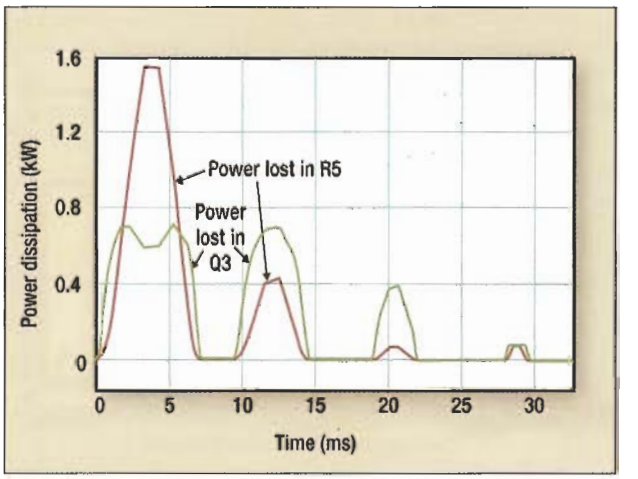


Fig. 4. *In this boost converter, 110% of the maximum allowable current is handled by resistor R5, if the voltage across it is equal to the maximum rectified input voltage.*

250 Hz, is significantly higher than the input line voltage, typically 50 Hz or 60 Hz. Charging the capacitor with a rectified 60-Hz sinewave is much lower than the resonant frequency of the LC (Fig. 1).

The peak current into the capacitor is approximately 55 A. This can create problems since the worst-case operating peak current is about 8 A.

Applying power at the zero crossing of the ac line voltage, however, is not the worst-case condition. If the input power is applied at a point where the input ac voltage is approaching the peak voltage, the output voltage will charge in much less than a half-cycle. Because it will now be limited to the resonance of the LC circuit, the output voltage will overshoot to a voltage that is potentially twice the input voltage, and the peak charge current will increase significantly (Fig. 2). The only limiting factors are parasitic elements such as the resistance of the inductor winding, the pc-board traces and the source impedance; however, these would not be enough to save components from failure.

The traditional method of preventing the voltage overshoot is to put a diode from the positive terminal of the input bridge rectifier to the positive terminal of the output capacitor. This will prevent any voltage overshoot of the output capacitor at turn-on. However, it does not prevent the overcurrent. In fact, it will increase the current spike. Though it is not shown here and is not required for start-up, with the PFC circuit that will be presented later in the article it does help stabilize the control for input-voltage transients.

The overcurrent is normally handled with either a positive temperature coefficient resistor (PTC) or a negative temperature coefficient resistor (NTC). A PTC is put in series with the input and limits the current while the output capacitor is initially charged. Once charged, an internal housekeeping power supply starts and operates a relay that shorts the PTC, at which point the PFC boost converter can be started. If there is a failure, the PTC's temperature increases and results in an increase in resistance, resulting in less current through the line.

The NTC starts with a high resistance, and as its tem-

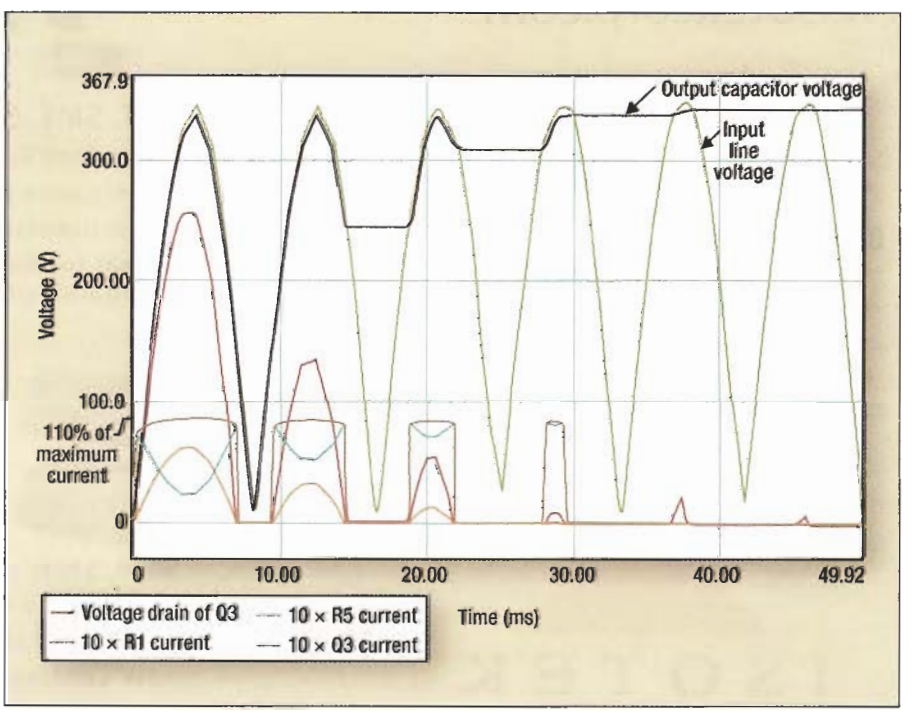


Fig. 5. *These plots for the boost converter in Fig. 4 show the current through resistor R5 and FET Q3, the total current through resistor R1, (scaled to a factor of 10 to fit this graph), the voltage across both resistor R5 and FET Q3, and the output capacitor voltage across C1.*

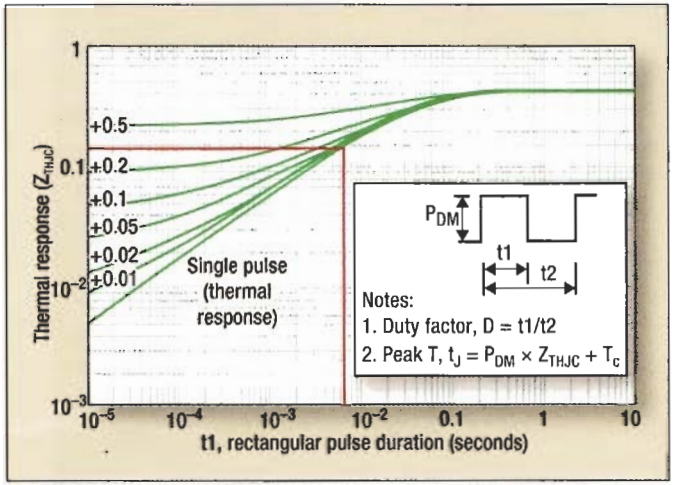


Fig. 6. *The maximum effective transient junction to case thermal impedance for the circuit in Fig. 4. Maximum current limiting (and thus less heating) can be obtained by a combination of adjusting the ratio of resistors R2 and R3 and increasing the value of resistor R1.*

perature increases, its resistance decreases. It is usually left in the circuit, so as long as it stays hot, the resistance stays low. Care must be taken to ensure that it gets hot enough to become insignificant even under light loads, but has enough impedance with a high ambient temperature to still perform the defined function. Furthermore, although the resistance is small, it will still result in losses during operation.

There are cases where the inrush current must be actively controlled. A circuit to accomplish this is presented in Fig. 3. This circuit limits the current at turn-on to a maximum of 10% more than the maximum low-line operation limit. The circuit also limits the power dissipation in the active element, FET Q3. Thermal junction calculations are shown to assist in determining the device needed to provide the current-limiting function.

This circuit safely limits the start-up inrush current to the maximum expected line current during operation. It prevents overshoot of the output upon power application.

A Closer Examination

The first thing the designer needs to realize is that the total energy stored in the output capacitor is the minimum energy that is going to be dissipated in the combination of Q3 and R5 of Fig. 3.

Resistor R5 is chosen first to have the 110% of the maximum allowable current through it, if the voltage across it is equal to the maximum rectified input voltage ($V_{IN_{MAX}}$). At the higher input voltages, R5 will be dissipating most of the energy each time the converter has power applied (Fig. 4).

If the resistor is sized to handle the energy ($0.5 \times C_{PFC} \times V_{IN_{MAX}}^2$) and the instantaneous voltage of $V_{IN_{MAX}}$, then one should have no problem with the turn-on. Since this is a one-of voltage pulse that will last only milliseconds, the requirements for the resistor are that it be capable of absorbing the energy pulse, that it can withstand the voltage and that there be no long-term need for thermal dissipation.

Next, R1, R2 and R3 are chosen. R1 is chosen so that the voltage across it is greater than the V_{BE} of Q2 at full load, but with very little margin. For these simulations, R1 was chosen to drop 1 V at 110% of the rated current. R2 was set to 650 Ω and R3 to 350 Ω so that at the maximum current, the base of transistor Q2 would be 0.65 V. Therefore, at 110% of the maximum load, the transistor Q2 would be turned on and start to pull down on the gate of Q3. As the voltage on Q3's gate is pulled down, Q3, which is in the active region, increases its impedance. This decreases the current flowing through it, limiting the current to the desired 110% limit.

This means that Q3 is dissipating power that will raise its junction temperature. As the voltage across the output capacitor increases, the voltage across Q3 and R5 will drop. This results in R5 carrying less current. Because of the active nature of the circuit, Q2 will carry more current, so that the total is 110% of the maximum load current (Fig. 5).

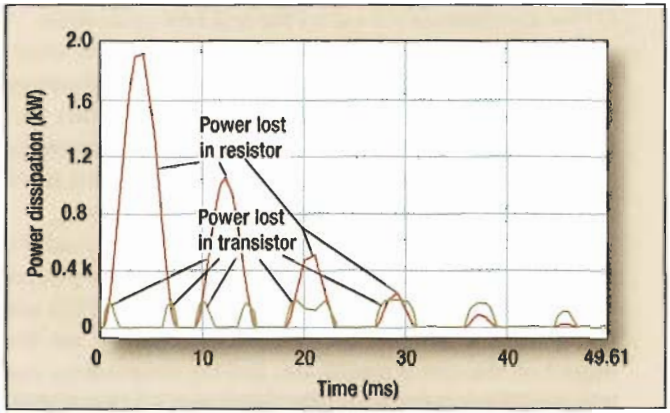


Fig. 7. *A combination of adjusting the ratio of resistors R2 and R3 and increasing the value of resistor R1, the circuit in Fig. 4 slows down the circuit's power-factor correction. It also causes resistor R5 to bear the brunt of lost power.*

Fig. 5 shows that the total current charging the capacitor is at the 110% level whenever the input voltage exceeds the voltage that is already stored on the capacitor. Fig. 4 adds the power lost in R5 and Q3 to the plot showing the power in each device.

As can be seen in Fig. 4, there is approximately 600 W of power being dissipated in the junction of the pass transistor

Q3 for approximately 7 ms on the first half-cycle alone.

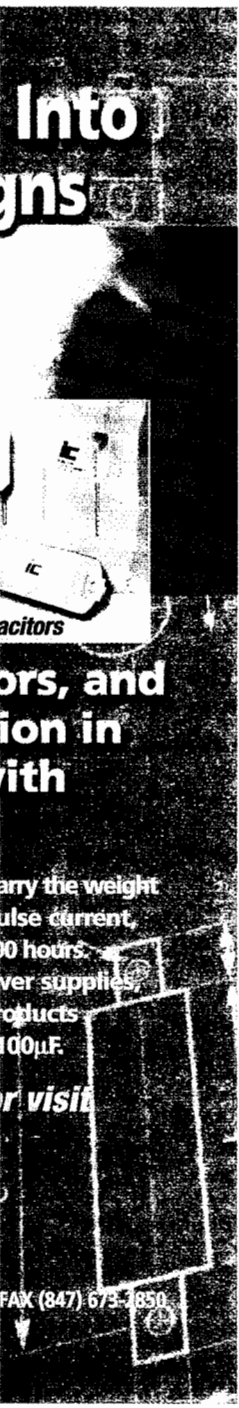
An IRFP450 FET is now examined for this application. The information needed is contained on the instantaneous thermal impedance graph (Fig. 6). The graph shows that for a pulse of 7 ms, the junction temperature increases by 0.15°C/W. This means that with the power predicted, there will be a 90°C temperature rise from the first pulse.

The second pulse has almost as much power. And the third one adds a significant contribution. This pushes the temperature well over 200°C. If two of the FETs are paralleled, the temperature rise drops in half — but the impact on the cost is significant, and the temperature rise

still might exceed the maximum junction temperature.

There are several options to prevent this level of heating. Limiting the current through the FET at higher voltages is the first and most obvious. This can be done by adjusting the ratio of R2 and R3, and by increasing the value of R1. Each of these has the desired effect of lowering the power in the FET's junction by combining both results for better overall performance.

By changing R1 to 0.175 Ω, R2 to 1 kΩ and R3 to 100 Ω, the energy lost in the first half-cycle of the line input current is spread over two pulses — each approximately 2 ms in duration and peaking at about 170 W. This averages out at (0.5 × 170 W × 2 ms) × 2 over 8.33 ms, or 40 W average over 8.33 ms for a temperature rise of 6°C for the first pulse, compared to 90°C in the previous condition.



The second pulse has the same additional power as the first pulse. The power in the subsequent pulses is higher as follows: the third at 90 W, the fourth at 91 W, the fifth at 61 W and the sixth at 26 W. This total power added and averaged over the start-up cycle results in a temperature rise at the junction of 105°C.

Remember, this power is for the full charge of the capacitor — not just the first half-cycle of the sine wave, so it looks like the junction is at a higher temperature than in Fig. 5 where it went up 90°C in the first 8 ms. This is still going to stress the FET. Thus, the resistance of R1 probably should be increased further to get the temperature down further. This will depend on the program derating requirements and ambient temperature conditions.

Nothing is free, and the downside of this is that the time to charge the PFC capacitor to the maximum line voltage is changed from 40 ms to 60 ms. Moreover, resistor R5 will have to absorb the additional power. This power loss is shown in Fig. 7.

The bottom line is that care must be exercised when selecting the resistor, because the instantaneous power is as significant as the voltage across it. It will probably be better if two or three resistors are used in series.

Once the PFC starts, this circuit can either be shorted out by a relay circuit or by another FET that is put across Q3 and R1. **PETech**