FAIRCHILD SEMICONDUCTOR™

Application Note 42045

ML4824, A Novel Method for an Off-Line PFC-PWM Combo Controller

INTRODUCTION

One of the most undesirable phenomena experienced by utility companies is the high harmonic content of the line current. The harmonic content of this line current tends to cause transformer overheating at the substations, which are responsible for providing power to all sectors of a given area. For three-phase distribution, neutral currents will flow in the presence of these harmonics. For single-phase distribution, the narrow conduction angle demanded by capacitive input filters in switching power converters causes high harmonic content in the current waveform, resulting in lower operating efficiency.

A viable solution to this problem is the inclusion of a power factor correction (PFC) stage to facilitate more efficient power usage as well as lowering the harmonic content of the line current. The most popular topology for this task is the switched-mode boost converter. Here the boost converter stage is inserted between the input rectifier and the bulk storage capacitor. This forces the input current to be in phase with the input voltage and provides a boosted D.C. voltage reservoir for the following power stage.

In many instances the power supply system must interface to a wide range input voltage (80-264V) requiring the boosted voltage be equal to or greater than 380VDC. For safe operation a capacitor with a voltage rating of at least 400V is necessary. Traditional cascaded power stages require large bulk capacitance values with low ESR to minimize peak to peak ripple voltage and lower self heating. Together these requirements result in a costly capacitor.

To understand why the bulk capacitor requirements are traditionally so stringent consider the circuit shown in Figure 1, a PFC power stage with resistive load. The bulk capacitor C1 must supply load current I0 when VSW is on, storing energy in the boost inductor L1. It must also "absorb" the peak current from L1 each time VSW switches off. The result of these currents into and out of C1 is a large ripple voltage across it. It is this large current with steep wavefronts that place the high demand on C1's bulk capacitance and ESR values to minimize output ripple.

Next, consider Figures 2 and 3, a PFC stage followed by an "unsynchronized" PWM stage. (Note 1: In this note the terms "unsynchronized" and "synchronized" are used to describe the switching action of 2 power switches operating from the same system clock. The switches are "synchronized" when one of them (SW2) turns on when the other (SW1) turns off. They are "unsynchronized" when both are switched on at the same time.) Here SW1 and SW2 are switched on and off at the same time. The peak currents and therefore the ripple voltage are less than a PFC stage with a resistive load. Even further reductions are possible by "synchronizing" the 2 stages (Figures 4 and 5).

Micro Linear's ML4824 Combo Controller IC is an integrated solution for systems benefitting from the advantages made possible by synchronizing the 2 cascaded power stages. In this application note the differences between the traditional combo modulation scheme (unsynchronized or trailing edge modulation) and the ML4824's leading/trailing edge modulation scheme are explained. A typical application is shown and test results are compared with the traditional approach. Then, a detailed look is taken inside the ML4824 and key design formulas are reviewed which will enable users to begin their own design.

CASCADE POWER CONVERTER

The cascade connection of power stages is a very effective and powerful tool in the design of state-of-the-art high frequency switch mode power converters (1). In recent years, power factor corrected power converters are rapidly gaining popularity. They offer improved performance when compared to traditional off-line switching power converters. However, special system stability considerations must be made.

Traditional trailing edge modulation results in a momentary no-load condition when the buck switch is turned off. This condition makes loop compensation difficult as it results in 2 poles located close to the RHPZ (Right Half Plane Zero) already in play because the boost inductor operates in continuous conduction current mode. Synchronous switching techniques as employed in the ML4824 push these poles further out in frequency allowing unity gain crossover to be placed at as high as one-half the line frequency.

For example, consider a single power stage boost converter as shown in Figure 1. The load of this stage is connected to the output filter and its value affects the loop response of the converter. When the load is reduced, the poles due to the inductor and the capacitor become closer and the phase margin is reduced.

In the cascade power stage, the load could be momentarily connected or disconnected. (See Figure 2 for a boost-buck cascade stage.) Many systems attempt to reduce the no load period by speeding up the loop response for the second stage and hence, a second (usually faster) clock has to be used resulting in a more complicated system.

TRAILING EDGE MODULATION AND LEADING EDGE MODULATION

Conventional pulse width modulation (PWM) employs trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. Then the error amplifier output voltage is compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 3 shows a typical trailing edge control scheme.

In the case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock; when the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during the OFF time of the switch. Figure 4 shows a leading edge control scheme.

THE OUTPUT VOLTAGE RIPPLE OF THE PFC STAGE

If the boost-buck cascade power converter of Figure 2 is applied to the off-line PFC/PWM power converter, the output ripple voltage of the PFC stage can be separated into two portions. One portion is due to the voltage drop across the C1's ESR. The other is due to dv/dt of C1. Assuming both converters are in the Continuous Conduction Mode (CCM), and conventional trailing edge modulation without synchronous switching is used, the ripple voltage is

$$\text{Total Ripple Voltage} = I_{2MAX} \times ESR + \frac{0.433 \times I_{2MAX}}{C_1 \times f_{PFC}} \quad (1)$$

$$I_{2MAX} = \frac{\text{Average Input Power} \times \sqrt{2}}{\text{Efficiency} \times V_{INRMS}} \quad (2)$$

If the dv/dt ripple voltage is dominant, dv reaches maximum when the phase of the input voltage waveform is at 60° or 120°.

One of the advantages of the new control scheme is that it requires only one system clock. Switch 1 (SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary no load period, thus lowering ripple voltage generated by the switching action. With synchronous switching, the ripple voltage of the first stage is reduced. Figure 5 shows the boost-buck cascade power

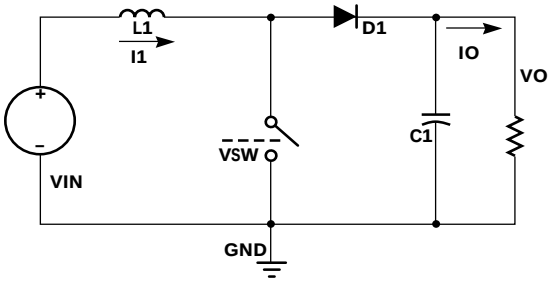


Figure 1. A Single Boost Power Stage with a Load.

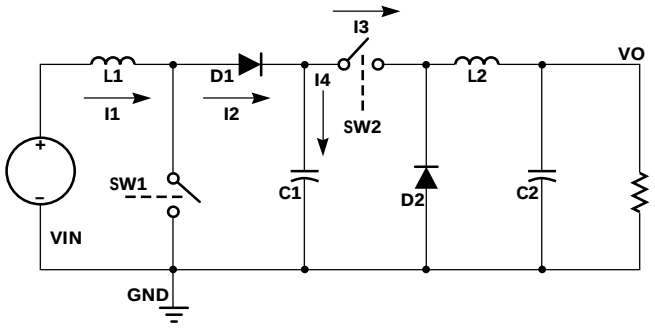


Figure 2. A Cascade Boost-Buck Power Converter without Synchronous Switching.

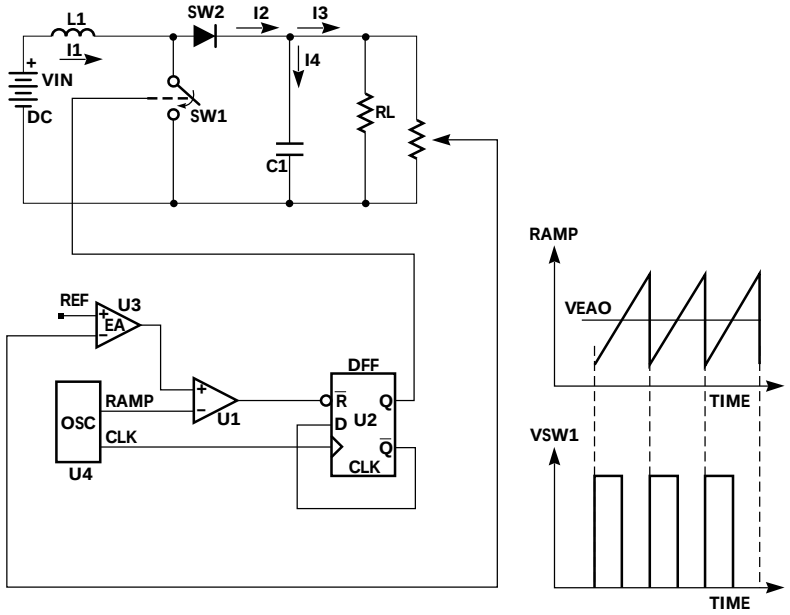


Figure 3. Trailing Edge Modulation Control Scheme.

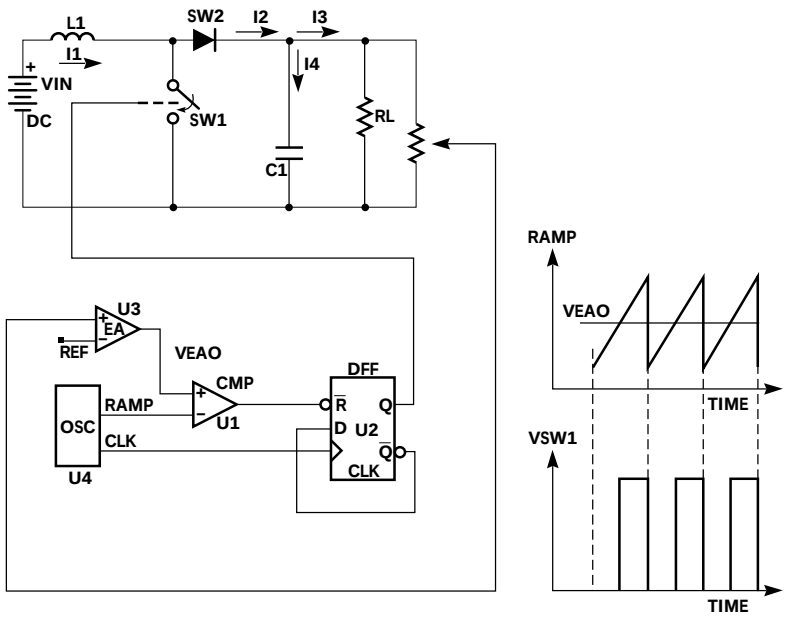


Figure 4. Leading/Trailing Edge Modulation Control Scheme.

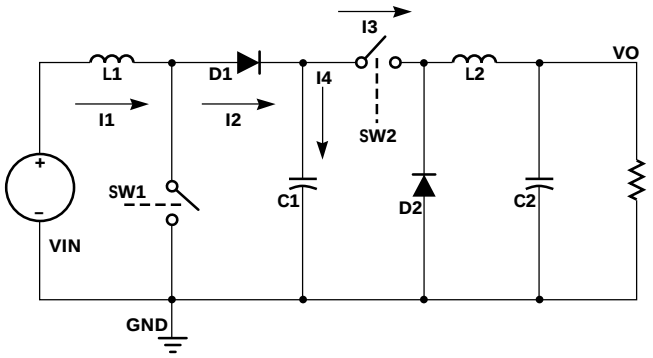


Figure 5. Synchronous Switching Cascade Power Converter.

converter with synchronous switching which differs from Figure 2 only in the switching sequence. The ripple voltage of Figure 5 is

$$\text{Total Ripple Voltage} = \left(I_{2MAX} - I_3\right) \times ESR + \frac{0.433 \times \left(I_{2MAX} - I_3\right)}{C_1 \times f_{PFC}} \qquad (3)$$

SYNCHRONOUS SWITCHING IN OFF-LINE PFC-PWM CASCADE POWER CONVERTER

A 200W off-line PFC/PWM cascade converter has been evaluated. Figure 6 shows the schematic of the 200W off-line PFC PWM cascade converter. The results show that the 120Hz component of the output ripple voltage has been reduced by 30%.

EXPERIMENTAL RESULTS

By virtue of the leading edge modulation PFC stage, working together with the trailing edge modulation PWM stage the system performance is enhanced. A comparison was made between the ML4824 and the ML4819 which employs trailing edge modulation for both power stages. The ML4819 is designed to function as a peak current controller with current mode PWM for the output stage. The test conditions are

C_{DC} = 50µF, V_{IN} = 220V A.C.,

Average Input Power = 75W,

f_{PFC} = 80KHz, and L_{PFC} = 1.5mH

See Figure 7.

APPLICATION CIRCUIT

POWER FACTOR SECTION

The function of the power factor correction section is to ensure the current follows the voltage in time and amplitude proportionally. This means that, for steady-state constant output power conditions, the current amplitude will follow the voltage amplitude in the same proportion at any instant in time. When the voltage amplitude is at 100%, current amplitude will be maximum. When the voltage is at 50% amplitude, the current amplitude will be at half its maximum value.

The result is a sinusoidal current waveform in phase with the incoming sinusoidal voltage waveform.

The power factor correction section is comprised of a boost type power stage with primary side of inductor T_1 as the input inductor. The secondary side is used as an auxiliary voltage source for powering the control circuit.

Since this stage is concerned with current processing, and the frequency of the current is related to the line frequency, the voltage control loop for this section is forced to have a slow response to allow the current to follow the voltage. This slow voltage loop response necessitates the addition of another power stage for faster and more accurate voltage processing.

The power factor correction section derives its timing from the same oscillator as the pulse width modulation section. This section has its own current limit comparator for current mode control. A comparator is also used for supplying overvoltage protection commands.

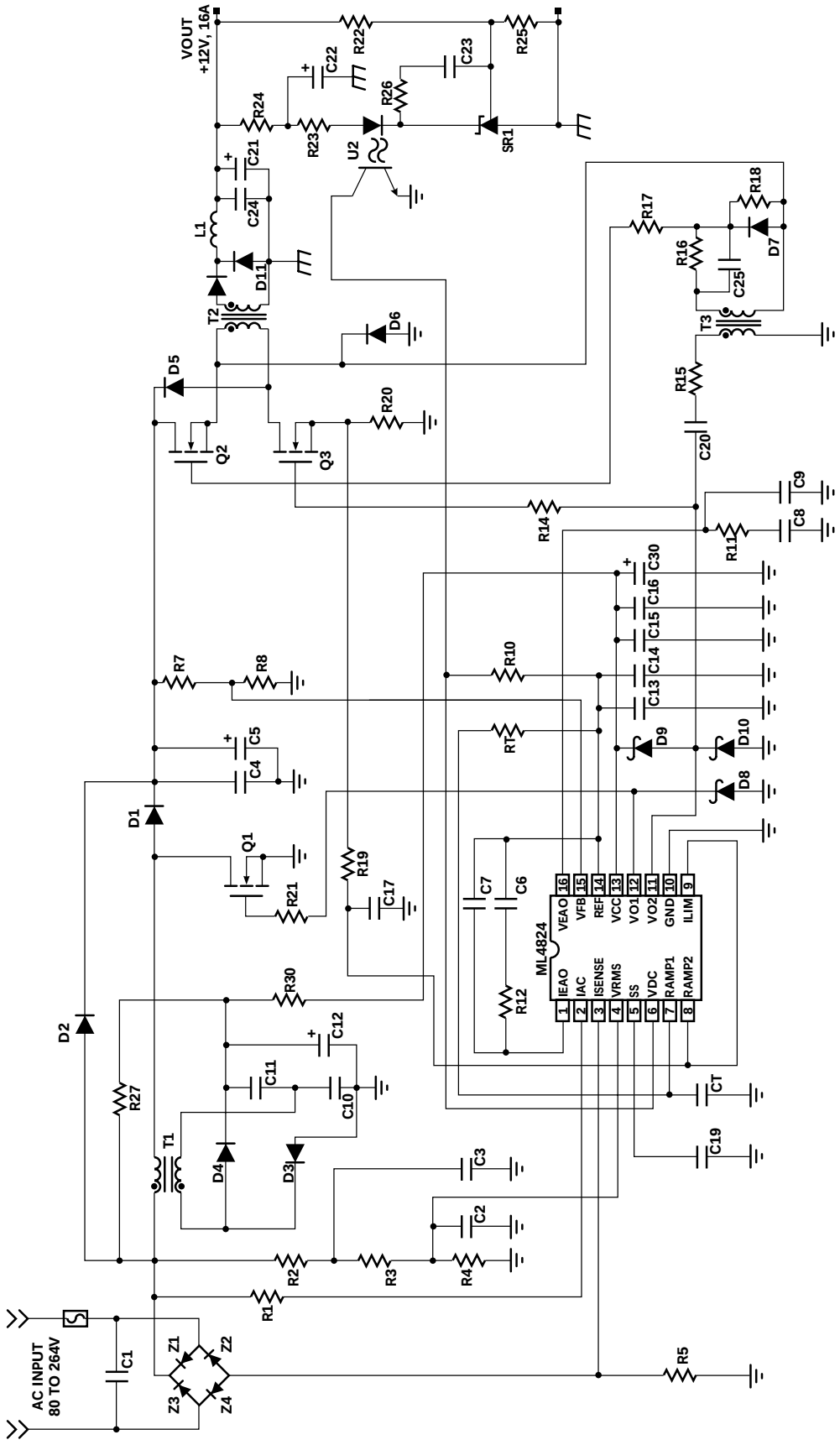
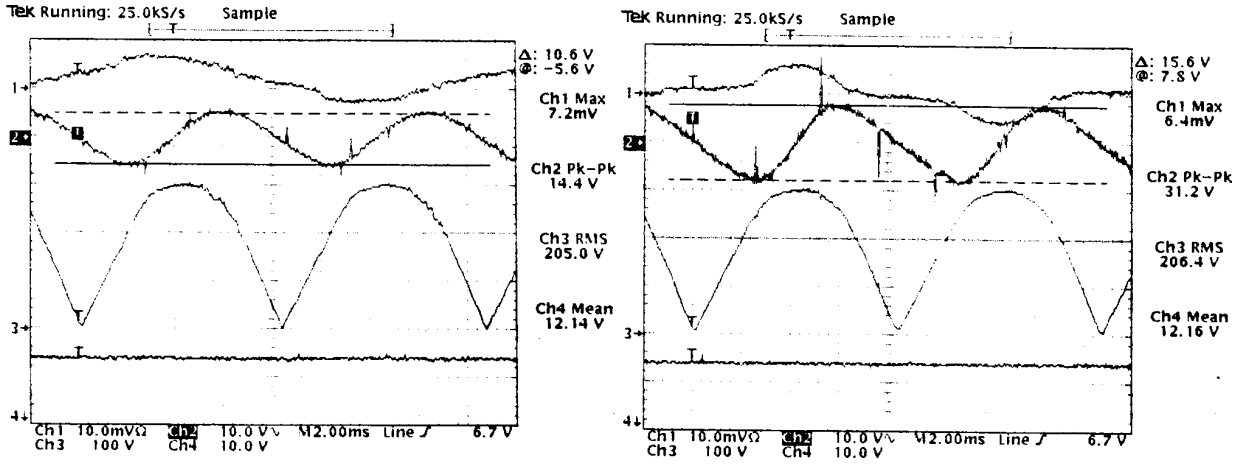


Figure 6. A 200W Off-Line PFC/PWM Power Converter with Synchronous Switching.



(7a) ML4824 Test Results

(7b) ML4819 Test Results

Figure 7. Comparison of Leading/Trailing Edge Modulation (Fig. 7a) to Trailing Edge Modulation only (Fig. 7b). (Middle traces are output ripple voltage.)

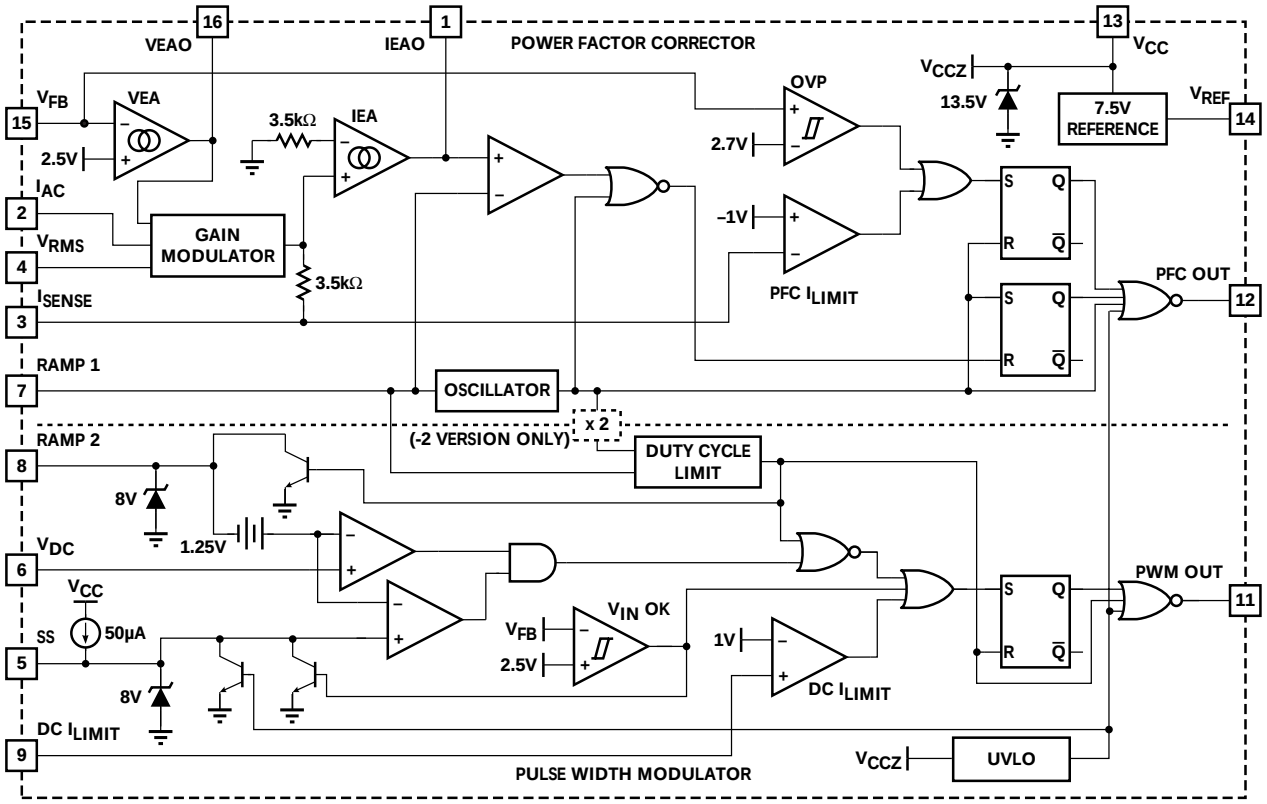


Figure 8. ML4824 Block Diagram.

PULSE WIDTH MODULATOR SECTION FOR DC TO DC CONVERTER

The pulse width modulator section is configured as a controller for a two-switch forward converter. The switch current is sensed via the voltage drop across resistor R_{18}. Resistor R_{19} and capacitor C_{17} function as a noise filter. The two switches toggle ON and OFF together at the same time. Reset of the primary side of the transformer T_2 is facilitated by diodes D_5 and D_6, which should be high voltage, high speed rectifiers.

OSCILLATOR

The oscillator frequency is determined by the values for R_T and C_T. The ON time of the oscillator is given by the following expressions:

$$T_{ON} = R_T C_T \ln \frac{V_{REF} - 1.25}{V_{REF} - 3.75} \quad (4)$$

$$\cong R_T C_T \times 0.51 \text{ for } V_{REF} = 7.5 \text{ volts}$$
$$T_{OFF} = 490 C_T \quad (5)$$

Typically, for the example circuit, which is operating at 80kHz, R_T is 52.3kΩ, and C_T is 470pF.

$$\text{Period, } T = T_{ON} + T_{OFF} + 2T_D \quad (6)$$

where T_D represents the propagation delay (approximately 20ns) of the circuit.

PFC RAMP (RAMP 1)

The peak-to-peak amplitude of the PFC ramp is set by the two voltages derived from the 7.5V bandgap reference. Two comparators are used. The upper threshold is 3.75V, the lower 1.25V. The potential difference between the two inputs to these two comparators is 2.5 volts, which is the peak-to-peak amplitude of the ramp. This ramp is used in the power factor correction section.

PWM RAMP (RAMP 2)

There is also a second ramp which can be derived from sensing the switch current, or for voltage mode control, can be derived from the output (feed-forward signal) of the power factor corrector. This second ramp is used for control of the combo's PWM DC-DC converter stage.

THE GAIN MODULATOR

The gain of the gain modulator is automatically controlled by the voltage feedback amplifier output voltage (VEAO) and the r.m.s. voltage (VRMS) from the rectifier input bridge. A third input to the gain modulator is the 120Hz A.C. line input current (IAC), which supplies an in phase sinusoidal reference.

To reduce noise, current is sampled instead of voltage. A resistor at the IAC node connected to the line will generate an input current to the gain modulator.

The gain modulator output ($I_{GM(OUT)}$) is also a 120Hz sine wave. The quality of this waveform is dependent entirely on the quality of the line voltage. If the line voltage is noisy, the output of the gain modulator will also be noisy. This is the reason why the bandwidth of VRMS and VEAO have to be low.

D.C. O.K. COMPARATOR

The output voltage of the power factor correction section is monitored by the internal D.C. O.K. comparator. If the output of this section is too low, the pulse width modulator section will not be permitted to turn ON. Once the output level reaches 380 volts DC, the pulse width modulator section will commence switching, with a programmable soft-start interval.

The power factor correction section can also be configured to have soft start by two possible arrangements. (1) the output of the current error amplifier is high impedance, and if the compensation network is tied to the reference voltage (V_{REF}), then the power factor stage will soft start. (2) If the first arrangement is not slow enough for safe starting, then extra components can be added to VEAO to assist soft start.

VOLTAGE LOOP COMPENSATION AND WIDE BANDWIDTH TRANSCONDUCTANCE AMPLIFIER

The voltage loop compensation has been sped up with a high gain, wideband uncompensated transconductance stage. A unique transconductance curve is shown in Figure 11 which is different from the conventional operational amplifier. The transconductance amplifiers on ML4824 exhibits low transconductance when the two inputs of the amplifier are balanced; and transconductance will increase when the two input voltages are unbalanced. Because of such enhancement while the system is slewing, the system bandwidth and the slew rate also increases.

The transconductance amplifier itself does not require local feedback compensation. Loop compensation is also much easier to manage.

To design a compensation network, it is required to find the power stage voltage transfer function. However, a precise PFC stage model is not available at high frequencies.

The conventional approach is to obtain a first order approximation. Below 30Hz or at half of the line frequency, the current mode model described in (2) is valid since the PFC stage never reaches the steady state above 30Hz.

The PFC stage is a resistor emulated at the line frequency. At the line frequency, the instantaneous input power, which is A.C., is not equal to the instantaneous output power, which is D.C. The instantaneous input power at the peak of the voltage waveform delivers more power than the average power required. Therefore the excessive power must be stored temporarily in the high voltage reservoir capacitor. At frequencies above the line frequency the instantaneous system power has not reached the steady state. Therefore the D.C. operating point for A.C. analysis cannot be determined. However below one half of the line frequency, the system operating point can be averaged based on the average input power.

For the voltage loop response above the line frequency, the first order model is simply a current source feeding the high voltage capacitor. See Figure 9.

$$\frac{\Delta V_{OUT}}{\Delta V_{EAO}} = \frac{AVERAGE\,P_{IN}}{V_{OUT\,DC} \times \Delta V_{EAO} \times S \times C_{DC}} = \frac{AVERAGE\,P_{IN}}{V_{OUT\,DC} \times 5.3V \times S \times C_{DC}} \quad (7)$$

Here the swing of the voltage loop error amplifier is 5.3V. This transfer function indicates the zero crossing frequency, W_C which is

$$\frac{Average\,P_{IN}}{V_{OUT\,DC} \times 5.3 \times S \times C_{DC}} \quad (8)$$

At frequencies below one half of the line frequency, the conventional current mode model can be applied.

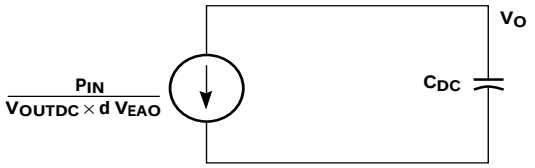


Figure 9. High Frequency Power Stage Model for Voltage Loop.

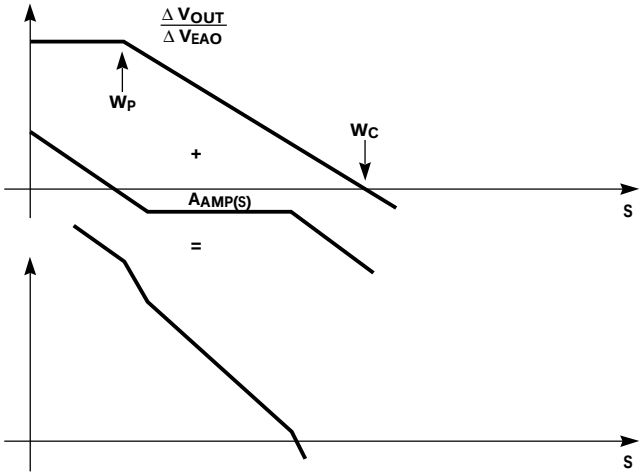


Figure 10. Overall Voltage Loop Response.

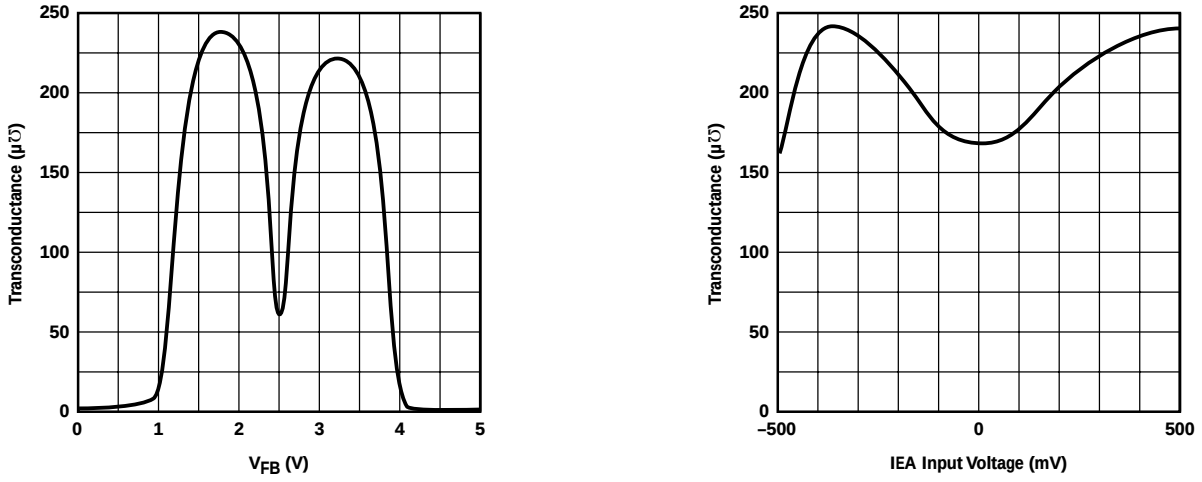


Figure 11. Voltage Loop OTA, U1, and Current Loop OTA, U2, Transconductance, GM.

The model depicts a pole location. When the duty cycle is 1, the pole is

$$\frac{2}{R_L \times C_{DC}} \quad (9)$$

Now the compensation network can be designed. If lead lag compensation is applied, the loop crossover frequency can be set around 30Hz assuming 60Hz line frequency. See Figure 10.

CURRENT LOOP COMPENSATION WITH WIDE BANDWIDTH TRANSCONDUCTANCE AMPLIFIER

The current loop error amplifier is a high performance, wideband uncompensated transconductance amplifier. The designer can adjust his own bandwidth based on the system requirement. See Figure 11.

A procedure similar to the voltage loop can be used to obtain the transfer function for the power stage of the current loop. At high frequencies, the power stage behaves as a voltage source driving an inductor. See Figure 12.

$$\omega_C = \frac{R_{SENSE} \times V_{IN}}{V_{R_TC_T\,P-P} \times L} = \frac{R_{SENSE} \times V_{IN}}{2.5V \times L} \quad (10)$$

$$\omega_P = \frac{2}{R_L \times C_{DC}} \quad (11)$$

CURRENT GAIN MODULATOR AND MAXIMUM AVERAGE POWER LIMIT

The function of the current gain modulator is similar to the method used in ML4821 to generate a reference sine wave current in phase with the line voltage. The maximum input power is also set by the gain modulator.

The gain K is curve fitted to $1/V_{RMS}^2$ gain to simplify universal input design modulators (see Figure 13). Below 1.2V, K enters a brown out protection region and will not fit the $1/V_{RMS}^2$ curve. This feature can be used to set the minimum A.C. input voltage, usually 80VAC. The $I_{GM(OUT)}$ maximum current is limited at 200µA internally. $R_{GM(OUT)}$ is an on-chip resistor of 3.5K. The high loop gain and the high bandwidth current loop amplifier will keep the product of $I_{GM(OUT)} \times R_{GM(OUT)}$ (3.5K) equal to $R_{SENSE} \times I_{IN}$. Since $I_{GM(OUT)}$ is equal to $K \times (V_{EAO} - 1.5) \times I_{AC}$, and I_{AC} is derived from the rectified sinusoidal line voltage, $I_{GM(OUT)}$ is a sine wave reference generated in phase with the sinusoidal line voltage.

TIMING DIAGRAM AND HOW TO IMPLEMENT DOUBLE FREQUENCY PWM FOR ML4824-2

There are two versions of the ML4824 available. In the ML4824-1, the PFC switching frequency is equal to the PWM switching frequency. These two sections synchronize at the rising edge of the system clock. In the ML4824-2, the PWM switching frequency is equal to twice the PFC switching frequency.

To implement $f_{PWM} = 2\ f_{PFC}$, the R_TC_T ramp have been used as a reference ramp and 4 timing areas have been generated. See Figure 14.

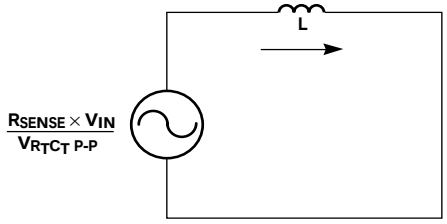


Figure 12. High Frequency Power Stage Model for Current Loop.

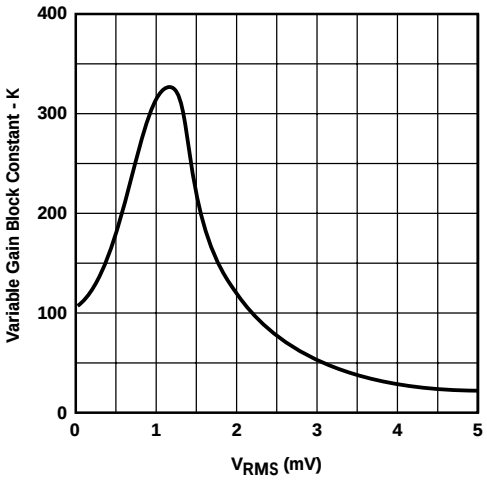


Figure 13. Gain Modulator Gain, (K).

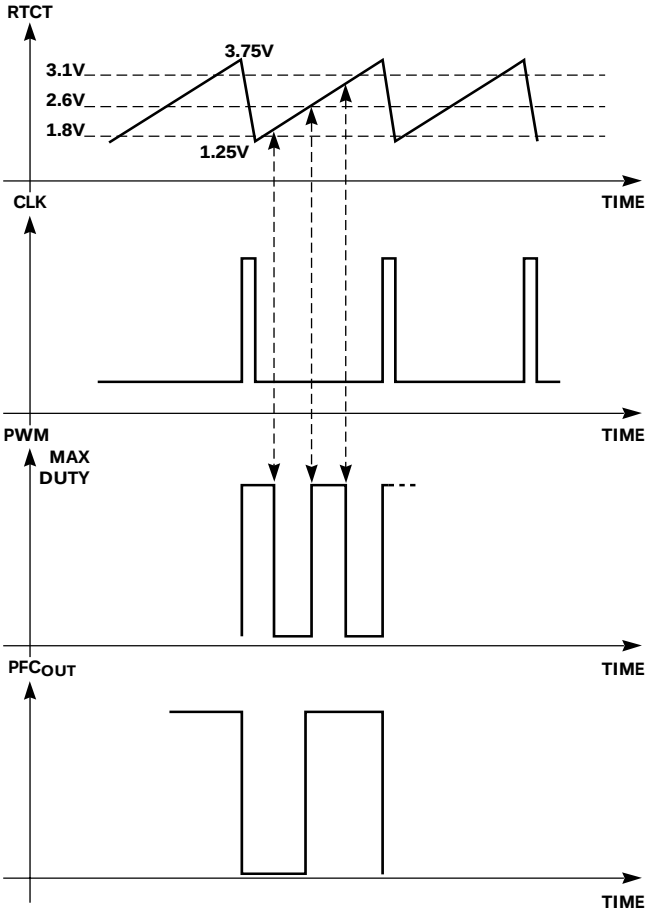


Figure 14. BL4824-2 Timing Diagram.

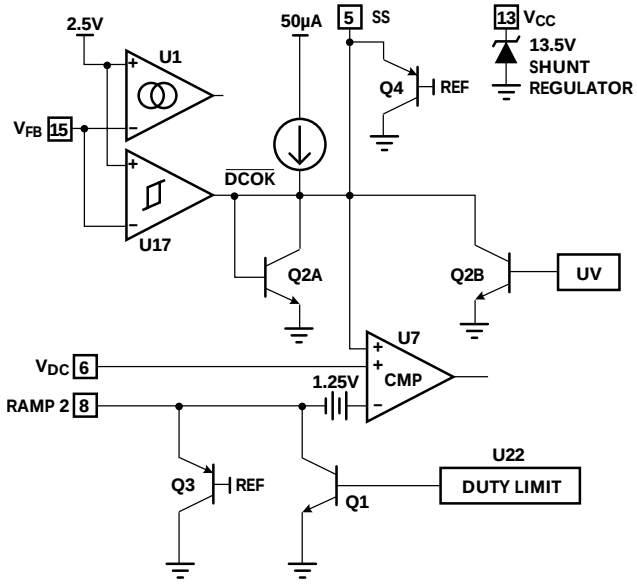


Figure 15. D.C. O.K. Comparator, PWM Comparator, and Soft Start.

D.C. O.K. COMPARATOR, UNDER VOLTAGE, AND SOFT START

The D.C. O.K. comparator, U7 monitors the PFC output to disable or enable the D.C. to D.C. PWM section. It also discharges the ISS pin. When the PFC output reaches the design value, the PWM section will monotonically ramp up the D.C. output voltage. This feature will reduce the cost of the house keeping circuitry which generates a 13.0V V_{CC}.

The ISS will be pulled down during under voltage lockout which will ensure a smooth transition to protect the components.

The PFC section also has the soft start feature due to the presence of the two transconductance amplifiers. Additional external soft start can be added, i.e., additional delay time can be configured to cause a more gradual increase of the output power, which is requested by the PFC output through the Voltage Transconductance Amplifier.

VOLTAGE MODE WITH FEED-FORWARD RAMP

In the PWM section, a voltage mode control system can be configured instead of current mode control, if desired. A feed-forward ramp can be realized by connecting a resistor between PFC high voltage D.C. output and RAMP 2, and connecting a capacitor between RAMP 2 and GND.

CONCLUSION

An integrated solution which simplifies the off-line PFC power supply design has been shown. Leading edge modulation for synchronous switching is the main feature of this controller. Noise immunity of the ML4824 is excellent because of the use of leading edge modulation for the power factor correction stage and trailing edge modulation for the D.C. to D.C. second stage. At the DC to DC stage, an internal discharge transistor on RAMP 2 reduces the switching noise right after the switch is on, so it does not require a leading edge blanking. Other features include current-mode control, 16-pin package, soft start, on-chip shunt regulator, wide bandwidth error amplifier and many other fault detection functions. Finally, to achieve optimal off-line PFC/PWM cascade power converter design, we conclude:

1. The synchronous switching method should be utilized;

2. The duty ratio of the second stage should be close to 0.5.

For more information on a typical application, please see Application Note 33, “ML4824 Combo Controller Applications.”

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3. J. Dronik, “Is Cascade Connection of Power Converters Inefficient?” Proc. PCIM Power Conversion Conference pp. 34–43, 1993

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