ESD FAIL!

You thought your electrostatic-discharge protection was bulletproof, yet the IC still fried in test. Now what?

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Key points:
- ESD protectors with low dynamic resistance won't necessarily protect circuits.
- Most damage is caused within the first nanosecond of an ESD event.
- The ESD protector should set as close as possible to the point of current entry, not to the device being protected.

Resources:
Littelfuse Inc., *www.littelfuse.com*
Circle 622

Dissipating static safely, *http://machinedesign.com/article/dissipating-static-safely-0705*

Top tips on squelching electrical noise, http://machinedesign.com/article/top-tips-on-squelching-electrical-noise-0619

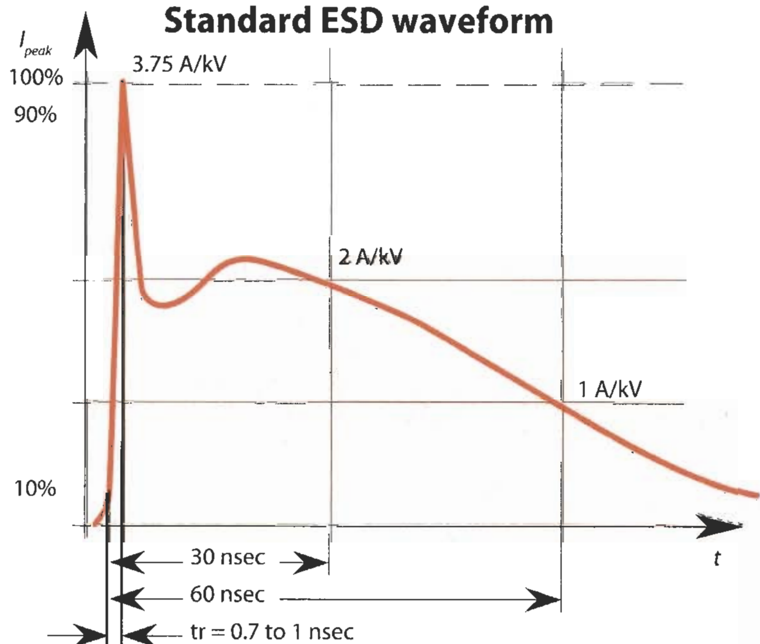
The generally accepted main goal of electrostatic-discharge (ESD) protection is to provide a low-resistance shunt path to ground (GND) for unwanted voltage spikes. A key to how well such measures serve their purpose is its dynamic-resistance figure used in the selection process. Fortunately, there are well-known ways to calculate the effective dynamic-resistance that protection devices, such as polymeric ESD suppressors or silicon-diode arrays, exhibit during an ESD transient.

Logic dictates that the device with the lowest dynamic resistance should give the best chance of dissipating spikes. But sometimes it doesn't. All is not lost, however, as several techniques help boost the level of ESD protection.

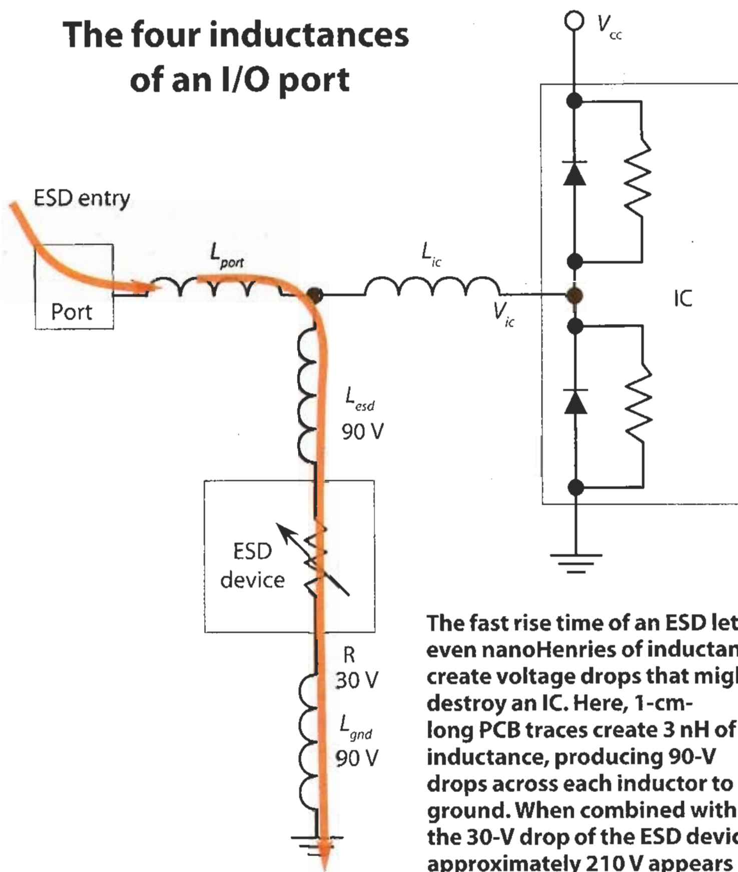
The challenge

The standard ESD pulse shape is defined by IEC61000-4-2. It specifies an initial current spike with a peak voltage of 2,000 to 8,000 V and a rise time of 0.7 to 1.0 nsec. Current level is rated at 3.75 A/kV at the peak voltage, or 30 A for an 8-kV voltage test. Current levels at 30 and 60 nsec are also specified at 2 A/kV and 1 A/kV, respectively.

This presents a special challenge to many modern electronic products built with state-of-the-art chipsets that use construction technologies well below 130 nm. These technologies poorly tolerate any dc voltage over 3.3 V, so an ESD pulse can be catastrophic for such a device. Furthermore, chipmakers have reduced onboard or



The ESD threat/pulse is defined by the IEC61000-4-2 standard.



The fast rise time of an ESD let even nanoHenries of inductance create voltage drops that might destroy an IC. Here, 1-cm-long PCB traces create 3 nH of inductance, producing 90-V drops across each inductor to ground. When combined with the 30-V drop of the ESD device, approximately 210 V appears on the input to the IC.

on-chip ESD protection to 500 V, well below the typical field requirement of 8 kV.

Board designers not only need external ESD protection, but also need to make sure it's robust enough to protect small-geometry chipsets. Just placing an 8-kV rated ESD protection device on the data lines or I/O pins being protected does not guarantee the chip set itself will pass an 8 kV in-system test.

Board layout and device location are crucial for effective protection from ESD. To that end, the designer must understand the effects that parasitic inductances have at the board level. For example, an 8-kV ESD strike at the test specification of 30 A through a printed-circuit board (PCB) trace with just 1-nH inductance generates a 30-V spike on that trace. This voltage is calculated using the equation:

$$V_{L,\,parasitic} = L_{parasitic} \times di/dt$$

where $L_{parasitic}$ is the parasitic inductance of the trace and $V_{L,\,parasitic}$ is the voltage developed across it with the change in current over time, di/dt.

In looking at a typical circuit-board layout, the input trace circuit can be divided into four separate areas: the trace from the input to the junction of the ESD device (L_{port}), the trace from the ESD junction to the input of the IC (L_{IC}), the trace from the junction of the ESD device to the device itself (L_{ESD}), and the trace from the ESD device to ground (L_{GND}). These four parasitic inductances, L_{ESD}, L_{GND}, L_{IC}, and L_{port}, must be considered when deciding on the placement of the ESD device. L_{ESD} and L_{GND} tend to raise the clamping voltage (V_{IC}) while L_{IC} and L_{port} work to the designer's advantage to lower V_{IC}.

Shorten traces to lower L_{ESD} and L_{GND}

Sometimes a board's layout prevents an ESD device being placed directly atop the PCB trace. Reasons vary, but placing an ESD component even 1 cm away from the data line being protected can ultimately translate into tens of volts on the device. The same is true for ground (GND) buses. In some designs the ESD device GND must pass through multiple vias and may even take a circuitous path to reach the GND plane. Both of these inductances create voltage spikes in addition to the voltage created by the ESD current flowing through the ESD device given by $V_{ESD} = I_{peak} \times R_{dynamic}$, where V_{ESD} is the voltage drop across the ESD device, I_{peak} is the peak current of the electrostatic event, and $R_{dynamic}$ is the resistance of the ESD device as it conducts.

The following simplified examples show how L_{ESD} and L_{GND} affect V_{IC}. Common PCB manufacturing processes give approximately 3 nH/cm for typical microstrip traces assuming certain widths, thicknesses, and dielectric constants. With that in mind, assume an 8kV ESD pulse is applied to the input of the I/O pin. The ESD device has a 1-Ω dynamic resistance. The first layout assumes both L_{ESD} and L_{GND} equal 1.5 nH (0.5-cm spacing):

$$V_{IC} = (L_{ESD} + L_{GND}) \times di/dt + I_{peak} \times R_{dynamic}$$

$$V_{IC} = (1.5\text{ nH} + 1.5\text{ nH}) \times 30\text{ A}/1\text{ nsec} + 30\text{ A} \times 1.0\ \Omega = 120\text{ V}$$

The second layout doubles the length of the traces, so each become 1-cm long for 3-nH each:

$$V_{IC} = (3\text{ nH} + 3\text{ nH}) \times 30\text{ A}/1\text{ nsec} + 30\text{ A} \times 1.0\ \Omega = 210\text{ V}$$

This example shows that lengthening the ESD protector trace from 0.5 to 1 cm increases V_{IC} by 75%! So the rule is to keep the traces connecting the ESD protector as short as possible.

Shrink the ratio of L_{port} to L_{IC}

Often datasheets for ESD protectors recommend putting the device as close as possible to the point of ESD

entry. Manufacturers do this so the ratio of L_{port} to L_{IC} is as small as possible ($L_{IC} >> L_{port}$). The inductance of L_{port} will not necessarily affect the overall ESD performance but the inductance of L_{IC} most certainly will.

The nonlinearity of L_{IC} acts as a buffer to the initial peak of the ESD current pulse. This creates a substantial voltage drop toward the IC. This inductance gets smaller the closer the ESD device gets to the IC, and the voltage drop shrinks to the point where it provides no additional advantage. So it's in the designer's interest to make the ratio of L_{port} to L_{IC} as small as possible to take advantage of the parasitic nature of the PCB trace.

Use of L_{IC} and L_{port} is a straightforward way to improve overall ESD performance. However, there are designs that will still fail prematurely no matter how low the aforementioned ratio. In other words, the value of L_{IC} does not sufficiently buffer the peak ESD current.

Adding a buffer resistor

One problem with the previous techniques is that the on-chip ESD structures can see too much current. They then become damaged, shorting the I/O to *GND* or V_{CC}.

The ESD protector and the IC being protected actually share current from an ESD pulse. For example, a positive ESD pulse lets the protection device take the majority of the current, but some current travels into the IC and is routed out the V_{CC} terminal. The overall circuit forms a resistive current divider between the ESD protector and the IC.

The rail diode on the IC is responsible for steering the remaining or "let-through" current into V_{CC} where it returns to GND through a bypass capacitor. It's difficult to determine the equivalent resistance for the IC's ESD protection, but it's undoubtedly higher than the on-board ESD device. For example, if the resistance of the on-chip protection (R_{chip}) is 10 Ω, and the $R_{dynamic}$ for the external ESD protector is 1 Ω, the peak current seen by the IC is:

$$I_{IC} = I_{peak} * R_{dynamic}/(R_{dynamic} + R_{chip})$$
$$I_{IC} = 30\text{ A} * 1\ \Omega/(1\ \Omega + 10\ \Omega) = 2.73\text{ A}$$

Resistors added in series between the external ESD device and the IC help lower peak current flow into the IC. For this example, adding a 10-Ω buffer resistance (R_{buffer}) reduces the peak current flowing into the IC by almost 50%.

$$I_{IC} = I_{peak} * R_{dynamic}/(R_{dynamic} + R_{buffer} + R_{chip})$$
$$I_{IC} = 30\text{ A} * 1\ \Omega/(1\ \Omega + 10\ \Omega + 10\ \Omega) = 1.43\text{ A}$$

Obviously, a resistance beyond 10 Ω would further reduce the let-through current. The details of the application determines the maximum resistance permitted.

Care must be taken when employing this technique in some of the high-speed applications such as high-definition multimedia interface (HDMITM) and USB 3.0. The R_{buffer} resistor could disturb the line impedance and attenuate the signal beyond the standards' compliance specifications. Careful board design can compensate for any ill effects. Nevertheless, board designers should keep this technique in their toolbox and apply it in situations where the board or in-system ESD level falls below their requirement.

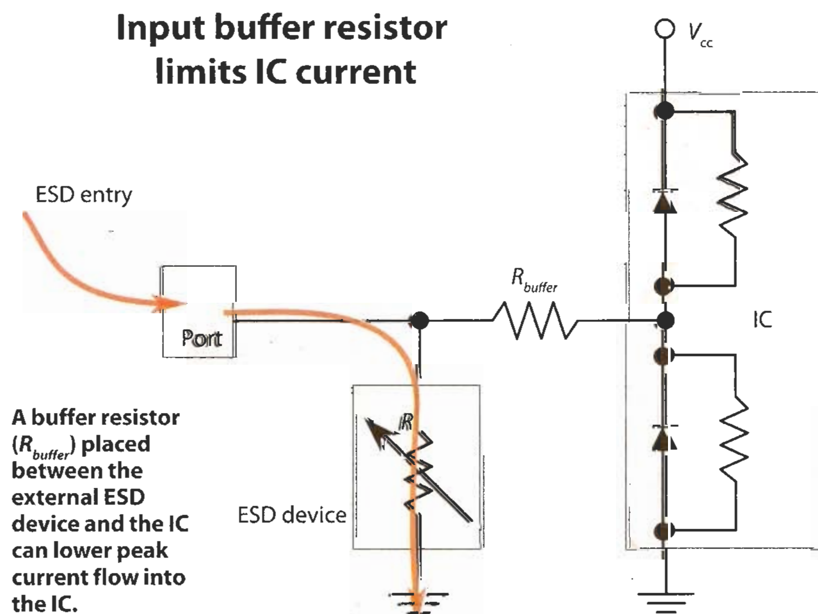
Four simple steps to success

The ESD protection device alone may not be enough to protect modern chip sets from ESD transients. Fortunately, board designers can use these four strategies to optimize ESD protection:

1. Reduce the length of the parasitic stub trace or L_{ESD}.
2. Reduce the length of the GND trace and/or number of vias used to decrease L_{GND}.
3. Make the ratio of L_{port} to L_{IC} as small as possible on a given design.
4. Use buffering resistors between the ESD device and IC if the above are still insufficient.

All these practices reduce the voltage seen by the IC, as well as limit the amount of current the on-chip ESD structures must handle. Following these simple rules will give the board designer a more robust ESD solution that exceeds industry standards. **MD**

Input buffer resistor limits IC current



A buffer resistor (R_{buffer}) placed between the external ESD device and the IC can lower peak current flow into the IC.