Simple Voltmeter Monitors TTL Supplies

National Semiconductor
Linear Brief 48
Michael Maida

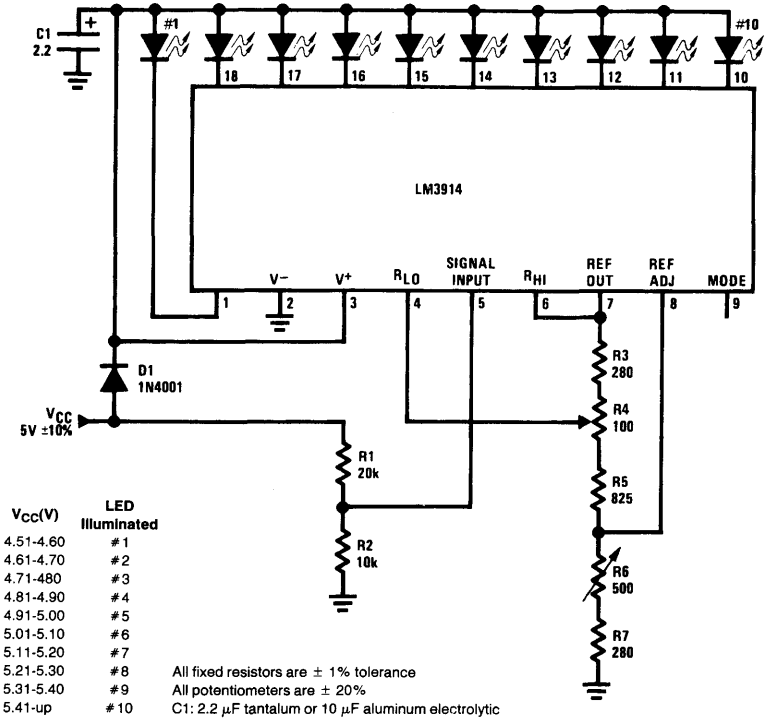
Using a National Semiconductor LM3914 bar/dot display driver chip, a few resistors and some LEDs, a simple expanded-scale voltmeter is easily constructed. Furthermore, it runs from the same single 5V ± 10% supply it monitors and can provide TTL-compatible undervoltage and overvoltage warning signals.

The complete circuit is shown in *Figure 1*. Resistors R1 and R2 attenuate V_{CC} by a factor of three at the LM3914 signal input, ensuring proper biasing of the IC with V_{CC} as low as 4V. The IC's internal reference sets the voltage across the series combination of R3, R4 and R5 at 1.25V, establishing a reference load current of about 1 mA. This current is joined by the small, constant current from the reference adjust pin (75 μA, typ) and flows to ground through R6 and R7, developing a voltage drop. Adjusting R6 varies this voltage drop and, consequently, the voltage at pin 7, nominally 1.803V (= 5.41V/3).

Pin 7 is connected to the top of the LM3914's internal ten-step voltage divider (pin 6). The bottom of this divider (pin 4) is connected to the center tap of potentiometer R4. By varying the pot setting this voltage can be set to 1.47V (= 4.41V/3) without significantly affecting the potential at pin 7. The optional diode D1 protects against damaging the IC by connecting the leads backwards.

In operation, the LM3914's ten internal voltage comparators compare the signal input, $V_{CC}/3$, to the reference voltage on the divider, lighting each successive LED for every 100 mV increase in V_{CC} above 4.5V as shown. The LM3914 regulates the LED currents at 10 times the reference load current, here about 10 mA, so external current-limiting resistors are not required. With pin 9 left open circuit, the LM3914 functions in Dot mode (only one LED on at a time). If desired, a Bar mode display could be obtained by connecting pin 9 to V_{CC}, but the dot display seems more suitable in this application.

To calibrate, set V_{CC} at 5.41V and adjust R6 until LED #9 and LED #10 are equally illuminated. (A built-in overlap of about 1 mV ensures all LEDs won't go out at a threshold point.) There's no need to vary the system supply voltage to perform this adjustment. Instead, disconnect R1 from V_{CC} and connect it to an accurate reference. Then, at 4.5V, adjust R4 until LED #1 just barely turns on. There is a slight interaction caused by the finite resistance (10k, typ) of the LM3914's voltage divider, so that repeating the above procedure once is advised.



V_{CC}(V)	LED Illuminated
4.51-4.60	#1
4.61-4.70	#2
4.71-480	#3
4.81-4.90	#4
4.91-5.00	#5
5.01-5.10	#6
5.11-5.20	#7
5.21-5.30	#8
5.31-5.40	#9
5.41-up	#10

All fixed resistors are ± 1% tolerance
All potentiometers are ± 20%
C1: 2.2 μF tantalum or 10 μF aluminum electrolytic

TL/H/8496–1

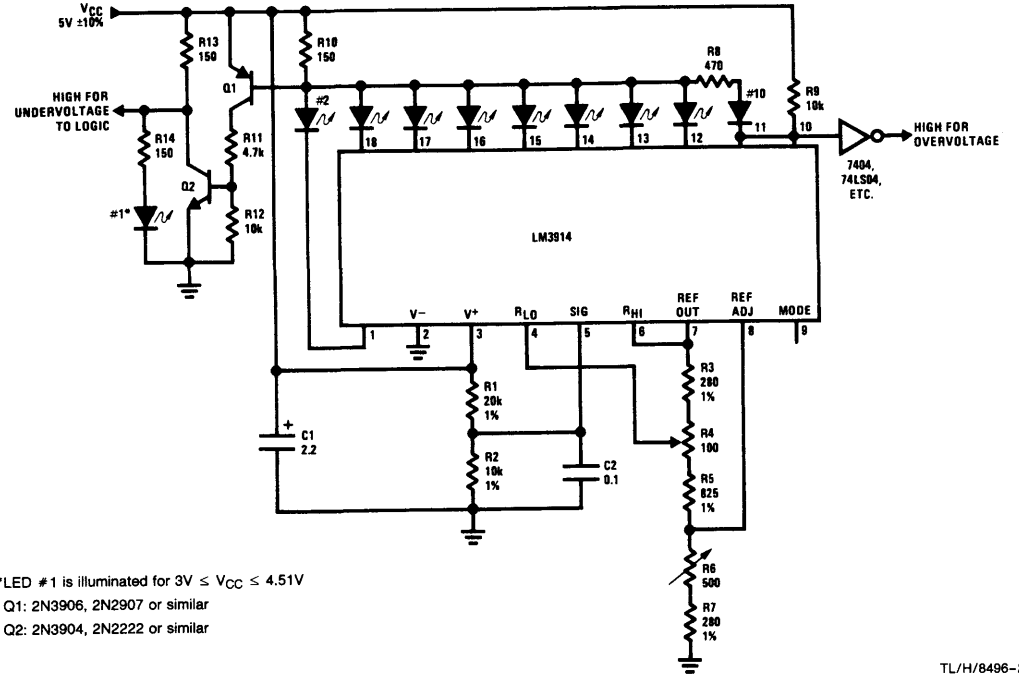
FIGURE 1. 5V Power Supply Monitor

The LED driver outputs can directly drive a TTL gate, so that the LED #1 and LED #10 outputs may be used for undervoltage and overvoltage warning signals. These may be used to initiate a soft shutdown or summon an operator, for example. The interfacing circuitry is shown in *Figure 2*. The 470Ω resistor R8 ensures that the LM3914 output will saturate to provide the proper TTL low level. Pull-up resistor R9 provides the logic high level.

In the previous circuit the undervoltage LED goes out when V_{CC} is less than 4.51V, a deficiency that is corrected here, Transistors Q1 and Q2 shut off LED #1 whenever any other LED is turned on by the LM3914. Q2's output will directly drive TTL.

Calibration procedure is the same as before. The LM3914 output thresholds have been shifted up by 100 mV and output #10 is or-tied with output #9. Other outputs may be wire-or'd together if 100 mV resolution is not necessary. If desired, the outputs can be color coded by making LED #1 and LED #10 red, LED #2 and LED #9 amber, and the rest of the LEDs green to ease interpretation.

This circuit is useful where quick and easy voltage adjustments must be made, such as in the field or on the production line. The circuit's low cost makes it feasible to incorporate it into the system, where the overvoltage and undervoltage warning signals provide an attractive extra. Of course, these techniques can be used to monitor any higher voltages, positive or negative.



*LED #1 is illuminated for 3V ≤ V_{CC} ≤ 4.51V

Q1: 2N3906, 2N2907 or similar

Q2: 2N3904, 2N2222 or similar

TL/H/8496–2

FIGURE 2. Power Supply Monitor with TTL Interface and Extended Undervoltage Range

Programmable Power Regulators Help Check Out Computer System Operating Margins

National Semiconductor
Linear Brief 49
Robert Pease

It is a familiar situation that some computer systems which are functional with a 5V supply may run marginally at 5.1V but can show a solid failure at 5.3V (or, vice versa) even though all these voltages are within the system's specifications. The LM338 is an example of a monolithic voltage regulator which can be placed under computer control, and can trim the supply to a particular variation above (and below) the design-center voltage. Simultaneously the computer is exercised through a standard test sequence. Any deviation from correct functioning, at one supply voltage level or another, will serve as a warning of impending malfunction or failure. This test approach can be used for diagnostics, for troubleshooting, and for engineering evaluation. It can help detect skew, race conditions, timing problems, and noise and threshold problems.

HERE'S HOW

During normal operation, the latch (IC 1) is programmed to have its Q1 and Q2 outputs *HIGH*, and its Q3 and Q4 *LOW*. Then R4 and R5 are connected effectively in parallel with R6, and V_{OUT} is adjusted to 5V. If Q4 is commanded *HIGH*, the net conductance from the *adjust bus* to ground will decrease, and V_{OUT} will rise 3% to 5.151V. Conversely if Q1 is commanded *LOW*, the output voltage will fall 3.3% to 4.835V. The complete list of output voltages (in approximately 3.2% steps) is shown in Table I, covering a ±9.5% total range.

The same basic function can be accomplished for −5.2V regulators (as are used for ECL) using LM337 negative adjustable regulators. If the command is from TTL latches, the circuit of *Figure 2* will be suitable to interface between the (0V and 2.4V) logic levels and the saturated PNP collectors as shown. The resistors R101–R104 are switched by transistors Q101–Q104 in a similar way to *Figure 1*. Note that the resistors in *Figure 2* are in a binary-weighted proportion. To decrease V_{OUT} by 2%, just change Q4 to *LOW*, but to *increase* V_{OUT} by 2%, set Q1 *HIGH* and Q2, Q3, Q4 all *LOW*, in a standard offset binary scheme.

TABLE I. Available Trim Range

Q1	Q2	Q3	Q4	V_{OUT}	$\%\Delta V_{OUT}$
1	1	0	0	5.000V	(trimmed)
1	1	0	1	5.151V	+3.0%
1	1	1	0	5.299V	+6.0%
1	1	1	1	5.469V	+9.4%
0	1	0	0	4.835V	−3.3%
1	0	0	0	4.669V	−6.6%
0	0	0	0	4.526V	−9.5%

Figure 2 also provides another feature. If Q5 goes *LOW*, Q105 will saturate and pull the adjust bus to within 100 mV of ground, and the V_{OUT} will collapse to −135V. The negative supply will be effectively shut down, and the computer will draw substantially zero power.

In an extreme case of automation, the computer could trim the −5.2V supply to the "best" value, and the trimpot would be completely superfluous. The circuit of *Figure 2* has a trim resolution of 3% steps, and can set V_{OUT} well within 2% of the ideal value, so long as some measurement has decided which voltage is "ideal".

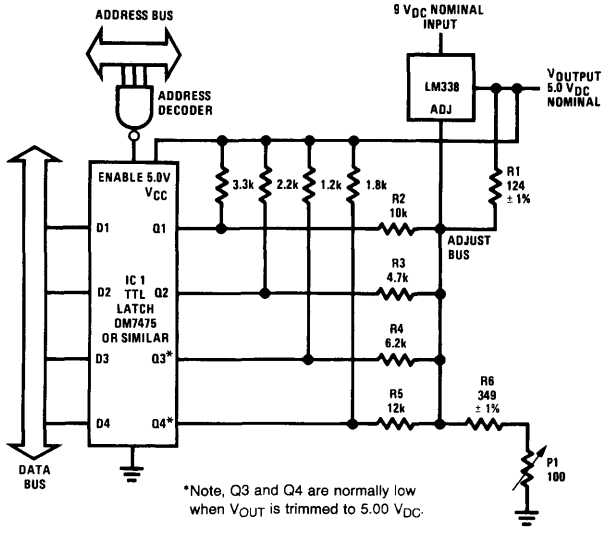


FIGURE 1. Programmable Power Supply

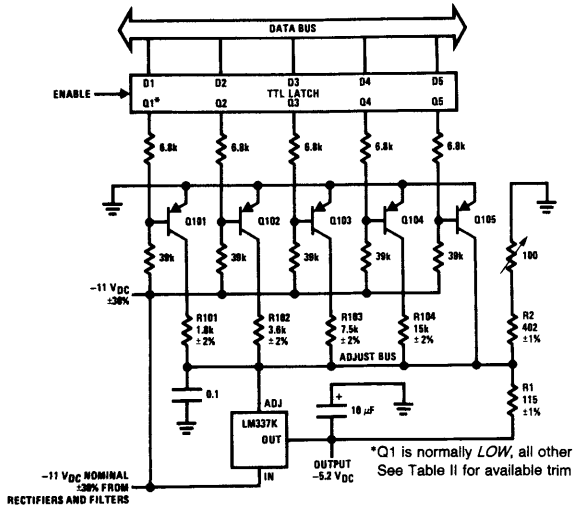


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FIGURE 2. Programmable Negative Supply

TABLE II. Available Trim Range

Q1	Q2	Q3	Q4	V_{OUT}	$\%\Delta V_{OUT}$
0	1	1	1	5.200V	(trimmed)
0	1	1	0	5.110V	−1.7%
0	1	0	1	5.025V	−3.4%
0	1	0	0	4.944V	−4.9%
0	0	1	1	4.853V	−6.7%
0	0	1	0	4.779V	−8.1%
0	0	0	1	4.707V	−9.5%
0	0	0	0	4.638V	−10.8%
1	0	0	0	5.310V	+2.1%
1	0	0	1	5.409V	+4.0%
1	0	1	0	5.513V	+6.0%
1	0	1	1	5.622V	+8.1%
1	1	0	0	5.757V	+10.7%
1	1	0	1	5.880V	+13.1%
1	1	1	0	6.010V	+15.6%
1	1	1	1	6.147V	+18.2%

Add Kelvin Sensing and Parallel Capability to 3-Terminal Regulators

National Semiconductor
Linear Brief 51

Paralleling of 3-terminal regulators is generally not recommended because the devices do not share current equally. If, for instance, you try to make a 3 amp regulator using three 1 amp regulators, the device with the highest output could be carrying 2.5 amps in a current limit mode. The regulator with the second highest output would be carrying only 0.5 amps, and the third regulator would be totally off. The reliability of such a system is poor because of the combination of high temperature and high current in the first regulator. A simple way to improve sharing is to insert a low value resistor in series with each output. The problem with this approach is that load regulation is very poor if the resistors are made large enough to ensure adequate sharing.

A new technique for current sharing overcomes the load regulation problem and, as an added bonus, provides remote sensing capability not available in the standard 3-terminal regulators. This is a great advantage when the regulators must be mounted off-card with their outputs fed through a connector. Total cost of added components is less than 50¢.

Figure 1 shows the new Kelvin sense scheme using the LM338 5 amp adjustable regulator. A1 forces a voltage drop across R3 equal to the voltage across the parasitic resistance, r_S. The current through R3 flows into the output of A1 and out the negative supply pin. This creates a voltage drop across R4 just equal to the voltage across r_S, cancelling the effect of r_S on load regulation. There is an error in V_{OUT} created by the quiescent current of A1, but for a 5V output, this error is only about 0.7%. Voltage loss across r_S must be limited to 300 mV to avoid current limiting in A1. If larger drops must be accommodated, R3 and R4 will have to be increased. C1 is necessary only if intermediate values of capacitance (2 μF–20 μF) are put directly across the load. Any of the positive adjustable regulators may be used in place of the LM338.

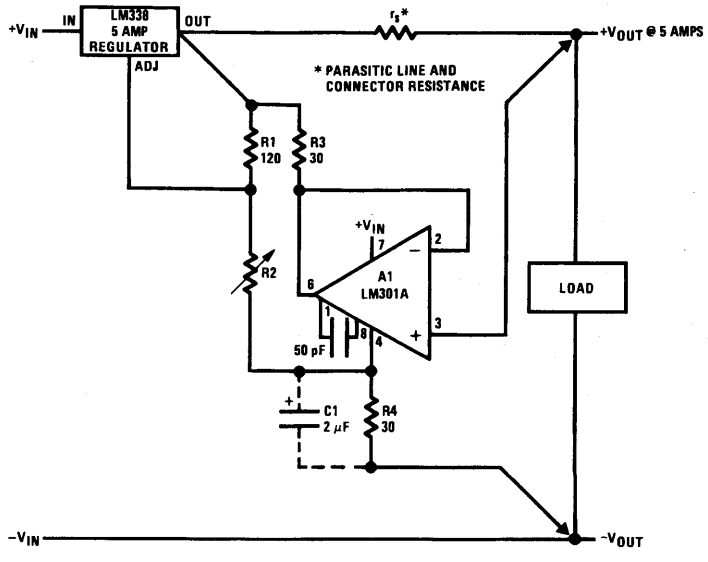

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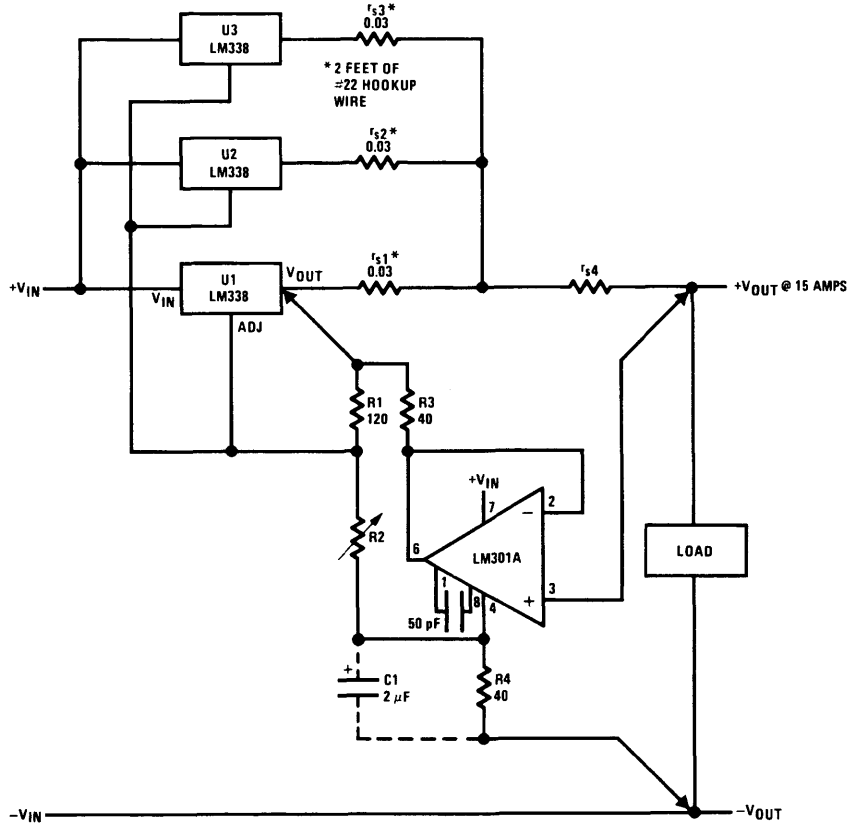
FIGURE 1

Figure 2 combines Kelvin sensing with paralleling, where the voltage loss across the current sharing resistors is corrected by the sensing connection. r_{S1} through r_{S3} are equal lengths of #22 gauge lead wire which act as ballasting resistors. These resistors can be kept small because LM338 adjustment pins are paralleled, forcing the outputs to track to within about 60 mV. r_{S4} consists of the parasitic resistance of any additional output lead plus connector loss. The total loss for r_{S4} may be up to 0.25V without loss of proper Kelvin sensing. Note that if U1 has the lowest reference voltage of the three regulators, full Kelvin sensing might not become effective until output current has increased above a threshold value of several amps. If this is undesirable, the adjustment pin of U1 may be connected to a 5Ω tap on R1, increasing its effective reference voltage by 50 mV. The current load for U1 would be 1.5 amps higher, however.



TL/H/8498-2

FIGURE 2

A Low-Noise Precision Op Amp

National Semiconductor
Linear Brief 52
Robert A. Pease

It is well known that the voltage noise of an operational amplifier can be decreased by increasing the emitter current of the input stage. The signal-to-noise ratio will be improved by the increase of bias, until the base current noise begins to dominate. The optimum is found at:

$$I_{e(optimum)} = \frac{KT}{q} \frac{\sqrt{h_{FE}}}{r_s}$$

where r_s is the output resistance of the signal source. For example, in the circuit of *Figure 1*, when $r_s = 1\ k\Omega$ and $h_{FE} = 500$, the I_e optimum is about 500 μA or 560 μA. However, at this rich current level, the DC base current will cause a significant voltage error in the base resistance, and even after cancellation, the DC drift will be significantly bigger than when I_e is smaller. In this example, $I_b = 1\ \mu A$, so $I_b \times r_s = 1$ mV. Even if the I_b and r_s are well matched at each input, it is not reasonable to expect the $I_b \times r_s$ to track better than 5 or 10 $\mu V/°C$ versus temperature.

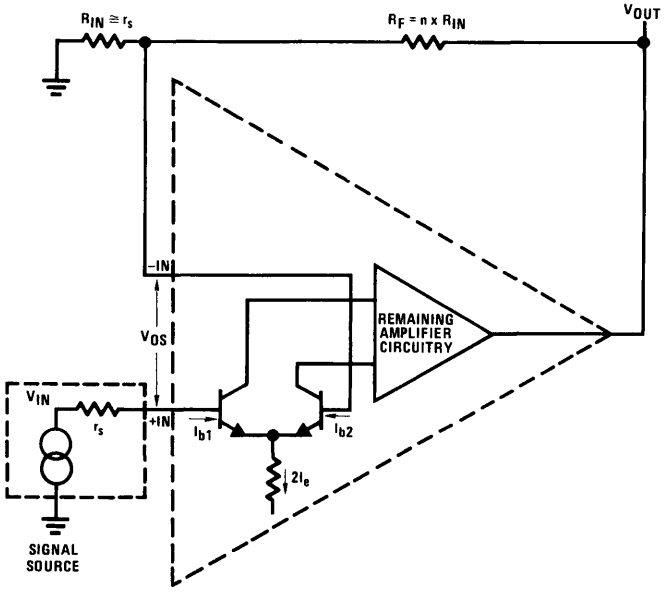
A new amplifier, shown in *Figure 2*, operates one transistor pair at a rich current, for low noise, and a second pair at a much leaner current, for low base current. Although this looks like the familiar Darlington connection, capacitors are added so that the noise will be very low, and the DC drift is very good, too. In the example of *Figure 2*, Q2 runs at $I_e = 500\ \mu A$ and has very low noise. Each half of Q1 is operated at 11 $\mu A = I_e$. It will have a low base current (20 nA to 40 nA typical), and the offset current of the composite op amp, $I_{b1} - I_{b2}$, will be very small, 1 nA or 2 nA. Thus, errors caused by bias current and offset current drift vs. temperature can be quite small, less than 0.1 $\mu V/°C$ at $r_s = 1000\Omega$.

The noise of Q1A and Q1B would normally be quite significant, about 6 $nV/\sqrt{Hz}$, but the 10 μF capacitors completely filter out the noise. At all frequencies above 10 Hz, Q2A and Q2B act as the input transistors, while Q1A and Q1B merely buffer the lowest frequency and DC signals.

For audio frequencies (20 Hz to 20 kHz) the voltage noise of this amplifier is predicted to be 1.4 $nV/\sqrt{Hz}$, which is quite small compared to the Johnson noise of the 1 kΩ source, 4.0 $nV/\sqrt{Hz}$. A noise figure of 0.7 dB is thus predicted, and has been measured and confirmed. Note that for best DC balance R6 = 976Ω is added into the feedback path, so that the total impedance seen by the op amp at its negative input is 1 kΩ. But the 976Ω is heavily bypassed, and the total Johnson noise contributed by the feedback network is below $\frac{1}{2}$ $nV/\sqrt{Hz}$.

To achieve lowest drift, below 0.1 $\mu V/°C$, R1 and R2 should, of course, be chosen to have good tracking tempco, below 5 ppm/°C, and so should R3 and R4. When this is done, the drift referred to input will be well below 0.5 $\mu V/°C$, and this has been confirmed, in the range +10°C to +50°C.

Overall, we have designed a low-noise op amp which can rival the noise of the best audio amplifiers, and at the same



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$$V_{OUT} \cong (n+1)\,V_{IN} + V_{OS} \times (n+1) + (I_{b2} - I_{b1}) \times r_s \times (n+1) + V_{noise} \times (n+1) + i_{noise} \times (r_s + R_{IN}) \times (n+1)$$

FIGURE 1. Conventional Low-Noise Operational Amplifier

time exhibits drift characteristics of the best low-drift amplifiers. The amplifier has been used as a precision pre-amp (gain = 1000), and also as the output amplifier for a 20-bit DAC, where low drift and low noise are both important.

To optimize the circuit for other r_s levels, the emitter current for Q2 should be proportional to $1/\sqrt{r_s}$. The emitter current of Q1A should be about ten times the base current of Q2A. The base current of the output op amp should be no more than 1/1000 of the emitter current of Q2. The values of R1 and R2 should be the same as R7.

Various formulae for noise:

Voltage noise of a transistor, per $\sqrt{Hz}$, $e_n = KT\sqrt{\frac{2}{qI_C}}$

Current noise of a transistor, per $\sqrt{Hz}$, $i_n = \sqrt{\frac{2qI_C}{h_{FE}}}$

Voltage noise of a resistor, per $\sqrt{Hz}$, $e_n = \sqrt{4\,KTR_S}$

For a more complete analysis of low-noise amplifiers, see AN-222, "Super Matched Bipolar Transistor Pair Sets New Standards for Drift and Noise", Carl T. Nelson.

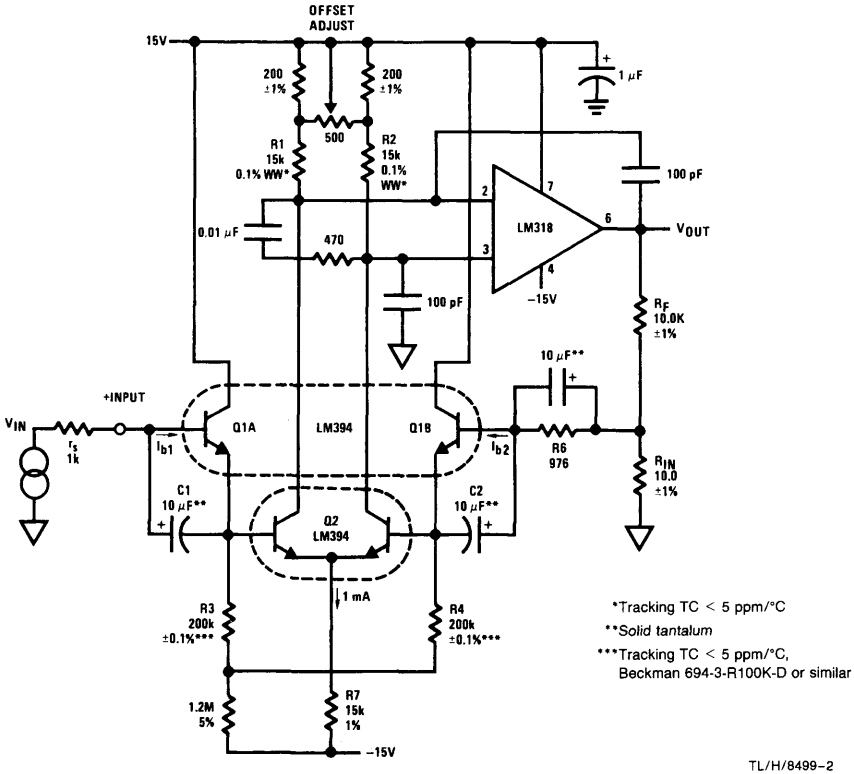

FIGURE 2. New Low-Noise Precision Operational Amplifier as Gain-of-1000 Pre-Amp

μP Interface for a Free-Running A/D Allows Asynchronous Reads

National Semiconductor
Linear Brief 53
Tim Regan

In many data acquisition applications it is necessary to have an A to D converter operate as its maximum conversion rate. The controlling microprocessor would then be able to read the most current input data at *any* point in time as required by software. To minimize program execution time, a DATA READ may not be snychronous to the completion of a conversion, and herein lies a problem. It is entirely possible that the processor could assert a READ command right at the instant the A/D converter is updating its output register. The data read would be the value of the converter's output lines in transition from the result of the previous conversion to the latest result, and would very likely be in error.

The addition of a simple binary counter to the A/D interface circuitry can be used to generate a READY signal to the microprocessor that will prevent a READ during a data update. The circuit of *Figure 1* shows a CD4024BC7-stage ripple carry binary counter used in conjunction with an ADC0801, 8-bit microprocessor compatible A to D converter. Circuit operation relies on two basic properties of the A/D converter. First of all, the free-running conversion time of the A/D must be a constant number of clock cycles; and secondly, the output latches must be updated prior to the end of conversion signal. The ADC0801 fulfills both of these requirements. The output data latches are updated one A/D clock period before the $\overline{INTR}$ falls low, and the free-running conversion time is always 72 clock periods long.

As part of the system power-up initializaton sequence, a logic low must be temporarily applied to the $\overline{SYSTEM\ RESET}$ input to the A/D to force the converter to start. At the end of a conversion, the $\overline{INTR}$ output goes low, and both resets the counter outputs to all zeros and signals another conversion to start by pulling $\overline{WR}$ low. The length of time that the $\overline{INTR}$ output stays low is normally only a few internal gate propagation delays (approximately 300 ns) and is independent of the A/D clock frequency. The 1000 pF capacitor on this output extends this time to approximately 1 μs to insure adequate reset time for the counter.

A conversion is started on the low to high transition of the $\overline{INTR}$ and $\overline{WR}$ pins. The next data update will occur 71 clock periods after this edge occurs. The counter will signal that a data update is about to occur after 64 clock periods. If the processor attempts a DATA READ within an 8 clock period time frame around the data update time, its READY input line will remain low, signifying a NOT READY condition. The processor would then extend the READ cycle time until it receives a READY indication created by the counter being reset by $\overline{INTR}$. This insures that the latches have already been updated and proper data will be read.

If a READ is attempted during the 64 clock period interval after the start of a conversion, the READY IN line to the processor will go high to permit a normal READ cycle, and

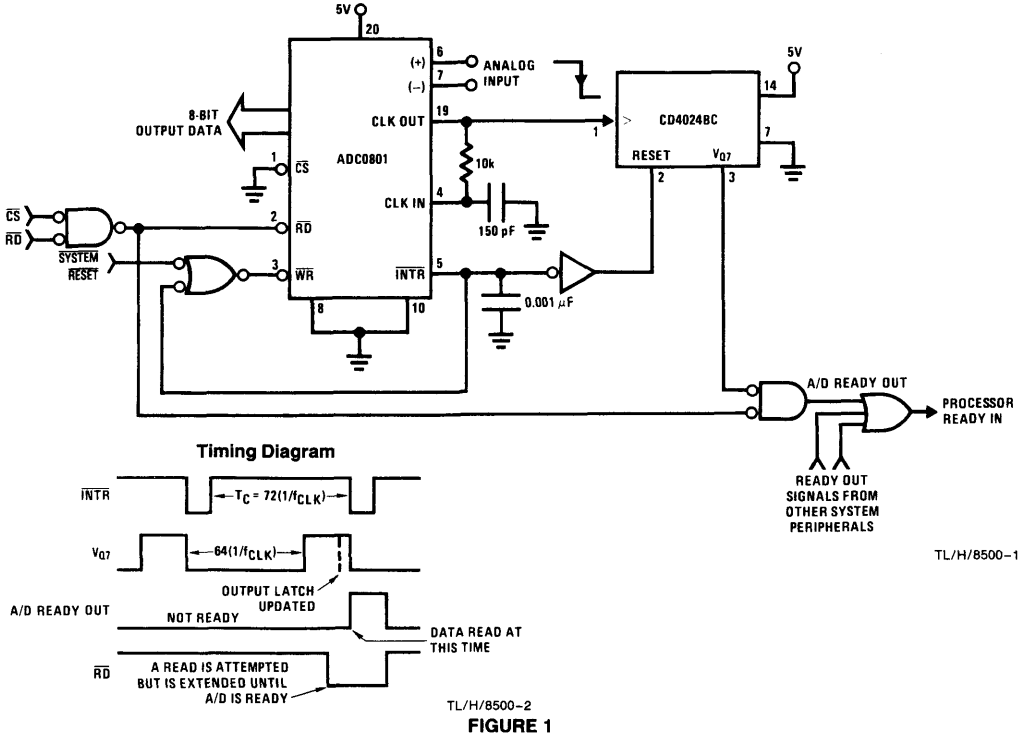

FIGURE 1

the data output by the A/D will be the result of the previous conversion. The processor READY IN logic, as shown, requires that all system devices that may need special READ or WRITE timing provide a NOT READY (a Logic 0 on their READY OUT lines) indication until selected to be read from or written to.

The chance of having the processor extend its READ cycle time is 1 in 9 (8 clock periods out of 72) and the maximum length of time a READ would be extended is 8 A/D clock periods. These two timing considerations are insignificant trade-offs to take to insure that proper A/D data is always read.

The Monolithic Operational Amplifier: A Tutorial Study

National Semiconductor
Appendix A

Invited Paper—
IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6

Abstract—A study is made of the integrated circuit operational amplifier (IC op amp) to explain details of its behavior in a simplified and understandable manner. Included are analyses of thermal feedback effects on gain, basic relationships for bandwidth and slew rate, and a discussion of pole-splitting frequency compensation. Sources of second-order bandlimiting in the amplifier are also identified and some approaches to speed and bandwidth improvement are developed. Brief sections are included on new JFET—bipolar circuitry and die area reduction techniques using transconductance reduction.

1.0 INTRODUCTION

The integrated circuit operational amplifier (IC op amp) is the most widely used of all linear circuits in production today. Over one hundred million of the devices will be sold in 1974 alone, and production costs are falling low enough so that op amps find applications in virtually every analog area. Despite this wide usage, however, many of the basic performance characteristics of the op amp are poorly understood.

It is the intent of this study to develop an understanding for op amp behavior in as direct and intuitive a manner as possible. This is done by using a variety of simplified circuit models which can be analyzed in some cases by inspection, or in others by writing just a few equations. These simplified models are generally developed from the single representative op amp configuration shown in *Figures 1* and *2*.

The rationale for starting with the particular circuit of *Figure 1* is based on the following: this circuit contains, in simplified form, all of the important elements of the most commonly used integrated op amps. It consists essentially of two voltage gain stages, an input differential amp and a common emitter second stage, followed by a class-AB output emitter follower which provides low impedance drive to the load. The two interstages are frequency compensated by a single small "pole-splitting" capacitor (see below) which is usually included on the op amp chip. In most respects this circuit is directly equivalent to the general purpose LM101 [1], μA 741 [2], and the newer dual and quad op amps [3], so the results of our study relate directly to these devices. Even for

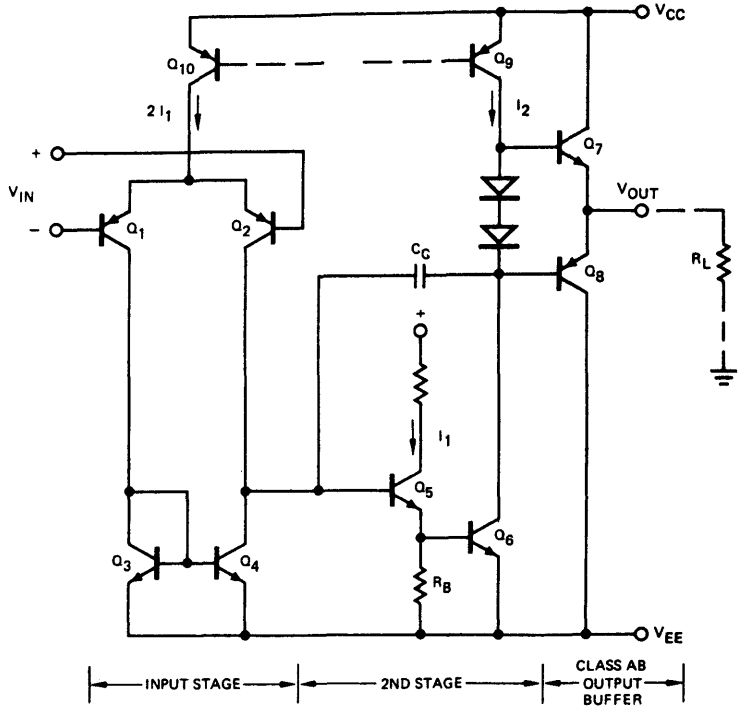

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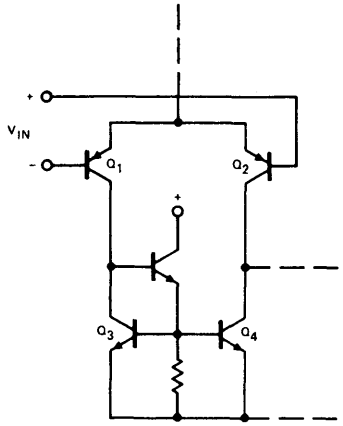
FIGURE 1. Basic two-stage IC op amp used for study. Minimal modifications used in actual IC are shown in *Figure 2*.



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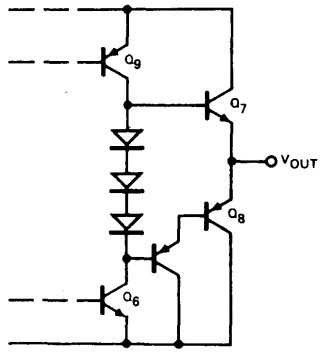
(a)



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(b)

FIGURE 2. (a) Modified current mirror used to reduce dc offset caused by base currents in Q3 and Q4 in *Figure 1*. (b) Darlington p-n-p output stage needed to minimize gain fall-off when sinking large output currents. This is needed to offset the rapid β drop which occurs in IC p-n-p's.

more exotic designs, such as wide-band amps using feedforward [4], [5], or the new FET input circuits [6], the basic analysis approaches still apply, and performance details can be accurately predicted. It has also been found that a good understanding of the limitations of the circuit in *Figure 1* provides a reasonable starting point from which higher performance amplifiers can be developed.

The study begins in Section 2, with an analysis of dc and low frequency gain. It is shown that the gain is typically limited by thermal feedback rather than electrical characteristics. A highly simplified thermal analysis is made, resulting in a gain equation containing only the maximum output current of the op amp and a thermal feedback constant.

The next three sections apply first-order models to the calculation of small-signal high frequency and large-signal slewing characteristics. Results obtained include an accurate equation for gain-bandwidth product, a general expression for slew rate, some important relationships between slew rate and bandwidth, and a solution for voltage follower behavior in a slewing mode. Due to the simplicity of the results in these sections, they are very useful to designers in the development of new amplifier circuits.

Section 6 applies more accurate models to the calculation of important second-order effects. An effort is made in this section to isolate all of the major contributors to bandlimiting in the modern amp.

In the final section, some techniques for reduction of op amp die size are considered. Transconductance reduction and layout techniques are discussed which lead to fabrication of an extremely compact op amp cell. An example yielding 8000 possible op amps per 3-in. wafer is given.

2.0 GAIN AT DC AND LOW FREQUENCIES

A. The Electronic Gain

The electronic voltage gain will first be calculated at dc using the circuit of *Figure 1*. This calculation becomes straightforward if we employ the simplified transistor model shown in *Figure 3(a)*. The resulting gain from *Figure 3(b)* is

$$A_V(0) = \frac{v_{out}}{v_{in}} \cong \frac{g_{m1}\beta_5\beta_6\beta_7 R_L}{1 + r_{i2}/r_{01}'} \quad (1)$$

where

$$r_{i2} \cong \beta_5(r_{e5} + \beta_6 r_{e6})$$

$$r_{01}' \cong r_{04}//r_{02}.$$

It has been assumed that

$$\beta_7 R_L < r_{06}//r_{09},\ g_{m1} = g_{m2},\ \beta_7 = \beta_8.$$

The numerical subscripts relate parameters to transistor Q numbers (i.e., r_{e5} is r_e of Q_5, β_6 is β_0 pf Q_6, etc.). It has also been assumed that the current mirror transistors Q_3 and Q_4 have α's of unity, and the usually small loading of R_B has been ignored. Despite the several assumptions made in obtaining this simple form for (1), its accuracy is quite adequate for our needs.

An examination of (1) confirms the way in which the amplifier operates: the input pair and current mirror convert the input voltage to a current $g_{m1}V_{in}$ which drives the base of the second stage. Transistors Q_5, Q_6, and Q_7 simply multiply this current by β^3 and supply it to the load R_L. The finite output resistance of the first stage causes some loss when compared with second stage input resistance, as indicated by the term $1/(1 + r_{i2}/r_{01}')$. A numerical example will help our perspective: for the LM101A, $I_1 \cong 10\ \mu A$, $I_2 \cong 300\ \mu A$, $\beta_5 = \beta_6 \cong 150$, and $\beta_7 \cong 50$. From (1) and dc voltage gain with $R_L = 2\ k\Omega$ is

$$A_V(0) \cong 625{,}000 \quad (2)$$

The number predicted by (2) agrees well with that measured on a discrete breadboard of the LM101A, but is much higher than that observed on the integrated circuit. The reason for this is explained in the next section.

B. Thermal Feedback Effects on Gain

The typical IC op amp is capable of delivering powers of 50–100 mW to a load. In the process of delivering this power, the output stage of the amp internally dissipates similar power levels, which causes the temperature of the IC chip to rise in proportion to the output dissipated power. The silicon chip and the package to which it is bonded are good thermal conductors, so the whole chip tends to rise to the same temperature as the output stage. Despite this, small

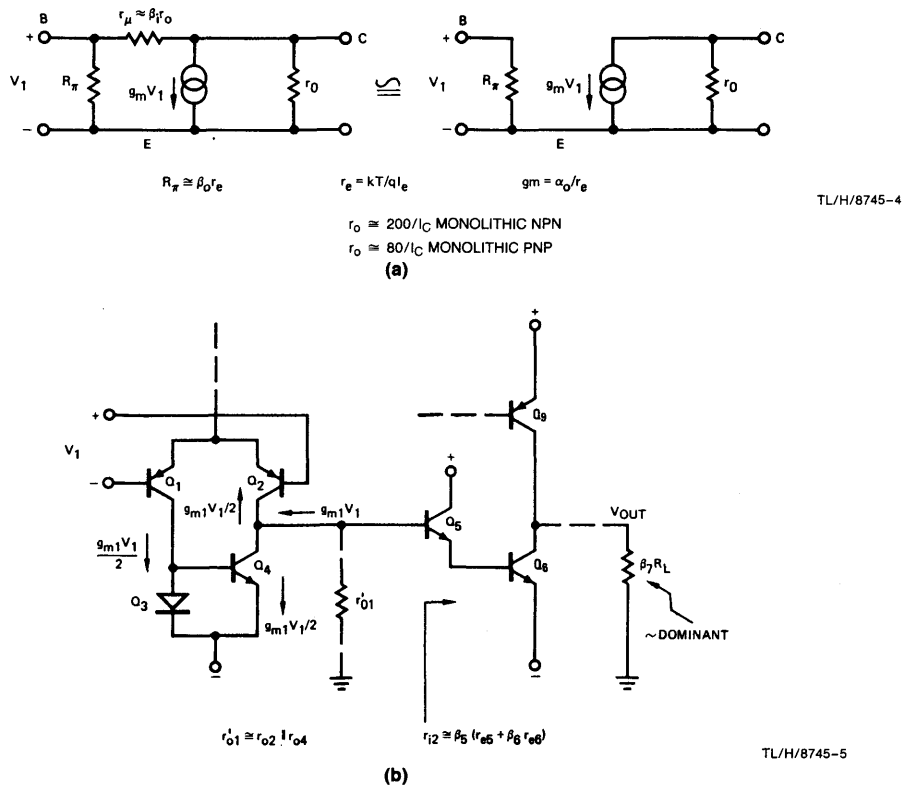

FIGURE 3. (a) Approximate π model for CE transistor at dc. Feedback element $r_\mu \cong \beta_4 r_o$ is ignored since this greatly simplifies hand calculations. The error caused is usually less than 10 percent because β_4, the intrinsic β under the emitter, is quite large. Base resistance r_x is also ignored for simplicity. (b) Circuit illustrating calculation of electronic gain for op amp of *Figure 1*. Consideration is given only to the fully loaded condition ($R_L \cong 2$ kΩ) where β_7 is falling (to about 50) due to high current density. Under this condition, the output resistance of Q6 and Q9 are nondominant.

temperature gradients from a few tenths to a few degrees centigrade develop across the chip with the output section being hotter than the rest. As illustrated in *Figure 4*, these temperature gradients appear across the input components of the op amp and induce an input voltage which is proportional to the output dissipated power.

To a first order, it can be assumed that the temperature difference $(T_2 - T_1)$ across a pair of matched and closely spaced components is given simply by

$$(T_2 - T_1) \cong \pm K_T P_d \quad °C \tag{3}$$

where

P_d power dissipated in the output circuit,

K_T a constant with dimensions of °C/W.

The plus/minus sign is needed because the direction of the thermal gradient is unknown. In fact, the sign may reverse polarity during the output swing as the dominant source of heat shifts from one transistor to another. If the dominant input components consist of the differential transistor pair of *Figure 4*, the thermally induced input voltage V_{int} can be calculated as

$$V_{int} \cong \pm K_T P_d (2 \times 10^{-3})$$
$$\cong \pm \gamma_T P_d \tag{4}$$

where $\gamma_T = K_T(2 \times 10^{-3})$ V/W, since the transistor emitter-base drops change about -2 mV/°C.

For a thermally well designed IC op amp, in which the power output devices are made to approximate either a point or a line source and the input components are placed on the resulting isothermal lines (see below and *Figure 8*), typical values measured for K_T are

$$K_T \approx 0.3°C/W \tag{5}$$

in a TO-5 package.

The dissipated power in the class-AB output stage P_d is written by inspection of *Figure 4*:

$$P_d = \frac{V_0 V_s - V_0^2}{R_L} \tag{6}$$

where

$$V_s = +V_{cc} \quad \text{when } V_0 > 0$$
$$V_s = -V_{ee} \quad \text{when } V_0 < 0.$$

A plot of (6) is *Figure 5* resembles the well-known class-AB dissipation characteristics, with zero dissipation occurring

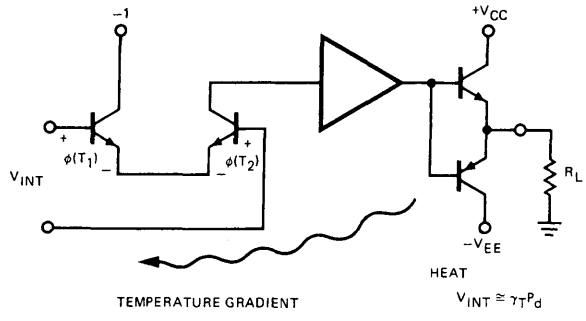

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FIGURE 4. Simple model illustrating thermal feedback in an IC op amp having a single dominant source of self-heat, the output stage. The constant $\gamma_T \cong 0.6$ mV/W and P_d is power dissipated in the output. For simplicity, we ignore input drift due to uniform heating of the package. This effect can be significant if the input stage drift is not low, see [7].

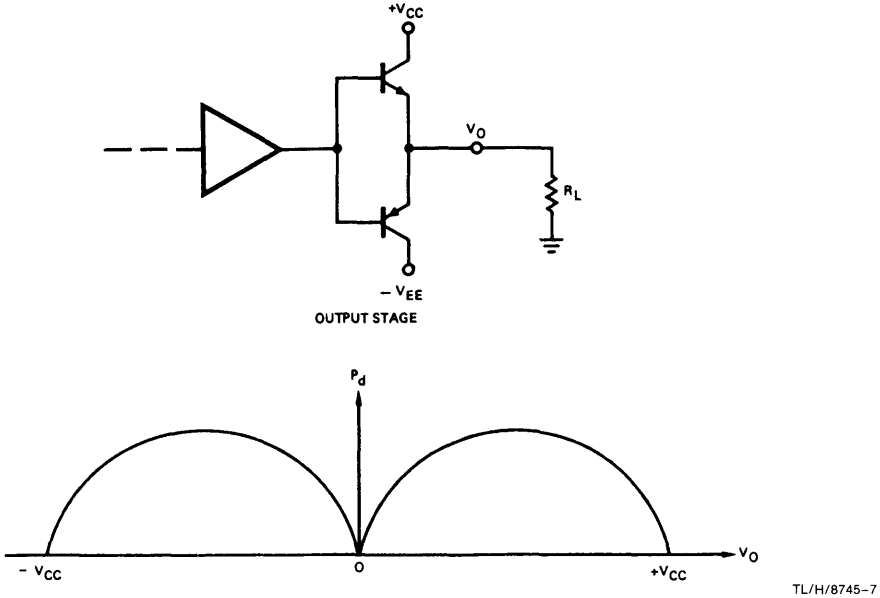

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FIGURE 5. Simple class-B output stage and plot of power dissipated in the stage, P_d, assuming device can swing to the power supplies. Equation (6) gives an expression for the plot.

for $V_0 = 0, +V_{cc}, -V_{ee}$. Dissipation peaks occur for $V_0 = +V_{cc}/2$ and $-V_{ee}/2$. Note also from (4) that the thermally induced input voltage V_{int} has this same double-humped shape since it is just equal to a constant times P_d at dc.

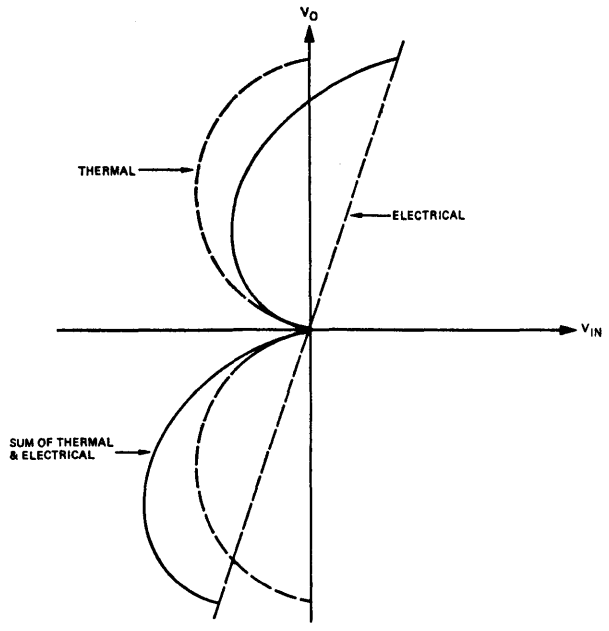
Now examine *Figures 6(a)* and *(b)* which are curves of open-loop V_0 versus V_{in} for the IC op amp. Note first that the overall curve can be visualized to be made up of two components: a) a normal straight line electrical gain curve of the sort expected from (1) and b) a double-humped curve similar to that of *Figure 5.* Further, note that the gain characteristic has either positive or negative slope depending on the value of output voltage. This means that the thermal feedback causes the open-loop gain of the feedback amplifier to change phase by 180°, apparently causing negative feedback to become positive feedback. If this is really true, the question arises: which input should be used as the inverting one for feedback? Further, is there any way to close the amplifier and be sure it will not find an unstable operating point and latch to one of the power supplies?

The answers to these questions can be found by studying a simple model of the op amp under closed-loop conditions, including the effects of thermal coupling. As shown in *Figure 7,* the thermal coupling can be visualized as just an additional feedback path which acts in parallel with the normal electrical feedback. Noting that the electrical form of the thermal feedback factor is [see (4) and (6)]

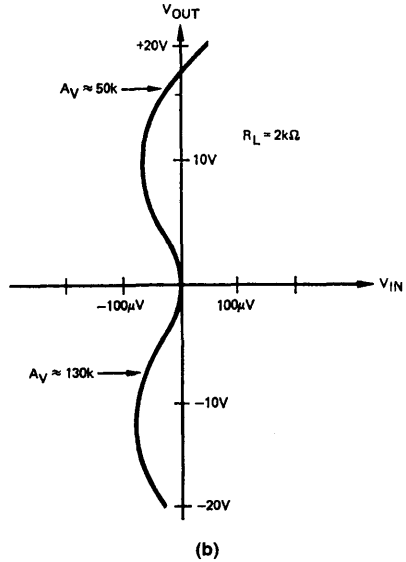
$$\beta_T = \frac{\partial V_{int}}{\partial V_0} = \pm \frac{\gamma_T}{R_L}(V_s - 2V_0). \qquad (7)$$

The closed-loop gain, including thermal feedback is

$$A_V(0) = \frac{\mu}{1 + \mu(\beta_e \pm \beta_T)} \qquad (8)$$



(a)



(b)

FIGURE 6. (a) Idealized dc transfer curve for an IC op amp showing its electrical and thermal components. (b) Experimental open-loop transfer curve for a representative op amp (LM101).

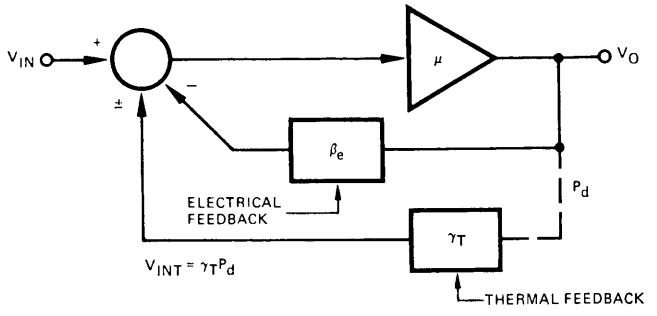


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FIGURE 7. Diagram used to calculate closed-loop gain with thermal feedback.

where μ is the open-loop gain in the absence of thermal feedback [(1)] and β_e is the applied electrical feedback as in *Figure 7.* Inspection of (8) confirms that as long as there is sufficient electrical feedback to swamp the thermal feedback (i.e., $\beta_e > \beta_T$), the amplifier will behave as a normal closed-loop device with characteristics determined principally by the electrical feedback (i.e., $A_V(0) \cong 1/\beta_e$). On the other hand, if β_e is small or nonexistant, the thermal term in (8) may dominate, giving an apparent open-loop gain characteristic determined by the thermal feedback factor β_T. Letting $\beta_e = 0$ and combining (7) and (8), $A_V(0)$ becomes

$$A_V(0) = \frac{\mu}{1 \pm \frac{\mu\gamma_T}{R_L}(V_S - 2V_0)}. \qquad (9)$$

Recalling from (6) that V_0 ranges between 0 and V_S, we note that the incremental thermal feedback is greatest when $V_0 = 0$ or V_S, and it is at these points that the thermally limited gain is smallest. To use the amplifier in a predictable manner, one must always apply enough electrical feedback to reduce the gain below this minimum thermal gain. Thus, a *maximum usable gain* can be defined as that approximately equal to the value of (9) with $V_0 = 0$ or V_S which is

$$A_V(0)|_{max} \cong \frac{R_L}{\gamma_T V_S} \qquad (10)$$

or

$$A_V(0)|_{max} \cong \frac{1}{\gamma_T I_{max}}. \qquad (11)$$

It was assumed in (10) and (11) that thermal feedback dominates over the open-loop electrical gain, μ. Finally, in (11) a maximum current was defined $I_{max} = V_S/R_L$ as the maximum current which would flow if the amplifier output could swing all the way to the supplies.

Equation (11) is a strikingly simple and quite general result which can be used to predict the expected maximum usable gain for an amplifier if we know only the maximum output current and the thermal feedback constant γ_T.

Recall that typically $K_T \cong 0.3°C/W$ and $\gamma_T = (2 \times 10^{-3})$ $K_T \cong 0.6$ mV/W. Consider, as an example, the standard IC op amp operating with power supplies of $V_S = \pm 15V$ and a minimum load of 2 kΩ, which gives $I_{max} = 15V/2\,k\Omega = 7.5$ mA. Then, from (11), the maximum thermally limited gain is about:

$$A_V(0)|_{max} \cong 1/(0.6 \times 10^{-3})(7.5 \times 10^{-3}) \cong 220{,}000. \qquad (12)$$

Comparing (2) and (12), it is apparent that the thermal characteristics dominate over the electrical ones if the minimum load resistor is used. For loads of 6 kΩ or more, the electrical characteristics should begin to dominate if thermal feedback from sources other than the output stage is negligible. It should be noted also that, in some high speed, high drain op amps, thermal feedback from the second stage dominates when there is no load.

As a second example, consider the so-called "power op amp" or high gain audio amp which suffers from the same thermal limitations just discussed. For a device which can deliver 1W into a 16Ω load, the peak output current and voltage are 350 mA and 5.7V. Typically, a supply voltage of about 16V is needed to allow for the swing loss in the IC output stage. I_{max} is then 8V/16Ω or 0.5A. If the device is in a TO-5 package γ_T is approximately 0.6 mV/W, so from (11) the maximum usable dc gain is

$$A_V(0)|_{max} \cong \frac{1}{(0.6 \times 10^{-3})(0.5)} \cong 3300. \qquad (13)$$

This is quite low compared with electrical gains of, say, 100,000 which are easily obtainable. The situation can be improved considerably by using a large die to separate the power devices from the inputs and carefully placing the inputs on constant temperature (isothermal) lines as illustrated in *Figure 8.* If one also uses a power package with a heavy copper base, γ_T's as low as 50 μV/W have been observed. For example, a well-designed 5W amplifier driving an 8Ω load and using a 24V supply, would have a maximum gain of 13,000 in such a power package.

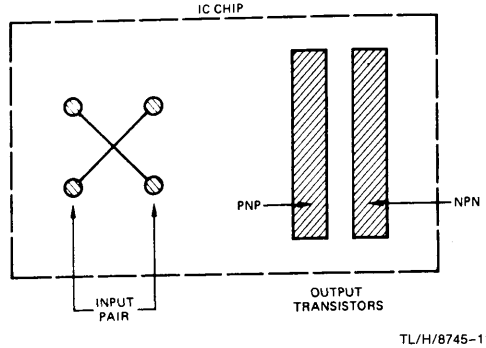

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FIGURE 8. One type layout in which a quad of input transistors is cross connected to reduce effect of nonuniform thermal gradients. The output transistors use distributed stripe geometrics to generate predictable isothermal lines.

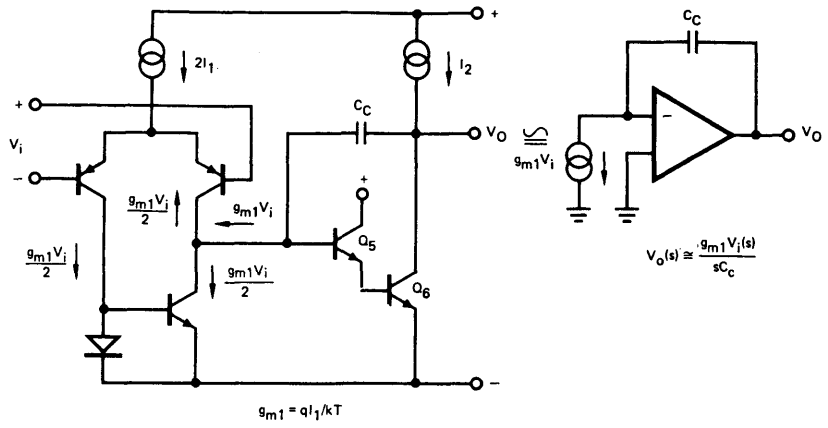

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FIGURE 9. First-order model of op amp used to calculate small signal high frequency gain. At frequencies of interest the input impedance of the second stage becomes low compared to first stage output impedance due to C_C feedback. Because of this, first stage output impedance can be assumed infinite, with no loss in accuracy.

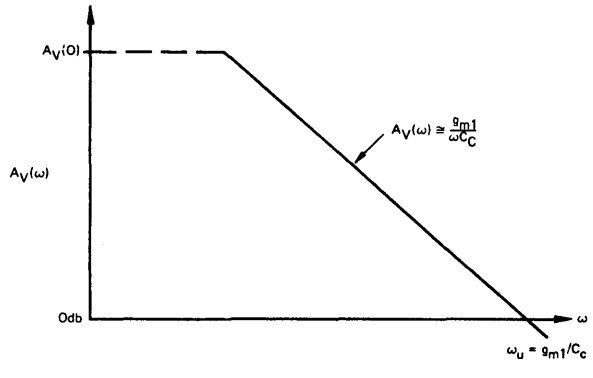

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FIGURE 10. Plot of open-loop gain calculated from model in *Figure 9*. The dc and LF gain are given by (10), or (11) if thermal feedback dominates.

As a final comment, it should be pointed out that the most commonly observed effect of thermal feedback in high gain circuits is low frequency distortion due to the nonlinear transfer characteristic. Differential thermal coupling typically falls off at an initial rate of 6 dB/octave starting around 100–200 Hz, so higher frequencies are uneffected.

3.0 SMALL-SIGNAL FREQUENCY RESPONSE

At higher frequencies where thermal effects can be ignored, the behavior of the op amp is dependent on purely electronic phenomena. Most of the important small and large signal performance characteristics of the classical IC op amp can be accurately predicted from very simple first-order models for the amplifier in *Figure 1* (8). The small-signal model that is used assumes that the input differential amplifier and current mirror can be replaced by a frequency independent voltage controlled current source, see *Figure 9*. The second stage consisting essentially of transistors Q_5 and Q_6, and the current source load, is modeled as an ideal frequency independent amplifier block with a feedback or "integrating capacitor" identical to the compensation capacitor, c_c. The output stage is assumed to have unity voltage gain and is ignored in our calculations. From *Figure 9,* the high frequency gain is calculated by inspection:

$$A_V(\omega) = \left|\frac{V_0}{V_i}(s)\right| = \left|\frac{g_{m1}}{sC_c}\right| = \frac{g_{m1}}{\omega C_c} \qquad (14)$$

where dc and low frequency behavior have not been included since this was evaluated in the last section. *Figure 10* is a plot of the gain magnitude as predicted by (14). From this figure it is a simple matter to calculate the open-loop unity gain frequency ω_u, which is also the gain-bandwidth product for the op amp under closed-loop conditions:

$$\omega_u = \frac{g_{m1}}{C_c}. \qquad (15)$$

In a practical amplifier, ω_u is set to a low enough frequency (by choosing a large C_C) so that negligible excess phase over the 90° due to C_C has built up. There are numerous contributors to excess phase including low f_t p-n-p's, stray capacitances, nondominant second stage poles, etc.

These are discussed in more detail in a later section, but for now suffice it to say that, in the simple IC op amp, $\omega_u/2\pi$ is limited to about 1 MHz. As a simple test of (15), the LM101 or the μA741 has a first stage bias current I_1 of 10 μA per side, and a compensation capacitor for unity gain operation, C_C, of 30 pF. These amplifiers each have a first stage g_m which is half that of the simple differential amplifer in *Figure 1* so $g_{m1} = qI_1/2kT$. Equation (15) then predicts a unity gain corner of

$$f_u = \frac{\omega_u}{2\pi} = \frac{g_{m1}}{2\pi C_C} = \frac{(0.192 \times 10^{-3})}{2\pi(30 \times 10^{-12})} = 1.02\ \text{MHz} \quad (16)$$

which agrees closely with the measured values.

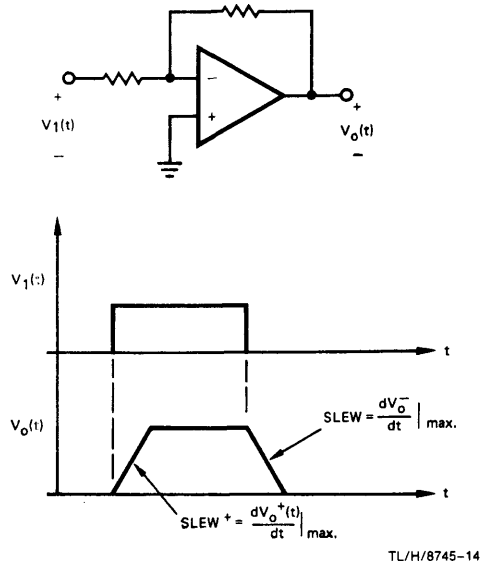

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FIGURE 11. Large signal "slewing" response observed if the input is overdriven.

4.0 SLEW RATE AND SOME SPECIAL LIMITS

A. A General Limit on Slew Rate

If an op amp is overdriven by a large-signal pulse or square wave having a fast enough rise time, the output does not follow the input immediately. Instead, it ramps or "slews" at some limiting rate determined by internal currents and capacitances, as illustrated in *Figure 11.* The magnitude of input voltage required to make the amplifier reach its maximum slew rate varies, depending on the type of input stage used. For an op amp with a simple input differential amp, an input of about 60 mV will cause the output to slew at 90 percent of its maximum rate, while a μA741, which has half the input g_m, requires 120 mV. High speed amplifiers such as the LM118 or a FET-input circuit require much greater overdrive, with 1–3V being common. The reasons for these overdrive requirements will become clear below.

An adequate model to calculate slew limits for the representative op amp in the inverting mode is shown in *Figure 12,* where the only important assumption made is that $I_2 \geq 2I_1$ in *Figure 1.* This condition always holds in a well-designed op amp. (If one lets I_2 be less than $2I_1$, the slew is limited by I_2 rather than I_1, which results in lower speed than is otherwise possible.) *Figure 12* requires some modification for noninverting operation, and we will study this later.

The limiting slew rate is now calculated from *Fig. 12.* Letting the input voltage be large enough to fully switch the input differential amp, we see that all of the first stage tail current $2I_1$ is simply diverted into the integrator consisting of A and C_C. The resulting slew rate is then:

$$\text{slew rate} = \left.\frac{dv_0}{dt}\right|_{max} = \frac{i_c(t)}{C_C}. \quad (17)$$

Noting that $i_c(t)$ is a constant $2I_1$, this becomes

$$\left.\frac{dv_0}{dt}\right|_{max} = \frac{2I_1}{C_C}. \quad (18)$$

As a check of this result, recall that the μA741 has I_1 = 10 μA and C_1 = 30 pF, so we calculate:

$$\left.\frac{dv_0}{dt}\right|_{max} = \frac{2 \times 10^{-5}}{30 \times 10^{-12}} = 0.67\frac{V}{\mu s} \quad (19)$$

which agrees with measured values.

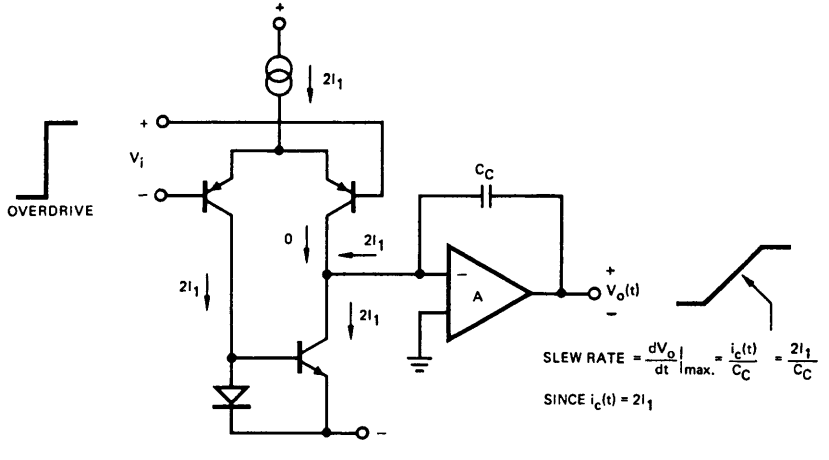

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FIGURE 12. Model used to calculate slew rate for the amp of *Figure 1* in the inverting mode. For simplicity, all transistor α's are assumed equal to unity, although results are essentially independent of α. An identical slew rate can be calculated for a negative-going output, obtained if the applied input polarity is reversed.

The large and small signal behavior of the op amp can be usefully related by combining (15) for ω_u with (18). The slew rate becomes

$$\left.\frac{dv_0}{dt}\right|_{max} = \frac{2\omega_u I_1}{g_{m1}}. \quad (20)$$

Equation (20) is a general and very useful relationship. It shows that, for a given unity-gain frequency, ω_u, the slew rate is determined entirely by just the ratio of first stage operating current to first stage transconductance, I_1/g_{m1}. Recall that ω_u is set at the point where excess phase begins to build up, and this point is determined largely by technology rather than circuit limitations. Thus, the only effective means available to the circuit designer for increasing op amp slew rate is to *decrease* the ratio of first stage transconductance to operating current, $g_{m1}/_1$.

B. Slew Limiting for Simple Bipolar Input Stage

The significance of (20) is best seen by considering the specific case of a simple differential bipolar input as in *Figure 1.* For this circuit, the first stage transconductance (for $\alpha_1 = 1$) is[1]

$$g_{m1} = qI_1/kT \quad (21)$$

so that

$$\frac{g_{m1}}{I_1} = q/kT. \quad (22)$$

Using this in (20), the maximum bipolar slew rate is

$$\left.\frac{dv_0}{dt}\right|_{max} = 2\omega_u\frac{kT}{q}. \quad (23)$$

This provides us with the general (and somewhat dismal) conclusion that slew rate in an op amp with a simple bipolar input stage is dependent only upon the unity gain corner and fundamental constants. Slew rate can be increased only by incerasing the unity gain corner, which we have noted is generally difficult to do. As a demonstration of the severity of this limit, imagine an op amp using highly advanced technology and clever design, which might have a stable unity gain frequency of 100 MHz. Equation (23) predicts that the slew rate for this advanced device is only

$$\left.\frac{dv_0}{dt}\right|_{max} = 33\frac{V}{\mu s} \quad (24)$$

which is good, but hardly impressive when compared with the difficulty of building a 100 MHz op amp.[2] But, there are some ways to get around this limit as we shall see shortly.

C. Power Bandwidth

Our intuition regarding slew rate will be enhanced somewhat if we relate it to a term called "power bandwidth". Power bandwidth is defined as the maximum frequency at which full output swing (usually 10V peak) can be obtained without distortion. For a sinusoidal output voltage $v_0(t) = V_p \sin\omega t$, the rate of change of output, or slew rate, required to reproduce the output is

$$\frac{dv_0}{dt} = \omega V_p \cos\omega t. \quad (25)$$

This has a maximum when $\cos\omega t = 1$ giving

$$\left.\frac{dv_0}{dt}\right|_{max} = \omega V_p, \quad (26)$$

so the highest frequency that can be reproduced without slew limiting, ω_{max} (power bandwidth) is

$$\omega_{max} = \frac{1}{V_p}\left.\frac{dv_0}{dt}\right|_{max}. \quad (27)$$

Thus, power bandwidth and slew rate are directly related by the inverse of the peak of the sine wave V_p. *Figure 13* shows the severe distortion of the output sine wave which results if one attempts to amplify a sine wave which results if one attempts to amplify a sine wave of frequency $\omega > \omega_{max}$.

[1]Note that (21) applies only to the simple differential input stage of *Figure 12.* For compound input stages as in the LM101 or μA741, g_{m1} is half that in (21), and the slew rate in (23) is doubled.

[2] We assume in all of these calculations that C_c is made large enough so that the amplifier has less than 180° phase lag at ω_u, thus making the amplifier stable for unity closed-loop gain. For higher gains one can of course reduce C_c (if the IC allows external compensation) and increase the slew rate according to (18).

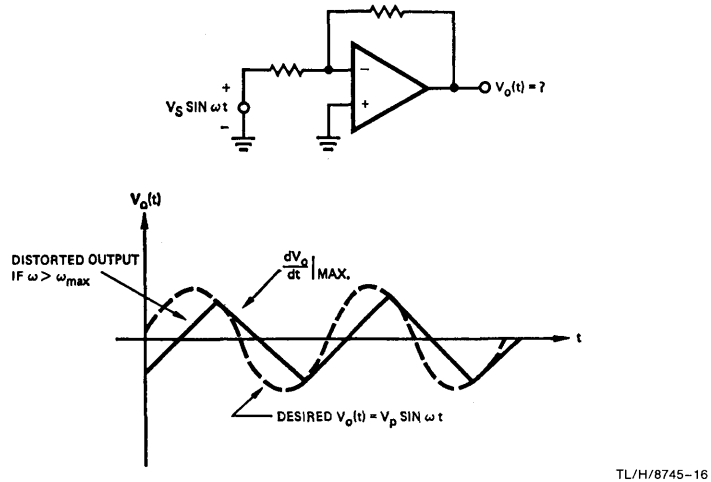

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FIGURE 13. Slew limiting effects on output sinewave that occur if frequency is greater than power bandwidth, ω_{max}. The onset of slew limiting occurs very suddenly as ω reaches ω_{max}. No distortion occurs below ω_{max}, while almost complete triangularization occurs at frequencies just slightly above ω_{max}.

Some numbers illustrate typical op amp limits. For a μA741 or LM101 having a maximum slew rate of 0.67V/μs, (27) gives a maximum frequency for an undistorted 10V peak output of

$$f_{max} = \frac{\omega_{max}}{2\pi} = 10.7\ \text{kHz}, \tag{28}$$

which is a quite modest frequency considering the much higher frequency small signal capabilities of these devices. Even the highly advanced 100 MHz amplifier considered above has a 10V power bandwidth of only 0.5 MHz, so it is apparent that a need exists for finding ways to improve slew rate.

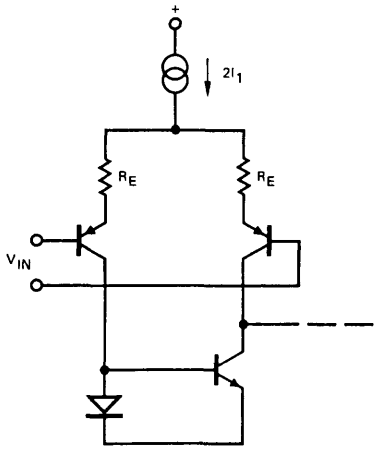

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FIGURE 14. Resistive degeneration used to provide slew rate enhancement according to (29).

D. Techniques for Increasing Slew Rate

1) Resistive Enhancement of the Bipolar Stage: Equation (20) indicates that slew rate can be improved if we reduce first stage g_{m1}/I_1. One of the most effective ways of doing this is shown in *Figure 14,* where simple resistive emitter degeneration has been added to the input differential amplifier (8). With this change, the g_{m1}/I_1 drops to

$$\frac{g_{m1}}{I_1} = \frac{38.5}{1 + T_E I_1/26\ \text{mV}} \tag{29}$$

at 25°C

The quantity g_{m1}/I_1 is seen to decrease rapidly with added R_E as soon as the voltage drop across R_E exceeds 26 mV. The LM118 is a good example of a bipolar amplifier which uses emitter degeneration to enhance slew rate [4]. This device uses emitter resistors to produce $R_E I_1$ = 500 mV, and has a unity gain corner of 16 MHz. Equations (20) and (29) then predict a maximum inverting slew rate of

$$\left.\frac{dv_0}{dt}\right|_{max} = 2\omega_u \frac{I_1}{g_{m1}} = \omega_u = 100\frac{V}{\mu s} \tag{30}$$

which is a twenty-fold improvement over a similar amplifier without emitter resistors.

A penalty is paid in using resistive slew enhancement, however. The two added emitter resistors must match extremely well or they add voltage offset and drift to the input. In the LM118, for example, the added emitter R's have values of 2.0 kΩ each and these contribute an input offset of 1 mV for each 4Ω (0.2 percent) of mismatch. The thermal noise of the resistors also unavoidably degrades noise performance.

2) Slew Rate in the FET Input Op Amp: The FET (JFET or MOSFET) has a considerably lower transconductance than a bipolar device operating at the same current. While this is normally considered a drawback of the FET, we note that this "poor" behavior is in fact highly desirable in applications to fast amplifiers. To illustrate, the drain current for a JFET in the "current saturation" region can be approximated by

$$I_D \cong I_{DSS}(V_{GS}/V_T - 1)^2 \tag{31}$$

where

I_{DSS} the drain current for $V_{GS} = 0$,

V_{GS} the gate source voltage having positive polarity for forward gate-diode bias,

V_T the threshold voltage having negative polarity for JFET's.

The small-signal transconductance is obtained from (31) as $g_m = \partial I_D/\partial V_G$. Dividing by I_D and simplifying, the ratio g_m/I_D for a JFET is

$$\frac{g_M}{I_D} \cong \frac{2}{(V_{GS} - V_T)} = \frac{2}{-V_T}\left[\frac{I_{DSS}}{I_D}\right]^{1/2}. \tag{32}$$

Maximum amplifier slew rate occurs for minimum g_m/I_D and, from (32), this occurs when I_D or V_{GS} is maximum. Normally it is impractical to forward bias the gate junction so a practical minimum occurs for (32) when $V_{GS} \cong 0V$ and $I_D \cong I_{DSS}$. Then

$$\left.\frac{g_m}{I_D}\right|_{min} \cong -2\frac{2}{V_T}. \tag{33}$$

Comparing (33) with the analogous bipolar expression, (22), we find from (20) that the JFET slew rate is greater than bipolar by the factor

$$\frac{\text{JFET slew}}{\text{bipolar slew}} \approx \frac{-V_T 2\omega_{uf}}{2kT/q\omega_{ub}} \tag{34}$$

where ω_{uf} and ω_{ub} are unity-gain bandwidths for JFET and bipolar amps, respectively. Typical JFET thresholds are around 2V ($V_T = -2V$), so for equal bandwidths (34) tells us that a JFET-input op amp is about forty times faster than a simple bipolar input. Further, if JFET's are properly substituted for the slow p-n-p's in a monolithic design, bandwidth improvements by at least a factor of ten are obtainable. JFET-input op amps, therefore, offer slew rate improvements by better than two orders of magnitude when compared with the conventional IC op amp. (Similar improvements are possible with MOSFET-input amplifiers.) This characteristic, coupled with picoamp input currents and reasonable offset and drift, make the JFET-input op amp a very desirable alternative to conventional bipolar designs.

As an example, *Figure 15,* illustrates one design for an op amp employing compatible p-channel JFET's on the same chip with the normal bipolar components. This circuit exhibits a unity gain corner of 10 MHz, a 33 V/μs slew rate, an input current of 10 pA and an offset voltage and drift of 3 mV amd 3 μV/°C [6]. Bandwidth and slew rate are thus improved over simple IC bipolar by factors of 10 and 100, respectively. At the same time input currents are smaller by about 10^3, and offset voltages and drifts are comparable to or better than slew enhanced bipolar circuits.

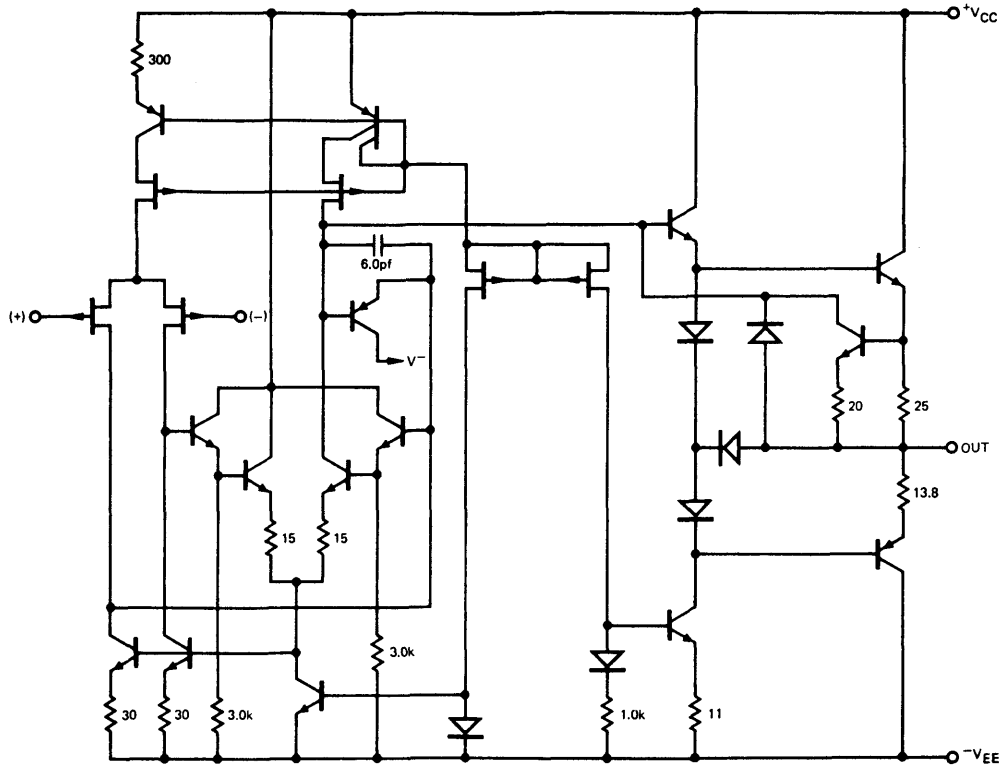

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FIGURE 15. Monolithic operational amplifier employing compatible p-channel JFET's on the same chip with normal bipolar components.

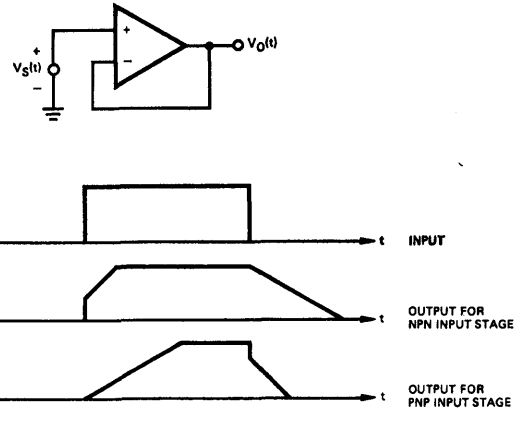

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FIGURE 16. Large signal response of the voltage follower. For an op amp with simple n-p-n input stage we get the waveform $v_{ON}(t)$, which exhibits a step slew "enhancement" on the positive going output, and a slew "degradation" on the negative going output. For a p-n-p input stage, these effects are reversed as shown by $v_{op}(t)$.

5.0 SECOND-ORDER EFFECTS: VOLTAGE FOLLOWER SLEW BEHAVIOR

If the op amp is operated in the noninverting mode and driven by a large fast rising input, the ouput exhibits the characteristic waveform in *Figure 16.* As shown, this waveform does not have the simple symmetrical slew characteristic of the inverter. In one direction, the output has a fast step (slew "enhancement") followed by a "normal" inverter slewing response. In the other direction, it suffers a slew "degradation" or reduced slope when compared with the inverter slewing response.

We will first study slew degradation in the voltage follower connection, since this represents a worst case slewing condition for the op amp. A model which adequately represents the follower under large-signal conditions can be obtained from that in *Figure 12* by simply tying the output to the inverting input, and including a capacitor C_S to account for the presence of any capacitance at the output of the first stage (tail) current source, see *Figure 17.* This "input tail" capacitance is important in the voltage follower because the input stage undergoes rapid large-signal excursions in this connection, and the charging currents in C_S can be quite large.

Circuit behavior can be understood by analyzing *Figure 17* as follows. The large-signal input step causes Q_1 to turn OFF, leaving Q_2 to operate as an emitter follower with its emitter tracking the variational output voltage, $v_0(t)$. It is seen that $v_0(t)$ is essentially the voltage appearing across both C_S and C_C so we can write

$$\frac{dv_0}{dt} \cong \frac{i_c}{C_c} \cong \frac{i_s}{C_s}. \tag{35}$$

Noting that $i_c \cong 2I_1 - i_s$ (unity α's assumed), (35) can be solved for i_s:

$$i_s \cong \frac{2I_1}{1 + C_c/C_s} \tag{36}$$

which is seen to be constant with time. The degraded voltage follower slew rate is then obtained by substituting (36) into (35):

$$\left.\frac{dv_0}{dt}\right|_{degr} \cong \frac{i_s}{C_s} \cong \frac{2I_1}{C_c + C_s}. \tag{37}$$

Comparing (37) with the slew rate for the inverter, (18), it is seen that the slew rate is reduced by the simple factor $1/(1 + C_s/C_c)$. As long as the input tail capacitance C_s is small compared with the compensation amplifiers where C_c is small, degradation become quite noticeable, and one is encouraged to develop circuits with small C_s.

As an example, consider the relatively fast LM118 which has $C_c \cong 5$ pF, $C_8 \cong 2$ pF, $2I_1 = 500$ μA. The calcualted inverter slew rate is $2I_1/C_c \cong 100V/\mu s$, and the degraded voltage follower slew rate is found to be $2I_1/(C_c + C_8) \cong 70V/\mu s$. The slew degradation is seen to be about 30 percent, which is very significant. By contrast a μA741 has $C_c \cong 30$ pF and $C_8 \cong 4$ pF which results in a degradation of less than 12 percent.

The slew "enhanced waveform can be similarly predicted from a simplified model. By reversing the polarity of the input and initally assuming a finite slope on the input step, the enhanced follower is analyzed, as shown in *Figure 18.* Noting that Q_1 is assumed to be turned ON by the step input and Q_2 is OFF, the output voltage becomes

$$v_0(t) \cong -\frac{1}{C_c}\int_0^t [2I_1 + i_s(t)]\, dt. \tag{38}$$

The voltage at the emitter of Q_1 is essentially the same as the input voltage, $v_i(t)$, so the current in the "tail" capacitance C_8 is

$$i_s(t) \cong C_8 \frac{dv_i}{dt} \cong \frac{C_8 V_{ip}}{t_1} \qquad 0 < t < t_1. \tag{39}$$

Combining (38) and (39), $v_0(t)$ is

$$-v_0(t) \cong \frac{1}{C_c}\int_0^t 2I_1\, dt + \frac{1}{C_c}\int_0^{t_1} \frac{C_8 V_{ip}}{t_1}\, dt \tag{40}$$

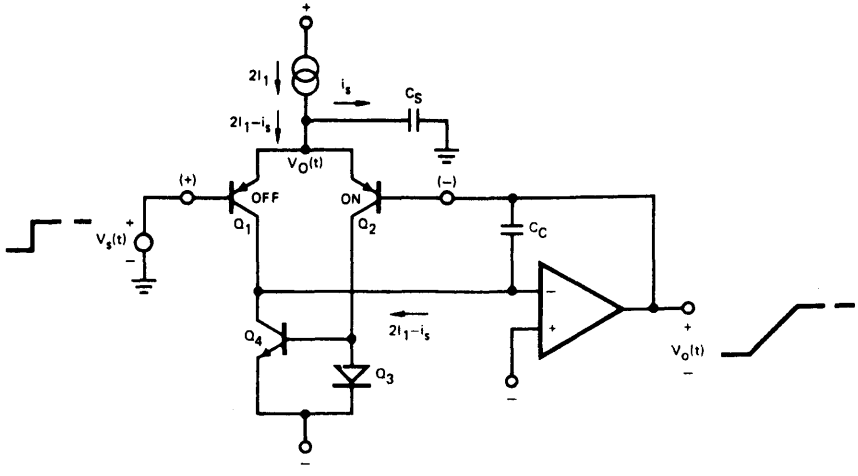

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FIGURE 17. Circuit used for calculation of slew "degradation" in the voltage follower. The degradation is caused by the capacitor C_8, which robs current from the tail, $2I_1$, thereby preventing the full $2I_1$ from slewing C_c.

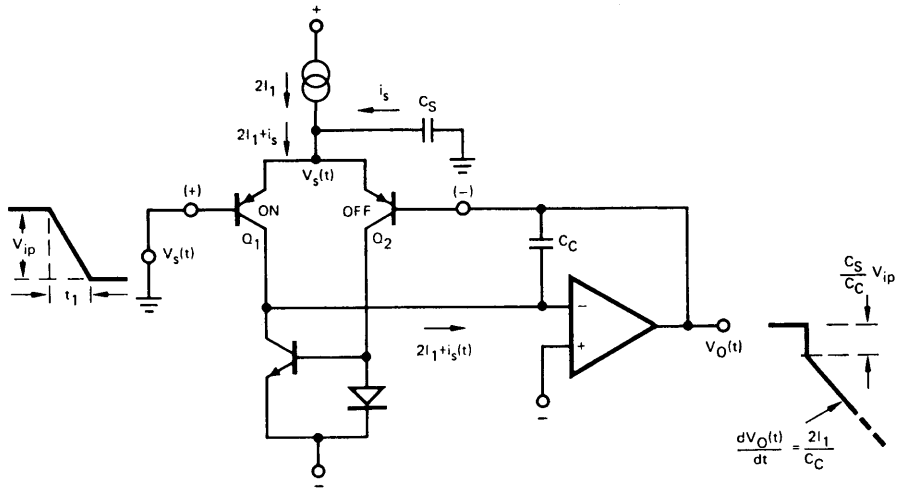

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FIGURE 18. *Circuit used for calculation of slew "enhancement" in the voltage follower. The fast falling input casues a step output followed by a normal slew response as shown.*

or

$$-v_0(t) \cong \frac{C_8}{C_c} V_{ip} + \frac{2I_1 t}{C_c}. \qquad (41)$$

Equation (41) tells us that the output has an initial negative step which is the fraction C_8/C_c of the input voltage. This is followed by a normal slewing response, in which the slew rate is identical to that of the inverter, see (18). This response is illustrated in *Figure 18.*

6. LIMITATIONS ON BANDWIDTH

In earilier sections, all bandlimiting effects were ignored except that of the compensation capacitor, C_c. The unity-gain frequency was set at a point sufficiently low so that negligible excess phase (over the 90° from the dominant pole) due to second-order (high frequency) poles had built up. In this section the major second-order poles which contribute to bandlimiting in the op amp are identified.

A. The Input Stage: p-n-p's, the Mirror Pole, and the Tail Pole

For many years it was popular to identify the lateral p-n-p's (which have f_t's $\cong$ 3 MHz) as the single dominant source of bandlimiting in the IC op amp. It is quite true that the p-n-p's do contribute significant excess phase to the amplifier, but it is not true that they are the sole contributor to excess phase [9]. In the input stage, alone, there is at least one other important pole, as illustrated in *Figure 19(a).* For the simple differential input stage driving a differential-to-single ended converter ("mirror" circuit), it is seen that the inverting signal (which is the feedback signal) follows two paths, one of which passes through the capacitance C_8, and the other through C_m. These capacitances combine with the dynamic resistances at their nodes to form poles designated the mirror pole at

$$p_m \cong \frac{I_1}{C_m kT/q}, \qquad (42)$$

and the tail pole at

$$p_t \cong \frac{2I_1}{C_8 kT/q}. \qquad (43)$$

It can be seen that if one attempts to operate the first stage at too low a current, these poles will bandlimit the amplifier. If, for example, we choose $I_1 = 1\ \mu A$, and assume $C_m \cong$ 7 pF (consisting of 4 pF isolation capacitance and 3 pF emitter transition capacitance) and $C_8 \cong 4$ pF,[3] $p_m/2\pi \cong$ 0.9 MHz and $p_t/2\pi \cong 3$ MHz either of which would seriously degrade the phase margin of a 1 MHz amplifier.

If a design is chosen in which either the tail pole or the mirror pole is absent (or unimportant), the remaining pole rolls off only half the signal, so the overall response contains a pole-zero pair separated by one octave. Such a pair generally has a small effect on amplifier response unless it occurs near ω_u, where it can degrade phase margin by as much as 20°.

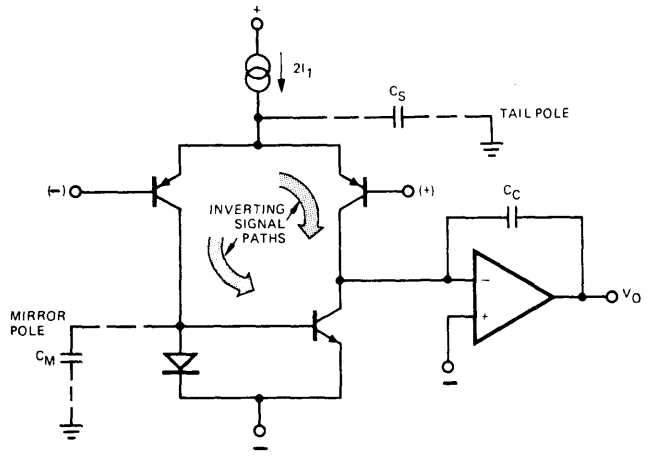
It is interesting to note that the compound input stage of the classical LM101 and μA741) has a distinct advantage over the simple differential stage, as seen in *Figure 19(b).* This circuit is noninverting across each half, thus it provides a path in which half the feedback signal bypasses both the mirror and tail poles.

B. The Second Stage: Pole Splitting

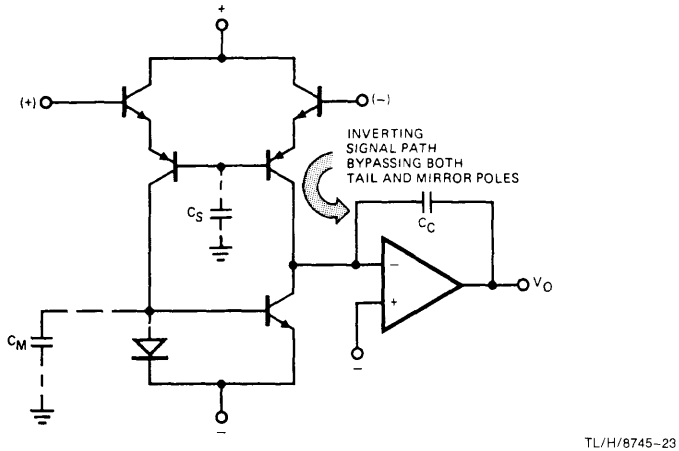
The assumption was made in Section 3 that the second stage behaved as an ideal integrator having a single dominant pole response. In practice, one must take care in designing the second stage or second-order poles can cause significant deviation from the expected response. Considerable insight into the basic way in which the second stage operates can be obtained by performing a small-signal analysis on a simplified version of the circuit as shown in *Figure 20* [10]. A straightforward two-node analysis of *Figure 20(c)* produces the following expression for v_{out}.

$$\frac{v_{out}}{i_s} = -g_m R_1 R_2 (1 - sC_p/g_m) \div$$
$$(1 + s[R_1 (C_1 + C_p) + R_2 (C_2 + C_p) + g_m R_1 R_2 C_p]$$
$$+ s^2 R_1 R_2 [C_1 C_2 + C_p (C_1 + C_2)]). \qquad (44)$$

[3] C_8 can have a wide range of values depending on circuit configuration. It is largest for n-p-n input differential amps since the current source has a collector-substrate capacitance ($C_8 \cong$ 3–4 pF at its output. For p-n-p input stages it can be as small as 1–2 pF.



(a)



(b)

FIGURE 19. (a) Circuit showing "mirror" pole due to C_m and "tail" pole due to C_8. One component of the signal due to an inverting input must pass through either the mirror or tail poles. (b) Alternate circuit to *Figure 19(a)* (LM101, μA741) which has less excess phase. Reason is that half the inverting signal path need not pass through the mirror pole or the tail pole.

The denominator of (44) can be approximately factored under conditions that its two poles are widely separated. Fortunately, the poles are, in fact, widely separated under most normal operating conditions. Therefore, one can assume that the denominator of (44) has the form

$$D(s) = (1 + s/p_1)(1 + s/p_2)$$
$$= 1 + s(1/p_1 + 1/p_2) + s^2/p_1p_2. \quad (45)$$

With the assumption that p_1 is the dominant pole and p_2 is nondominant, i.e., $p_1 \ll p_2$, (45) becomes

$$D(s) \cong 1 + s/p_1 + s^2/p_1p_2. \quad (46)$$

Equating coefficients of s in (44) and (46), the dominant pole p_1 is found directly:

$$p_1 \cong \frac{1}{R_1(C_1 + C_p) + R_2(C_2 + C_P) + g_mR_1R_2C_p} \quad (47)$$

$$\cong \frac{1}{g_mR_1R_2C_p}. \quad (48)$$

The latter approximation (48), normally introduces little error, because the g_m term is much larger than the other two. We note at this point that p_1, which represents the dominant pole of the amplifier, is due simply to the familiar Miller-multiplied feedback capacitance $g_mR_2C_p$ combined with input node resistance, R_1. The nondominant pole p_2 is found similarly by equating s^2 coefficients in (44) and (46) to get p_1p_2, and dividing by p_1 from (48). The result is

$$p_2 \cong \frac{g_mC_p}{C_1C_2 + C_p(C_1 + C_2)}. \quad (49)$$

Several interesting things can be seen in examining (48) and (49). First, we note that p_1 is inversely proportional to g_m (and C_p), while p_2 is directly dependent on g_m (and C_p).

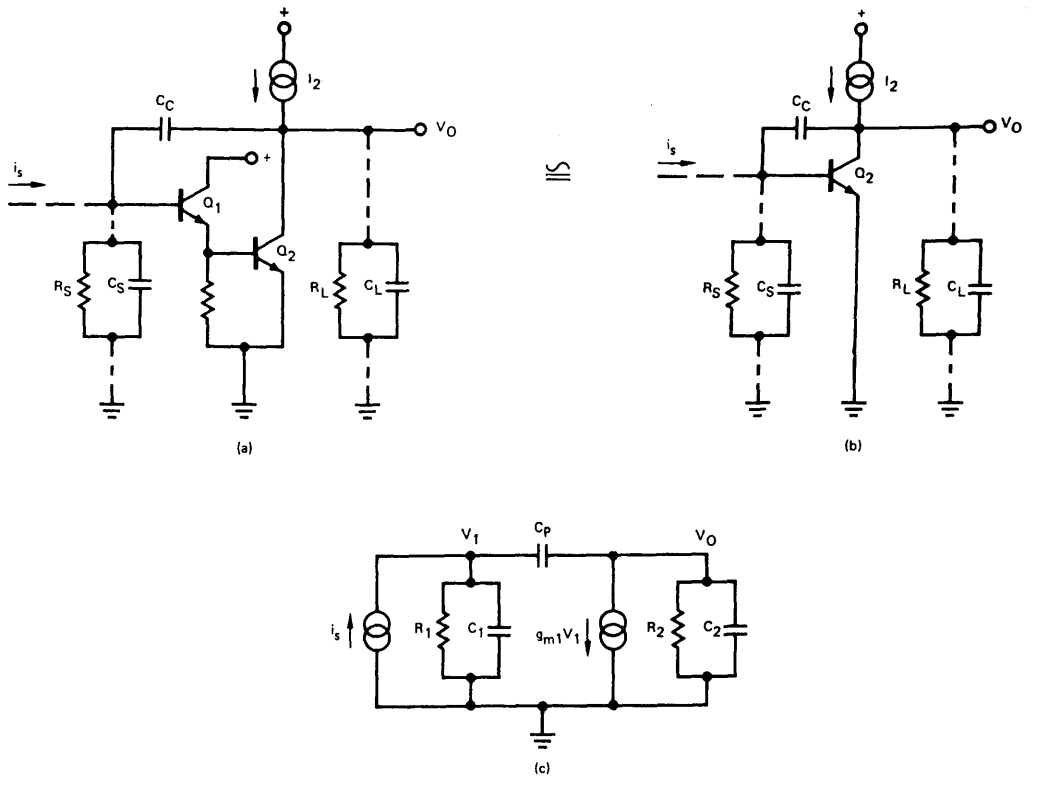


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FIGURE 20. Simplification of second stage used for pole-splitting analysis. (a) Complete second stage with input stage and output stage loading represented by R_8, C_8, and R_L, C_L respectively. (b) Emitter follower ignored to simplify analysis. (c) Hybrid π model substituted for transistor in (b). Source and load impedances are absorbed into model with the total impedances represented by R_1, C_1, and R_2 and C_2. Transistor base resistance is ignored and C_p includes both C_c and transistor collector-base capacitance.

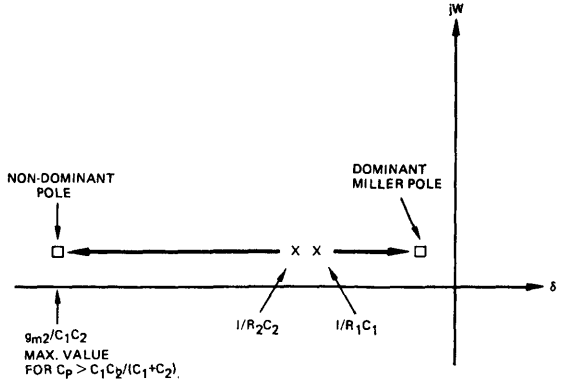

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FIGURE 21. Pole migration for second stage employing "pole-splitting" compensation. Plot is shown for increasing C_p and it is noted that the nondominant pole reaches a maximum value for large C_p.

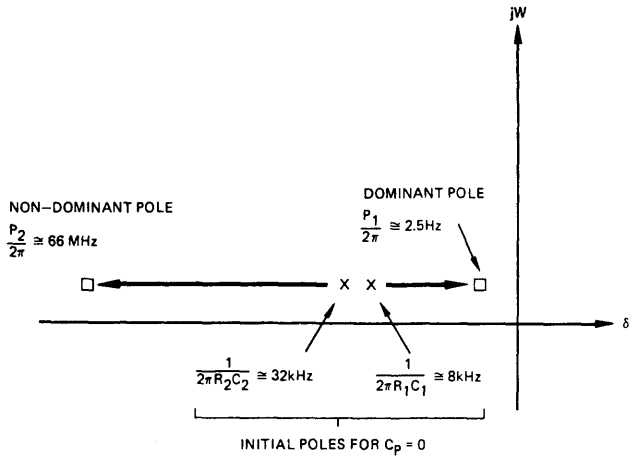

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FIGURE 22. Example of pole-splitting compensation in the μA741 op amp. Values used in (48) and (49) are: $g_{m2} = 1/87\Omega$, $C_p = 30$ pF, $C_1 \cong C_2 = 10$ pF, $R_1 = 1.7$ MΩ, $R_2 = 100$ kΩ.

Thus, as either C_p or transistor gain are increased, the dominant pole decreases and the nondominant pole increases. The poles p_1 and p_2 are being "split-apart" by the increased coupling action in a kind of inverse root locus plot.

This *pole-splitting* action is shown in *Figure 21,* where pole migration is plotted for C_p increasing from 0 to a large value. *Figure 22* further illustrates the action by giving specific pole positions for the μA741 op amp. It is seen that the initial poles (for $C_p = 0$) are both in the tens of kHz region and these are predicted to reach 2.5 Hz ($p_1/2\pi$) and 66 MHz ($p_2/2\pi$) after compensation is applied. This result is, of course, highly satisfactory since the second stage now has a single dominant pole effective over a wide frequency band.

C. Failure of Pole Splitting

There are several situations in which the application of pole-splitting compensation may not result in a single dominant pole response. One common case occurs in very wide-band op amps where the pole-splitting capacitor is small. In this situation the nondominant pole given by (49) may not become broadbanded sufficiently so that it can be ignored. To illustrate, suppose we attempt to minimize power dissipation by running the second stage of an LM118 (which has a small-signal bandwidth of 16 MHz) at 0.1 mA. For this op amp $C_p = 5$ pF, $C_1 \cong C_2 \cong 10$ pF. From (49), the nondominant pole is

$$\frac{p_2}{2\pi} \cong 16 \text{ MHz} \qquad (50)$$

which lies right at the unity-gain frequency. This pole alone would degrade phase margin by 45°, so it is clear that we need to bias the second stage with a collector current greater than 0.1 mA to obtain adequate g_m. Insufficient pole-splitting can therefore occur; but the cure is usually a simple increase in second stage g_m.

A second type of pole-splitting failure can occur, and it is often much more difficult to cope with. If, for example, one gets over-zealous in his attempt to broadband the nondominant pole, he soon discovers that other poles exist within the second stage which can cause difficulties. Consider a more exact equivalent circuit for the second stage of *Figure 20(a)* as shown in *Figure 23.* If the follower is biased at low currents or if c_p, Q_2 g_m, and/or r_x are high, the circuit can contain at least four important poles rather than the two

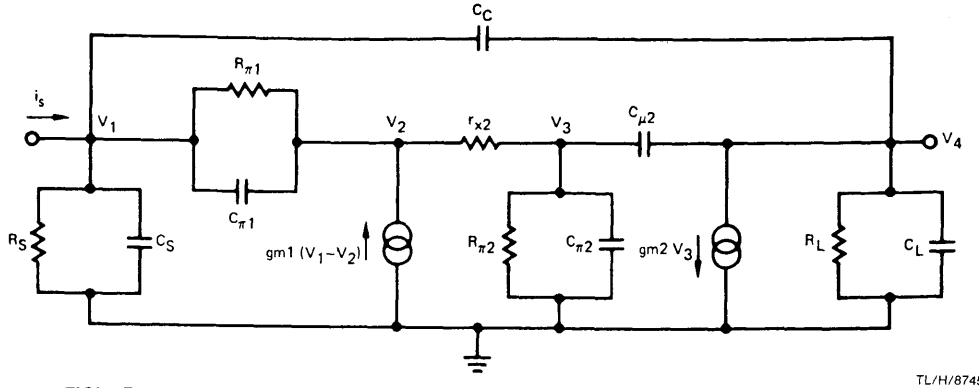

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FIGURE 23. More exact equivalent circuit for second stage of *Figure 20(a)* including a simplified π model for the emitter follower ($R\pi_1$, $C\pi_1$, g_{m1}) and a complete π for Q_2 (rx_2, $R\pi_2$, etc.).

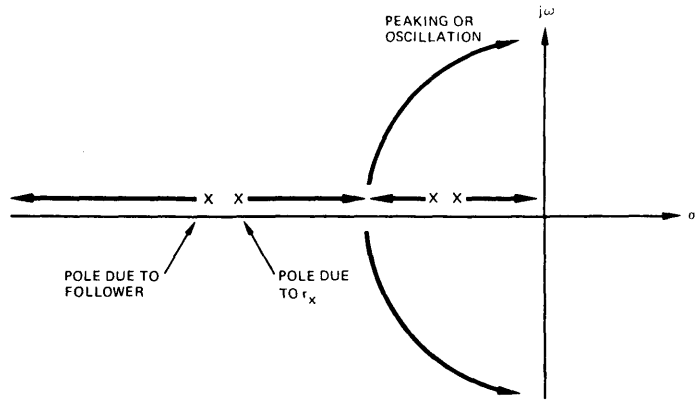

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FIGURE 24. Root locus for second stage illustrating failure of pole splitting due to high g_{m2}, r_{x2}, C_p, and/or low bias current in the emitter follower.

considered in simple pole splitting. Under these conditions, we no longer have a response with just negative real poles as in *Figure 21,* but observe a root locus of the sort shown in *Figure 24.* It is seen in this case that the circuit contains a pair of complex, possibly underdamped poles which, of course, can cause peaking or even oscillation. This effect occurs so commonly in the development of wide-band pole-split amplifiers that it has been (not fondly) dubbed "the second stage bump."

There are numerous ways to eliminate the "bump," but no single cure has been found which is effective in all situations. A direct hand analysis of *Figure 23* is possible, but the results are difficult to interpret. Computer analysis seems the best approach for this level of complexity, and numerous specific analyses have been made. The following is a list of circuit modifications that have been found effective in reducing the bump in various studies: 1) reduce g_{m2}, r_{x2}, $C_{\mu 2}$, 2) add capacitance or a series RC network from the stage input to ground—this reduces the high frequency local feedback due to C_p, 3) pad capacitance at the output for similar reasons, 4) increase operating current of the follower, 5) reduce C_p, 6) use a higher f_t process.

D. Troubles in the Output Stage

Of all the circuitry in the modern IC op amp, the class-AB output stage probably remains the most troublesome. None of the stages in use today behave as well as one might desire when stressed under worst case conditions. To illustrate, one of the most commonly used output stages is shown in *Figure 2(b).* The p-n-p's in this circuit are "substrate" p-n-p's having low current f_t's of around 20 MHz. Unfortunately, both β_0 and f_t begin to fall off rapidly at quite low current densities, so as one begins to sink just a few milliamps in the circuit, phase margin troubles can develop. The worst effect occurs when the amplifier is operated with a large capacitive load (>100 pF) while sinking high currents. As shown in *Figure 25,* the load capacitance on the

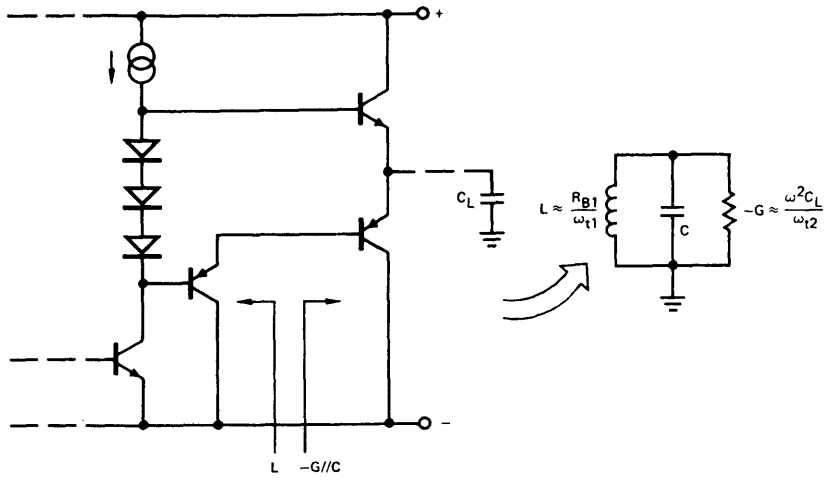

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FIGURE 25. Troubles in the conventional class-AB output stage of *Figure 2(b).* The low f_t output p-n-p's interact with load capacitance to form the equivalent of a one-port oscillator.

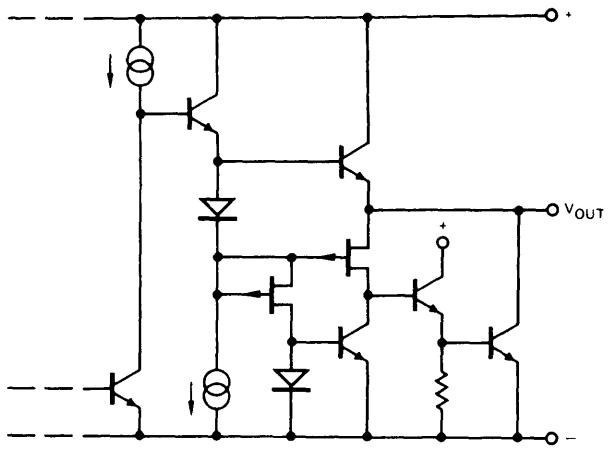

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FIGURE 26. The "BI-FET™" output stage employing JFET's and bipolar n-p-n's to eliminate sensitivity to load capacitance.

output follower causes it to have negative input conductance, while the driver follower can have an inductive output impedance. These elements combine with the capacitance at the interstage to generate the equivalent of a one-port oscillator. In a carefully designed circuit, oscillation is suppressed, but peaking (the "output bump") can occur in most amplifiers under appropriate conditions.

One new type of output circuit which does not use p-n-p's is shown in *Figure 26* [6]. This circuit employs compatible JFET's (or MOSFET's, see similar circuit in [11]) in a FET/bipolar quasi-complementary output stage, which is insensitive to load capacitance. Unfortunately, this circuit is rather complex and employs extra process steps, so it does not appear to represent the cure for the very low cost op amps.

7. The Gain Cell: Linear Large-Scale Integration

As the true limitations of the basic op amp are more fully understood, this knowledge can be applied to the development of more "optimum" amplifiers. There are, of course, many ways in which one might choose to optimize the device. We might, for example, attempt to maximize speed (bandwidth, slew rate, settling time) without sacrificing dc characteristics. The compatible JFET/bipolar amp of *Figure 15* represents such an effort. An alternate choice might be to design an amplifier having all of the performance features of the most widely used general purpose op amps (i.e., μA741, LM107, etc.), but having minimum possible die area. Such a pursuit is parallel to the efforts of digital large-scale integration (LSI) designers in their devlelopment of minimum

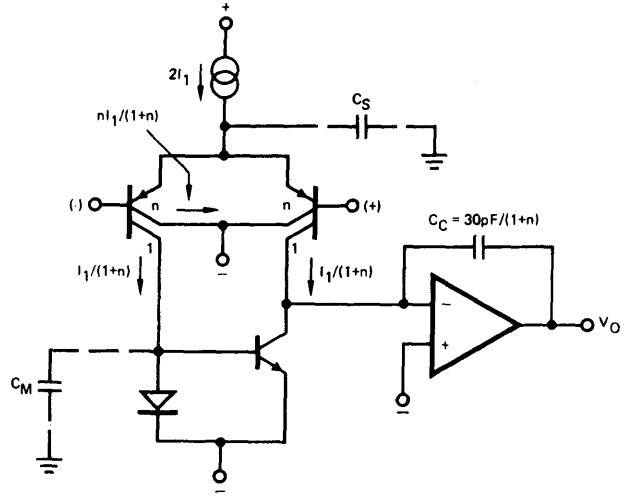

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FIGURE 27. Basic g_m reduction obtained by using split collector p-n-p's. C_c and area are reduced since $C_c = g_{m1}/\omega_u$.

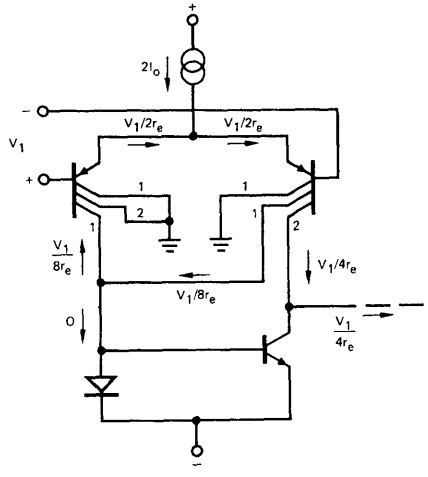
area memory cells or gates. The object of such efforts, of course, is to develop lower cost devices which allow wide and highly economic usage.

In this section we briefly discuss certain aspects of the linear *gain cell,* a general purpose, internally compensated op amp having a die area which is significantly smaller than that of equivalent, present day, industry standard amplifiers.

A. Transconductance Reduction

The single largest area component in the internally compensated op amp is the compensation capacitor (about 30 pF, typically). A major interest in reducing amplifier die area, therefore, centers about finding ways in which this capacitor can be reduced in size. With this in mind, we find it useful to examine (15), which relates compensation capacitor size to two other parameters, unity gain corner frequency ω_u, and first stage transconductance g_{m1}. It is immediately apparent that for a fixed, predetermined unity gain corner (about $2\pi \times 1$ MHz in our case), there is only one change that can be made to reduce the size of C_c: *the transconductance of the first stage must be reduced.* If we restrict our interest to simple bipolar input stages (for low cost), we recall the $g_{m1} = qI_1/kT$. Only by reducing I_1 can g_{m1} be reduced, and we earlier found in Section 6-A and *Figure 19(a)* and *(b)* that I_1 cannot be reduced much without causing phase margin difficulties due to the mirror pole and the tail pole.

An alternate basic approach to g_m reduction is illustrated in *Figure 27* [12]. there, a multiple collector p-n-p structure, which is easily fabricated in IC form, is used to split the collector current into two components, one component (the larger) of which is simply tied to ground, thereby "throwing away" a major portion of the transistor output current. The result is that the g_m of the transistor is reduced by the ratio of $1/(1 + n)$ (see *Figure 27*), and the compensation capaci-



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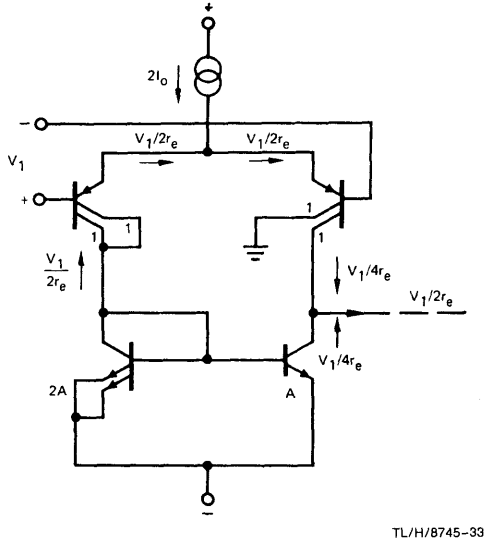
(a)



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(b)

FIGURE 28. Variations on g_m reduction. (a) Cross-coupled connection eliminates all ac current passing through the mirror, yet maintains dc balance. (b) This approach maintains high current on the diode side of the mirror, thereby broadbanding the mirror pole.

tance can be reduced directly by the same factor. It might appear that the mirror pole would still cause difficulties since the current mirror becomes current starved in *Figure 27,* but the effect is not as severe as might be expected. The reason is that the inverting signal can now pass through the high current wide-band path, across the differential amp emitters and into the second stage, so at least half the signal current does not become bandlimited. This partial bandlimiting can be further reduced by using one of the circuits in *Figure 28(a)* or *(b).*[4] In (a), the p-n-p collectors are cross coupled in such a way that the ac signal is cancelled in the mirror circuit, while dc remains completely balanced. Thus the mirror pole is virtually eliminated. The circuit does have a drawback, however, in that the uncorrelated noise currents coming from the two p-n-p's add rather than subtract at the input to the mirror, thereby degrading noise performance. The circuit in *Figure 28(b)* does not have this defect, but requires care in matching p-n-p collector ratios to n-p-n emitter areas. Otherwise offset and drift will degrade as one attempts to reduce g_m by large factors.

B. A Gain Cell Example

As one tries to make large reductions in die area for the gain cell, many factors must be considered in addition to novel circuit approaches. Of great importance are special layout/circuit techniques which combine a maximum number of components into minimum area.

In a good layout, for example, all resistors are combined into islands with transistors. If this is not possible initially, circuit and device changes are made to allow it. The resulting device geometrics within the islands are further modified in shape to allow maximum "packing" of the islands. That is, when the layout is complete, the islands should have shapes which fit together as in a picture puzzle, with no waste of space. Further area reductions can be had by modifying the isolation process to one having minimum spacing between the isolation diffusion and adjacent p-regions.

As example of a gain cell which employs both circuit and layout optimization is shown in *Figure 29*: This circuit uses the g_m reduction technique of *Figure 28(a)* which results in a compensation capacitor size of only 5 pF rather than the normal 30 pF. The device achieves a full 1 MHz bandwidth, a 0.67V/μs slew rate, a gain greater than 100,000, typical offset voltages less than 1 mV, and other characteristics normally associated with an LM107 or μA741. In quad form each amplifier requires an area of only 23 x 35 mils which is one-fourth the size of today's industry standard μA741 (typically 56 x 56 mils). This allows over 8000 possible gain cells to be fabricated on a single 3-inch wafer. Further, it appears quite feasible to fabricate larger arrays of gain cells, with six or eight on a single chip. Only packaging and applications questions need be resolved before pursuing such a step.

[4]The circuit in *Figure 28(a)* is due to R. W. Russell and the variation in *Figure 28(b)* was developed by D. W. Zobel.

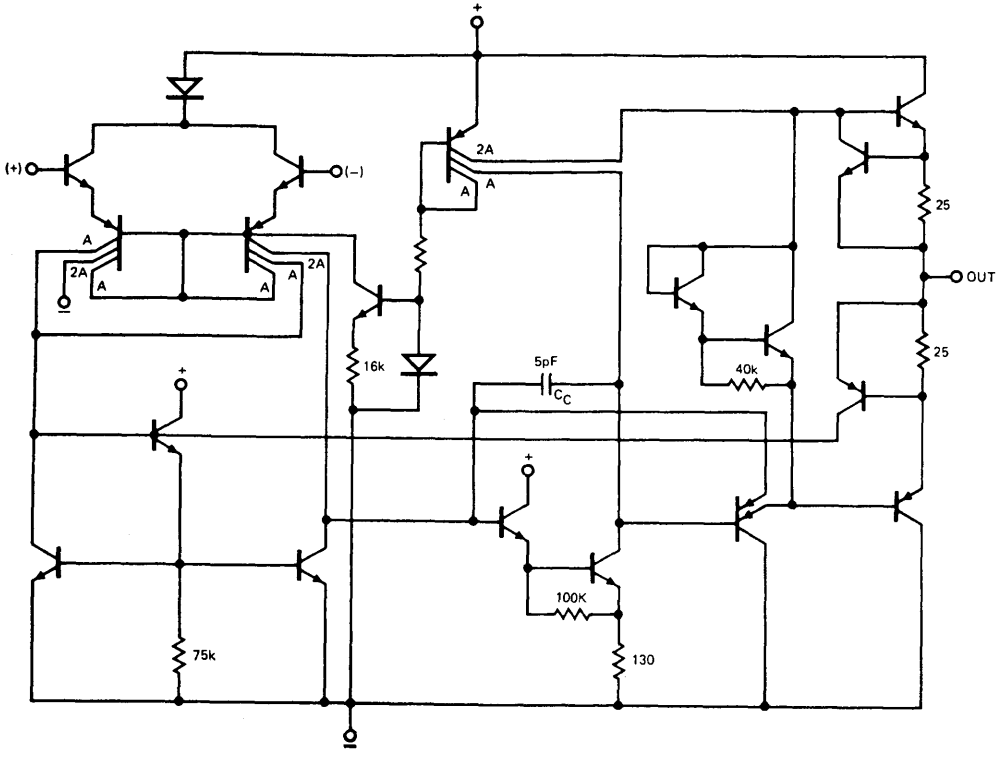

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FIGURE 29. Circuit for optimized gain cell which has been fabricated in one-fourth the die size of the equivalent μA741.

ACKNOWLEDGMENT

Many important contributions were made in the gain cell and FET/bipolar op amp areas by R. W. Russell. The author gratefully acknowledges his very competent efforts.

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[12] J. E. Solomon and R. W. Russell, "Transconductance Reduction Using Mulitple Collector PNP Transistors in an Operational Amplifier," U.S. Patent 3801923, Mar. 1974.

See also, as a general reference:

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V/F Converter ICs Handle Frequency-to-Voltage Needs

National Semiconductor
Appendix C
Robert A. Pease

Simplify your F/V converter designs with versatile V/F ICs. Starting with a basic converter circuit, you can modify it to meet almost any application requirement. You can spare yourself some hard labor when designing frequency-to-voltage (F/V) converters by using a voltage-to-frequency IC in your designs. These ICs form the basis of a series of accurate, yet economical, F/V converters suiting a variety of applications.

Figure 1 shows an LM331 IC (or LM131 for the military temperature range) in a basic F/V converter configuration (sometimes termed a stand-alone converter because it requires no op amps or other active devices other than the IC). (Comparable V/F ICs, such as RM4151, can take advantage of this and other circuits described in this article, although they might not always be pin-for-pin compatible).

This circuit accepts a pulse-train or square wave input amplitude of 3V or greater. The 470 pF coupling capacitor suits negative-going input pulses between 80 μs and 1.5 μs, as well as accommodating square waves or positive-going pulses (so long as the interval between pulses is at least 10 μs).

IC Handles the Hard Part

The LM331 detects an input-signal change by sensing when pin 6 goes negative relative to the threshold voltage at pin 7, which is nominally biased 2V lower than the supply voltage. When a signal change occurs, the LM331's input comparator sets an internal latch and initiates a timing cycle. During this cycle, a current equal to V_{REF}/R_S flows out of pin 1 for a time $t = 1.1\ R_tC$. The 1 μF capacitor filters this pulsating current from pin 1, and the current's average value flows through load resistor R_L. As a result, for a 10 kHz input, the circuit outputs 10 V_{DC} across R_L with good (0.06% typical) nonlinearity.

Two problems remain, however: the output at V1 includes about 13 mVp-p ripple, and it also lags 0.1 second behind an input frequency step change, settling to 0.1% of full-scale in about 0.6 second. This ripple and slow response represent an inherent tradeoff that applies to almost every F/V converter.

The Art of Compromise

Increasing the filter capacitor's value reduces ripple but also increases response time. Conversely, lowering the filter capacitor's value improves response time at the expense of larger ripple. In some cases, adding an active filter results in faster response and less ripple for high input frequencies.

Although the circuit specifies a 15V power supply, you can use any regulated supply between 4 V_{DC} and 40 V_{DC}. The output voltage can extend to within 3 V_{DC} of the supply voltage, so choose R_L to maintain that output range.

Adding a 220 kΩ/0.1 μF postfilter to the circuit slows the response slightly, but it also reduces ripple to less than 1 mVp-p for frequencies from 200 Hz to 10 kHz. The reduction in ripple achieved by adding this passive filter, while not as good as that obtainable using an active filter, could suffice in some applications.

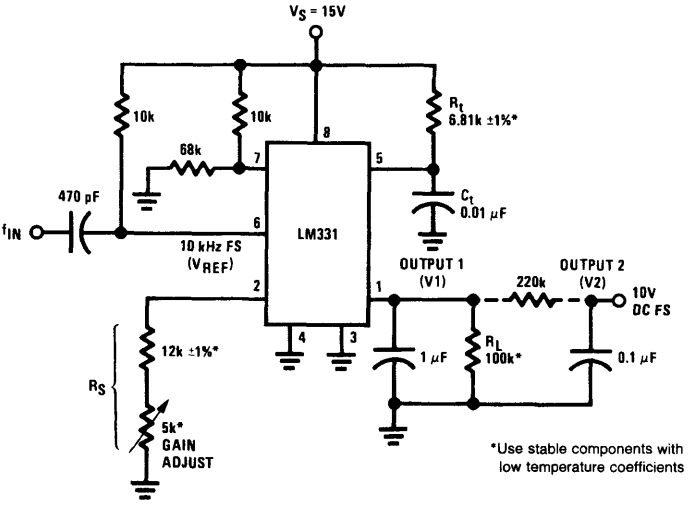

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FIGURE 1. A Simple Stand-Alone F/V Converter Forms the Basis for Many Other Converter-Circuit Configurations

Improving the Basic Circuit

Further modifications and additions to the basic F/V converter shown in *Figure 1* can adapt it to specific performance requirements. *Figure 2* shows one such modification, which improves the converter's nonlinearity to 0.006% typical.

Reconsideration of the basic stand-alone converter shows why its nonlinearity falls short of this improved version's. At low input frequencies, the current source feeding pin 1 in the LM331 is turned off most of the time. As the input frequency increases, however, the current source stays on more of the time, and its own impedance attenuates the output signal for an increasing fraction of each cycle time. This disproportionate attenuation at higher frequencies causes a parabolic change in full-scale gain rather than the desired linear one.

In the improved circuit, on the other hand, the PNP transistor acts as a cascade, so the output impedance at pin 1 sees a constant voltage that won't modulate the gain. Also, with an alpha ranging between 0.998 and 0.990, the transistor exhibits a temperature coefficient of between 10 ppm/°C and 40 ppm/°C—a fairly minor effect. Thus, this circuit's nonlinearity does not exceed 0.01% maximum for the 10V output range shown and is normally not worse than 0.01% for any supply voltage between 4V and 40V.

Add an Output Buffer

The circuit in *Figure 3* adds an output buffer (unity-gain follower) to the basic single-supply F/V converter. Either an LM324 or LM358 op amp functions well in a single-supply circuit because these devices' common-mode ranges extend down to ground. But if a negative supply is available, you can use any op amp; types such as the LF351B or LM308A, which have low input currents, provide the best accuracy.

The output buffer in *Figure 3* also acts as an active filter, furnishing a 2-pole response from a single op amp. This filter provides the general response

$$V_{OUT}/I_{OUT} = R_L/(1 + K1p + K2p^2).$$

(p is the differential operator d/dt.) As shown, R_L controls the filter's DC gain. The high frequency response rolls off at 12 dB/octave. Near the circuit's natural resonant frequency, you can choose the damping to give a little overshoot—or none, as desired.

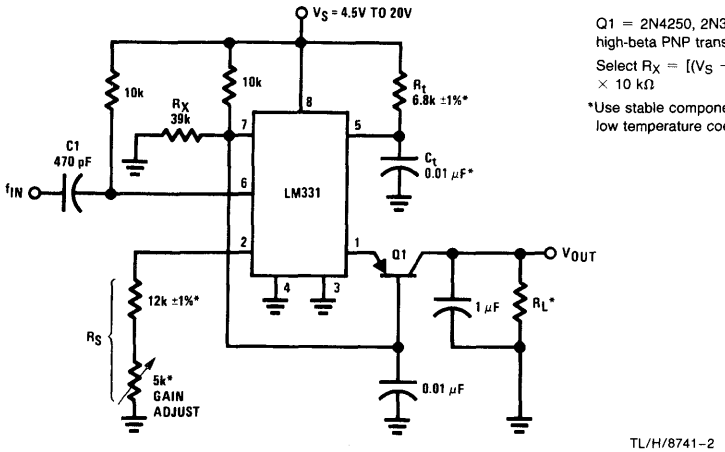

FIGURE 2. Adding a Cascade Transistor to the LM331's Output Improves Nonlinearity to 0.006%

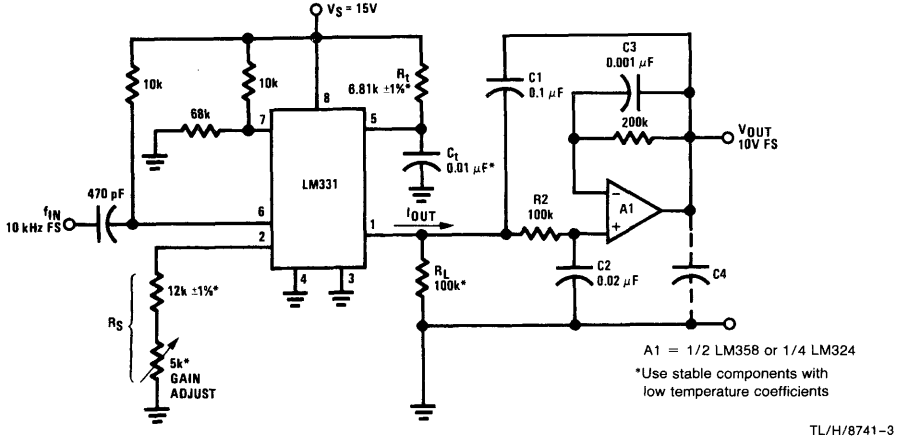

FIGURE 3. The Op Amp on This F/V Converter's Output Acts as a Buffer as Well as a 2-Pole Filter

Dealing with F/V Converter Ripple

Voltage ripple on the output of F/V converters can present a problem, and the chart shown in *Figure A* indicates exactly how big a problem it is. A simple, slow, RC filter exhibits low ripple at all frequencies. Two-pole filters offer the lowest ripple at high frequencies and provide a 30-times-faster step response than RC devices.

To reduce a circuit's ripple at moderate frequencies, however, you can cascade a second active-filter stage on the F/V converter's output. That circuit's response also appears in *Figure A* and shows a significant improvement in low-ripple bandwidth over the single-active-filter configuration, with only a 30% degradation of step response.

Figures B and *C* show filter circuits suitable for cascading. The inverting filter in *Figure B* requires closely matched resistors with a low TC over their temperature range for best accuracy. For lowest DC error, choose R5 = R2 + ($R_{IN}|R_F$). This circuit's response is

$$-V_{OUT}/V_{IN} = n/(1 + (R_F + R2 + nR2)C4p + R_FR2C3C4p^2).$$

where n = DC gain. If $R_{IN} = R_F$ and n = 1,

$$-V_{OUT}/V_{IN} = 1/(1 + (R_F + 2R2)C4p + R_FR2C3C4p^2).$$

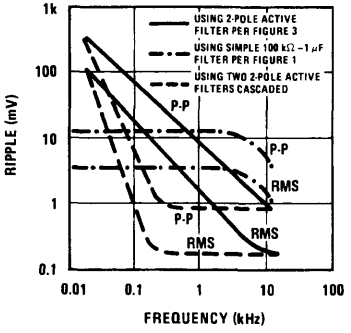

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FIGURE A. Output-Ripple Performance of Several Different F/V Converter Configurations Illustrates the Effect of Voltage Ripple

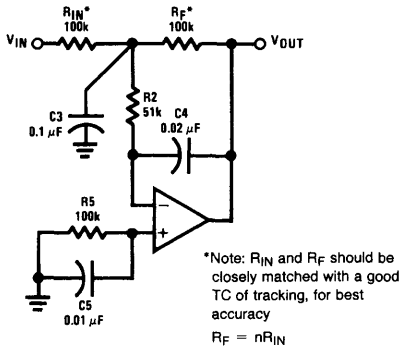

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FIGURE B. You Can Cascade This 2-Pole Inverting Filter onto an F/V Converter's Output

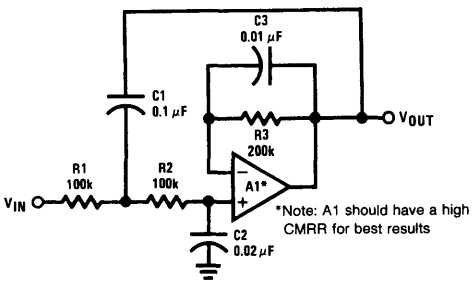

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FIGURE C. This 2-Pole Noninverting Filter Suits Cascade Requirements on F/V Converter Outputs

The circuit shown in *Figure C* does not require precision passive components, but for best accuracy, choosing an A1 with a high CMRR is critical. An LM308A op amp's 96 dB minimum CMRR suits this circuit well, but an LM358B's 85 dB typical figure also proves adequate for many applications. Circuit response is

$$V_{OUT}/V_{IN} = 1/(1 + (R1 + R2)\,C2p + R1R2C1C2p^2).$$

For best results, choose R3 = R1 + R2.

Components Determine Response

The specific response of the circuit in *Figure 3* is

$$V_{OUT}/I_{OUT} = R_L/(1 + (R_L + R2)C2p + R_LR2C1C2C2p^2).$$

Making C2 relatively large eliminates overshoot and sine peaking. Alternatively, making C2 a suitable fraction of C1 (as is done in *Figure 3*) produces both a sine response with 0 dB to 1 dB of peaking and a quick real-time response having only 10% to 30% overshoot for a step response. By maintaining *Figure 3's* ratio of C1:C2 and R2:R_L, you can adapt its 2-pole filter to a wide frequency range without tedious computations.

This filter settles to within 1% of a 5V step's final value in about 20 ms. By contrast, the circuit with the simple RC filter shown in *Figure 1* takes about 900 ms to achieve the same response, yet offers no less ripple than *Figure 3's* op amp approach.

As for the other component in the 2-pole filter, any capacitance between 100 pF and 0.05 μF suits C3 because it serves only as a bypass for the 200 kΩ resistor. C4 helps reduce output ripple in single positive power-supply systems when V_{OUT} approaches so close to ground that the op amp's output impedance suffers. In this circuit, using a tantalum capacitor of between 0.1 μF and 2.2 μF for C4 usually helps keep the filter's output much quieter without degrading the op amp's stability.

Avoid Low-Leakage Limitations

Note that in most ordinary applications, this 2-pole filter performs as well with 0.1 μF and 0.02 μF capacitors as the passive filter in *Figure 1* does with 1 μF. Thus, if you require a 100 Hz F/V converter, the circuit in *Figure 3* furnishes good filtering with C1 = 10 μF and C2 = 2 μF, and eliminates the 100 μF low-leakage capacitor needed in a passive filter.

Note also that because C1 always has zero DC voltage across it, you can use a tantalum or aluminum electrolytic capacitor for C1 with no leakage-related problems; C2, however, must be a low-leakage type. At room temperature, typical 1 μF tantalum components allow only a few nanoamperes of leakage, but leakage this low usually cannot be guaranteed.

Compensating for Temperature Coefficients

F/V converters often encounter temperature-related problems usually resulting from the temperature coefficients of passive components. Following some simple design and manufacturing guidelines can help immunize your circuits against loss of accuracy when the temperature changes.

Capacitors fabricated from Teflon or polystyrene usually exhibit a TC of −110 ±30 ppm/°C. When you use such a component for the timing capacitor in an F/V converter (such as C_t in the *figure*) the circuit's output voltage—or the gain in terms of volts per kilohertz—also exhibits a −110 ppm/°C TC.

But the resistor-diode network (R_X, D1, D2) connected from pin 2 to ground in the *figure* can cancel the effect of the timing capacitor's large TC. When R_X = 240 kΩ, the current flowing through pin 1 will then have an overall TC of 110 ppm/°C, effectively canceling a polystyrene timing capacitor's TC to a first approximation. Thus, you needn't find a zero-TC capacitor for C_t, so long as its temperature coefficient is stable and well established. As an additional advantage, the resistor-diode network nearly compensates to zero the TC of the rest of the circuit.

Bake It for a While

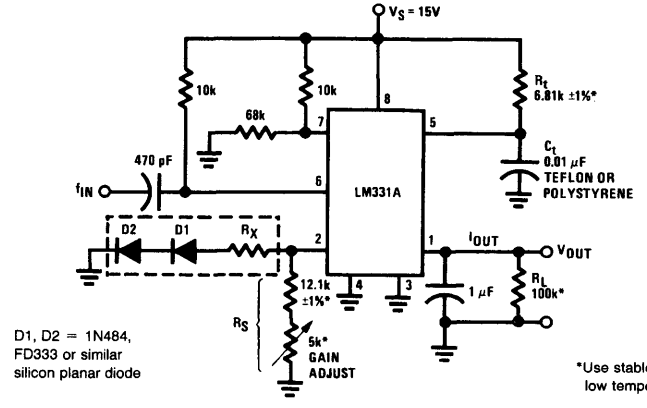
After the circuit has been built and checked out at room temperature, a brief oven test will indicate the sign and the size of the TC for the complete F/V converter. Then you can add resistance in series with R_X, or add conductance in parallel with it, to greatly diminish the TC previously observed and yield a complete circuit with a lower TC than you could obtain simply by buying low TC parts.

For example, if the circuit increases its full-scale output by 0.1% per 30°C (33 ppm/°C) during the oven test, adding 120 kΩ in series with R_X = 240 kΩ cancels the temperature-caused deviation. Or, if the full-scale output decreases by −0.04% per 20°C (−20 ppm/°C), just add 1.2 MΩ in parallel with R_X.

Note that to allow trimming in both directions, you must start with a finite *fixed* TC (such as the −110 ppm/°C of C_t), which then nominally cancels out by the addition of a finite *adjustable* TC. Only by using this procedure can you compensate for whatever polarity of TC is found by the oven test.

You can utilize this technique to obtain TCs as low as 20 ppm/°C, or perhaps even 10 ppm/°C, if you take a few passes to zero-in on the best value for R_X. For optimum results, consider the following guidelines:

- Use a good capacitor for C_t; the cheapest polystyrene capacitors can shift value by 0.05% or more per temperature cycle. In that case, you would not be able to distinguish the actual temperature sensitivity from the hysteresis, and you would also never achieve a stable circuit.
- After soldering, bake or temperature-cycle the circuit (at a temperature not exceeding 75°C in the case of polystyrene) for a few hours to stabilize all components and to relieve the strains of soldering.
- Do not rush the trimming. Recheck the room temperature value before *and* after you take the high temperature data to ensure a reasonably low hysteresis per cycle.
- Do not expect a perfect TC at −25°C if you trim for ±5 ppm/°C at temperatures from +25°C to 60°C. None of the components in the *figure's* circuit offer linearity much better than 5 ppm/°C or 10 ppm/°C cold, if trimmed for a zero TC at warm temperatures. Even so, using these techniques you can obtain a data converter with better than 0.02% accuracy and 0.003% linearity, for a ±20°C range around room temperature.
- Start out the trimming with R_X installed and its value near the design-center value (e.g., 240 kΩ or 270 kΩ), so you



Two Diodes and a Resistor Help Decrease an F/V Converter's Temperature Coefficient

will be reasonably close to zero TC; you will usually find the process slower if you start without any resistor, because the trimming converges more slowly.

- If you change R_X from 240 kΩ to 220 kΩ, do not pull out the 240 kΩ part and put in a new 220 kΩ resistor—you will get much more consistent results by adding a 2.4 MΩ resistor in parallel. The same admonition holds true for adding resistance in series with R_X.
- Use reasonably stable components. If you use an LM331A (±50 ppm/°C maximum) and RN55D film resistors (each ±100 ppm/°C) for R_L, R_t and R_S, you probably won't be able to trim out the resulting ±350 ppm/°C worst-case TC. Resistors with a TC specification of 25 ppm/°C usually work well. Finally, use the same resistor value (e.g., 12.1 kΩ ±1%) for both R_S and R_t; when these resistors come from the same manufacturer's batch, their TC tracking will usually rate at better than 20 ppm/°C.

Whenever an op amp is used as a buffer (as in *Figure 3*), its offset voltage and current (±7.5 mV maximum and ±100 nA, respectively, for most inexpensive devices) can cause a ±17.5 mV worst-case output offset. If both plus and minus supplies are available, however, you can easily provide a symmetrical offset adjustment. With only one supply, you can add a small positive current to each op amp input and also trim one of the inputs.

Need a Negative Output?

If your F/V converter application requires a negative output voltage, the circuit shown in *Figure 4* provides a solution with excellent linearity (±0.003% typical, ±0.01% maximum). And because pin 1 of the LM331 always remains at 0 V_{DC}, this circuit needs no cascade transistor. (Note, however, that while the circuit's nonlinearity error is negligible, its ripple is not.)

The circuit in *Figure 4* offers a significant advantage over some other designs because the offset adjust voltage derives from the stable 1.9 V_{DC} reference voltage at pin 2 of the LM331; thus any supply voltage shifts cause no output shifts. The offset pot can have any value between 200 kΩ and 2 MΩ.

An optional bypass capacitor (C2) connected from the op amp's positive input to ground prevents output noise arising from stray noise pickup at that point; the capacitance value is not critical.

A Familiar Response

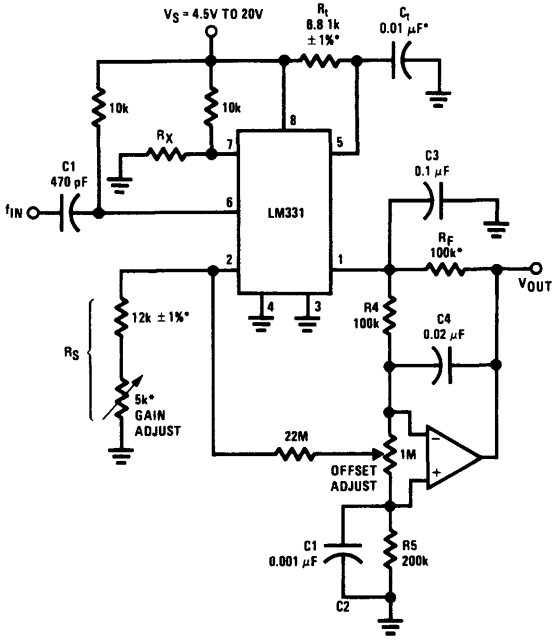
The circuit in *Figure 4* exhibits the same 2-pole response—with heavy output ripple attenuation—as the noninverting filter in *Figure 3*. Specifically,

$$V_{OUT}/I_{OUT} = R_F/(1 + (R4 + R_F)C4p + R4R_FC3C4p^2).$$

Here also, R5 = R4 + R_F = 200 kΩ provides the best bias current compensation.

The LM331 can handle frequencies up to 100 kHz by utilizing smaller-value capacitors as shown in *Figure 5*. This circuit increases the current at pin 2 to facilitate high-speed switching, but, despite these speed-ups, the LM331's 500 ppm/°C TC at 100 kHz causes problems because of switching speed shifts resulting from temperature changes.

To compensate for the device's positive TC, the LM334 temperature sensor feeds pin 2 a current that decreases linearly with temperature and provides a low overall temperature coefficient. An R_y value of 30 kΩ provides first-order compensation, but you can trim it higher or lower if you need more precise TC correction.



TL/H/8741–8

FIGURE 4. In This F/V Circuit, the Output-Buffer Op Amp Derives Its Offset Voltage from the Precision Voltage Source at Pin 2 of the LM331

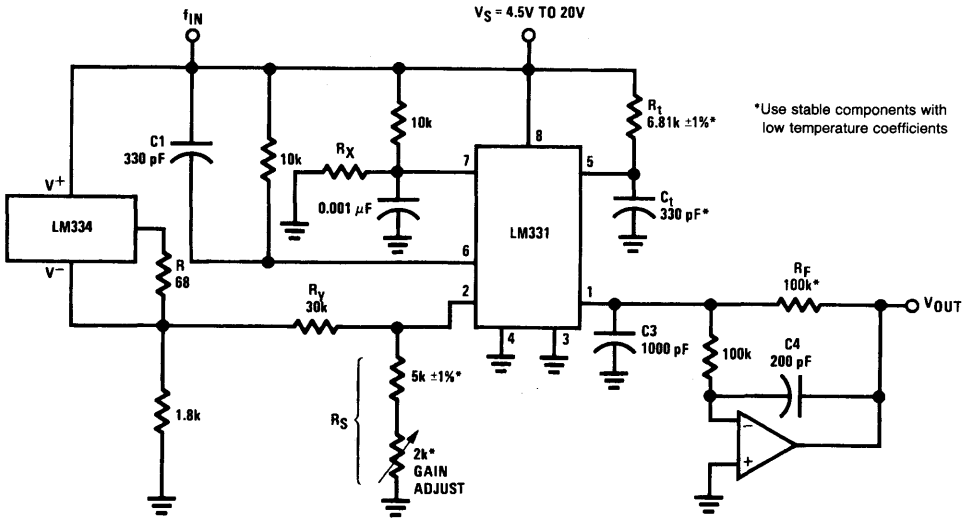
Detect Frequencies Accurately

Using an F/V converter combined with a comparator as a frequency detector is an obvious application for these devices. But when the F/V converter is utilized in this way, its output ripple hampers accurate frequency detection, and the slow filter frequency response causes delays.

If a quick response is not important, though, you can effectively utilize an LM331-based F/V converter to feed one or more comparators, as shown in *Figure 6*. For an input frequency drop from 1.1 kHz to 0.5 kHz, the converter's output responds within about 20 ms. When the input falls from 9 kHz to 0.9 kHz, however, the output responds only after a 600 ms lag, so utilize this circuit only in applications that can tolerate F/V circuits' inherent delays and ripples.

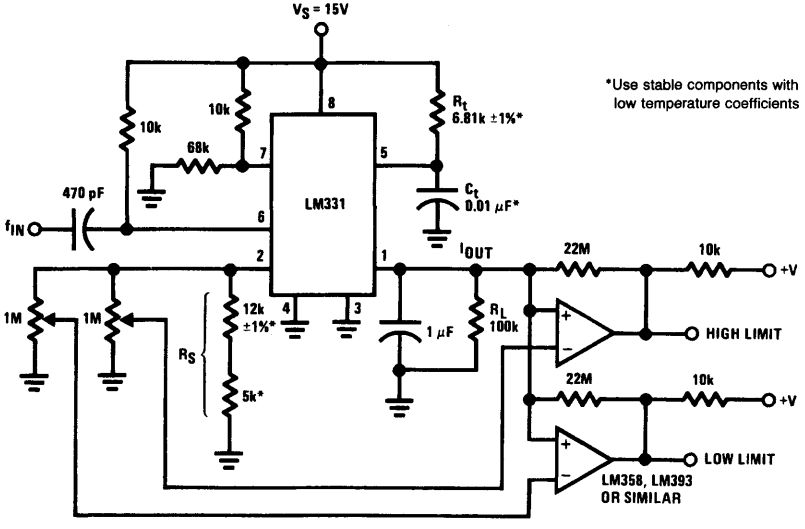
Author's Biography

Bob Pease is a staff scientist in the Advanced Linear Integrated Circuit Group at National Semiconductor Corp., Santa Clara, CA. Holder of four patents, he earned a BSEE from MIT. Bob lists tracking abandoned railroad roadbeds and designing V/F converters as hobbies.



TL/H/8741–9

FIGURE 5. An LM334 Temperature Sensor Compensates for the F/V Circuit's Temperature Coefficient



TL/H/8741–10

FIGURE 6. Combining a V/F IC with Two Comparators Produces a Slow-Response Frequency Detector

Versatile Monolithic V/Fs Can Compute as Well as Convert with High Accuracy

National Semiconductor
Appendix D
Robert A. Pease

The best of the monolithic voltage-to-frequency (V/F) converters have performance that's so good it equals or exceeds that of modular types. Some of these ICs can be designed into quite a variety of circuits because they're notably versatile. Along with versatility and high performance come the advantages that are characteristic of all V/F converters, including good linearity, excellent resolution, wide dynamic range, and an output signal that's easy to transmit as well as couple through an isolator.

One of the recently introduced monolithic types, the LM131, has both high performance and a design that's rather flexible. For instance, it can compute and convert at the same time; the computation is a part of the conversion. Among other functions, it can provide the product, ratio and square root of analog inputs.

This IC has an internal reference for its conversion circuitry that's also brought out to a pin, so it's available to external circuits associated with the converter. Not surprisingly, it turns out that any deviations of the reference, due to process variations and temperature changes have equal and opposite effects on the scale factors of the converter and the external circuitry. (This presumes, of course, that the scale factor of the external circuitry is a linear function of voltage.)

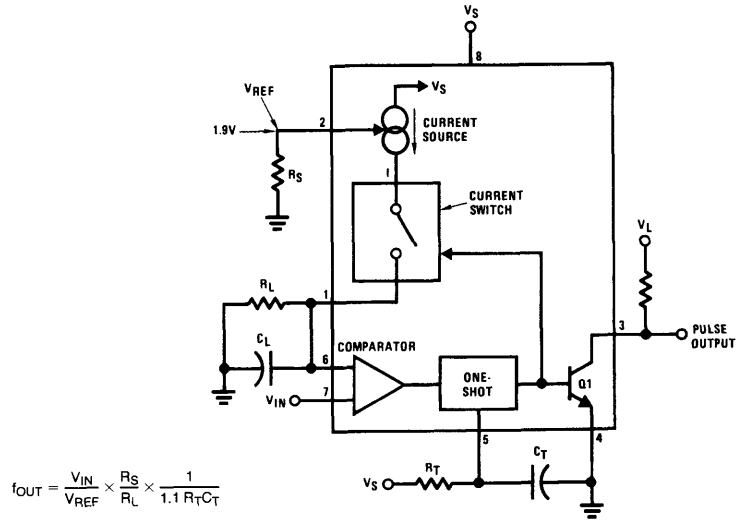
PRECISION RELAXATION OSCILLATOR

Before looking at some applications, quickly take a look at the basic circuit of an LM131 V/F converter *(Figure 1)*. Basically, this IC, like any V/F converter, is a precision relaxation oscillator that generates a frequency linearly proportional to the input voltage. As might be expected, the circuit has a capacitor, C_L, with a sawtooth voltage on it. Generally speaking, the circuit is a feedback loop that keeps this capacitor charged to a voltage very slightly higher than the input voltage, V_{IN}. If V_{IN} is high, C_L discharges relatively quickly through R_L, and the circuit generates a high frequency. If V_{IN} is low, C_L discharges slowly, and the converter puts out a low frequency.

When C_L discharges to a voltage equal to the input, the comparator triggers the one-shot. The one-shot closes the current switch and also turns on the output transistor. With the switch closed, current from the current source recharges C_L to a voltage somewhat higher than the input. Charging continues for a period determined by R_T and C_T. At the end of this period, the one-shot returns to its quiescent state and C_L resumes discharging.

Resistor R_S sets the amount of current put out by the current source. In fact, the current in pin 1, with the switch on, is identical to the current in pin 2. The latter pin is at a constant voltage (nominally 1.90V), so a given resistor value can set the operating currents. When connected to a high impedance buffer, this pin provides a stable reference for external circuits.

The open-collector output at pin 3 permits the output swing to be different from the converter's supply voltage, if the load circuit requires. The supplies don't have to be separate, however, and both the converter and its load can use the same voltage.



$$f_{OUT} = \frac{V_{IN}}{V_{REF}} \times \frac{R_S}{R_L} \times \frac{1}{1.1\,R_T C_T}$$

TL/H/8742–1

FIGURE 1. A voltage-to-frequency converter such as this is a relaxation oscillator with a frequency proportional to the input voltage. Current pulses keep C_L's average voltage slightly greater than the input voltage.

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STEADY AS SHE GOES

By far the simplest of the circuits that make use of the reference output voltage from the LM131 is one that simply ties this output pin right back to the signal input. This connection is just a V/F converter with a constant input, which makes it a constant-frequency oscillator. Even with this simple circuit *(Figure 2)*, variations in the reference voltage have two opposite effects that cancel each other out, so the circuit is particularly stable. In this type of circuit, the temperature-dependent internal delays tend to cancel as well, which isn't true of relaxation oscillators based on op amps or comparators.

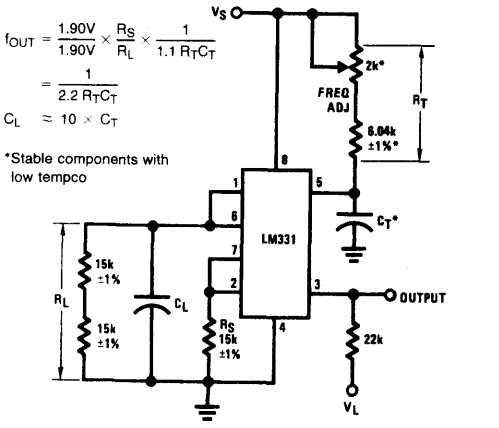

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FIGURE 2. A V/F converter is a stable-frequency oscillator if its input is connected to its reference output. If the reference voltage changes, the effects of the change cancel out, so the frequency doesn't change. With low tempco components for R_T and C_T, frequency stability vs temperature can be as good as ±25 ppm/°C.

Resistors R_L and R_S are best taken from the same batch. (R_L must be larger than R_S, so it's made up of two resistors.) By doing this, the tempco tracking, which is the critical parameter, is five to ten times better than it would be if R_L were a single 30.1 kΩ resistor.

Although the reference output, pin 2, can't be loaded without affecting the converter's sensitivity, the comparator input, pin 7, has a high impedance so this connection does no harm.

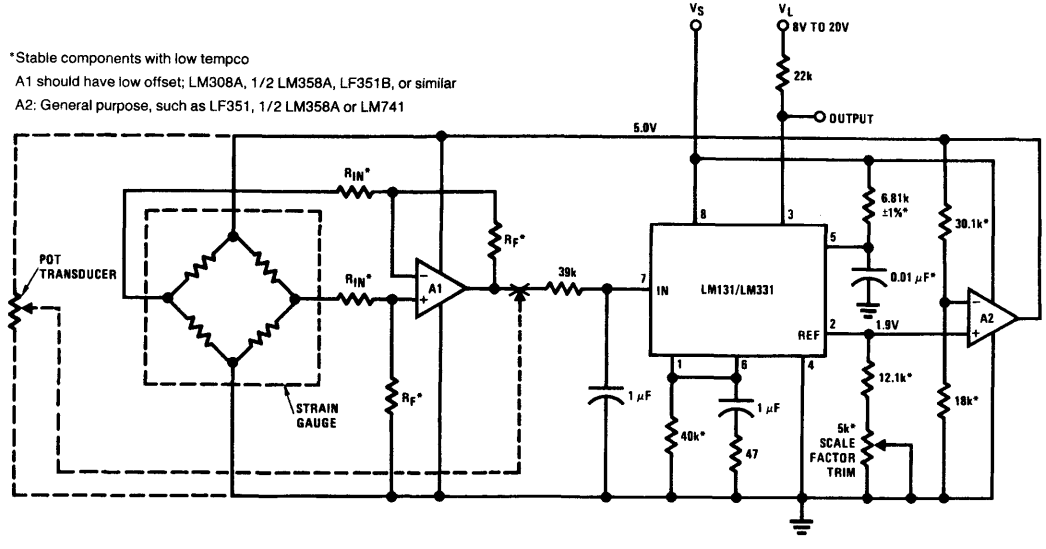
Frequency stability is typically ±25 ppm/°C, even with an LM331, which as a V/F converter is specified only to 150 ppm/°C maximum. From 20 Hz to 20 kHz, stability is excellent, and the circuit can generate frequencies up to 120 kHz.

Although the simplest way of using the reference output is to tie it back to the input, the reference can also be buffered and amplified to supply such external circuitry as a resistive transducer, which might be a strain gauge or a pot *(Figure 3)*. As in the stable oscillator already described, deviations of the internal reference voltage from the ideal cause the transducer's and the converter's sensitivities to change equally in opposite directions, so the effects cancel.

In this circuit, op amp A2 buffers and amplifies the constant voltage at pin 2 of the converter to provide the 5V excitation for the strain gauge. Amplifier A1, connected as an instrumentation amplifier, raises the output of the strain gauge to a usable level while rejecting common-mode pickup.

A potentiometer-type transducer works just as well with this circuit. Its wiper output takes the place of A1's output as shown at the X.

The reference terminal is both a constant voltage output and a current programming input. So far, it's been shown simply with one or two resistors going to ground. It is, however, a full-fledged signal input that accepts a signal from a current source quite well.



TL/H/8742-3

FIGURE 3. In this strain-to-frequency converter, the converter's reference excites the strain gauge (or the optional pot) through buffer amp A2. This makes the circuit insensitive to changes in the reference voltage.

This extra input is what enables the LM131 to compute while converting. For instance, it will convert the ratio of two voltages to a frequency proportional to the ratio *(Figure 4)*. The circuit is still a V/F converter, but has two signal inputs, both of them going to rather unorthodox places at that. The inputs, shown as voltages, are converted to currents by two current pumps (voltage-to-current converters). Of course, if currents of the proper ranges are available, the current pumps aren't needed. The left current pump, which includes Q1 and A1, determines how fast capacitor C_L discharges between output pulses. The other pump sets the current in the reference circuit to control the amount of recharge current when the one-shot fires. Tying the comparator input, pin 7, to the reference pin sets the comparator's trip point at a constant voltage.

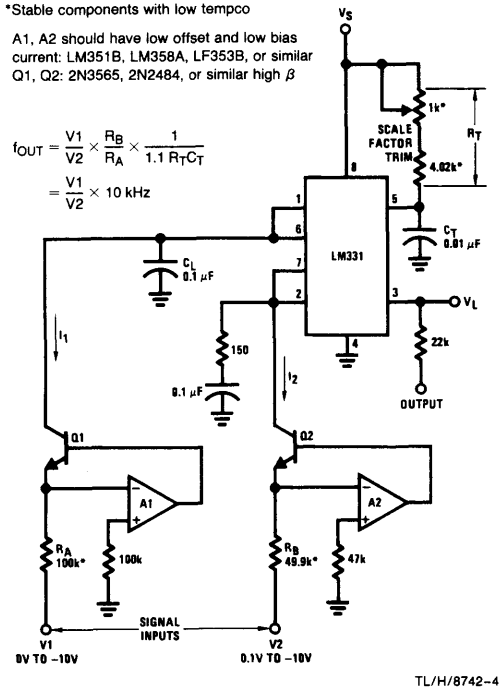


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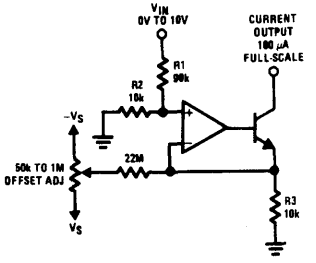
FIGURE 4. This circuit converts the ratio of two voltages to an equivalent frequency without a separate analog divider. Full-scale output is 15 kHz. The two op amp circuits convert the inputs to proportional currents.

To get an idea of how the circuit works, consider first the effect of, for instance, tripling the input voltage, V1. This make C_L discharge to the comparator trip point three times as fast, so the frequency triples. Next, consider a given change, such as doubling the voltage at the other input, V2. This doubles the recharge current to C_L during the fixed-width output pulse, which means C_L's voltage increases twice as much during recharging. Since the discharge into Q1 is linear (for V1 constant), it takes twice as long for C_L to discharge—the frequency becomes half of what it was before.

Although the current pumps in *Figure 4* must have negative inputs, rearranging the op amps according to *Figure 5* makes them accept positive inputs instead. Trimming out the offset in the op amp gives the ratio converter better linearity and accuracy. The trim circuit in *Figure 5a* needs stable positive and negative supplies for the offset trimmer, while the one in *Figure 5b* needs only a stable positive supply. Unmarked components in *Figure 5b* are the same as in *Figure 5a*.



a

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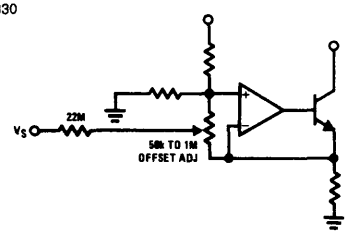
R1, R2, R3: Stable components with low tempco
Q1: $\beta \geq 330$



b

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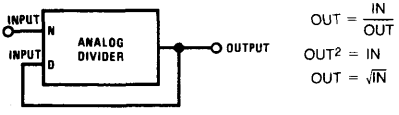
FIGURE 5. These current pumps adapt the converter circuits in *Figures 4* and *6* to positive input voltages. Optional offset trimming improves linearity and accuracy, especially with input signals that have a wide dynamic range.

Note that the full-scale range of the current pumps can be changed by varying the value of the input resistor(s). If either of these pump circuits is used with a single positive supply, the op amp should be a type such as 1/2 LM358 or 1/4 LM324, which has a common-mode range that includes the negative-supply bus.

COMPUTING SQUARE ROOTS IMPLICITLY

An analog divider computes the square root of a signal when the signal is fed to the divider's numerator input, and the output is fed back to the divider's denominator input.



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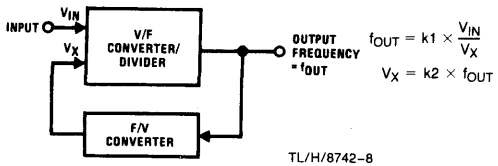
This type of computation is called implicit, because the end result of the computation is only implied, not explicitly stated by the equation that defines the computation.

In the implicit square root computing loop described in the text, a V/F converter serves as a divider. Since it's a converter, its inputs are voltages (or currents), but its output is a frequency. To connect its output back to one of its inputs so it will compute a square root means that its output frequency must be converted back to a voltage. This is taken care of by the frequency-to-voltage converter.



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Doing some algebraic substitution shows that:

$$f_{OUT} = k3 \times \sqrt{V_{IN}}$$

where

$$k3 = \sqrt{k1/k2}\,.$$

IT'LL TAKE RECIPROCALS

Taking the ratio of two inputs—in other words, doing division—is only one of the mathematical operations that can be combined with converting. Another one is a special case of division, which is taking reciprocals. In this instance, the numerator (V1 in *Figure 4*) is held constant, and the denominator, V2, changes over a wide range such as one or two decades. In this case, since the frequency is the reciprocal of the input, the period of the output is proportional to the input. When operated this way, the V2 current pump should have an offset trimmer. A constant current circuit is still needed to discharge capacitor C_L.

Nonlinearity (that is, deviation from the ideal law) with an LM331 is a little better than 1% for 10 kHz full-scale. Increasing C_T to 0.1 μF reduces the nonlinearity to below 0.2% while decreasing full-scale output to 1 kHz.

Two inputs can also be multiplied while converting to a frequency. The multiplying converter circuit *(Figure 6)* that does this has a more elaborate current pump than the ratio circuit of *Figure 4.* This pump is really two cascaded circuits; it includes op amps A2 and A3 as well as transistors Q2 and Q3. Current from this pump goes to pin 5 to control the one-shot's pulse width. (This current ranges from 13.3 μA to 1.33 mA.)

As in the ratio circuit, the left current pump controls the discharge rate of C_L. The other pump, however, controls the one-shot's pulse width to vary the amount that C_L charges during the pulse. If the V2 input is close to zero, the current from the pump into pin 5 is small, and the one-shot develops a wide pulse. This allows C_L to charge quite a bit. It takes a relatively long time for C_L to discharge to the comparator threshold, so the resulting frequency is low. As V2 goes negative (a greater absolute magnitude), the output frequency rises. Op amp A3 must have a common-mode range that extends to the positive supply voltage, which the specified types do.

Multiplying, dividing and converting can all be done at the same time by combining the V2 input current pump of *Figure 4* with the circuit of *Figure 6.* If a scale-factor trimmer is needed, R4 in *Figure 6* is a good choice, better than input resistors such as R1 or R2. Using the latter as trimmers would make the input impedance of the circuit change with trim setting.

Two V/F converter ICs along with some extra circuitry will take the square root of a voltage input. Square root functions are used mostly to simulate natural laws, but also to linearize functions that have a natural square-law relationship. One of the latter is converting diffential pressure to flow, where flow is proportional to the square root of differential pressure.

*Stable components with low tempco

$f_{OUT} = \frac{V1}{10V} \times \frac{V2}{10V} \times 10\ kHz$

V_S = 15V, regulated and stable

$R3 = \left(\frac{15.00V}{+V_S}\right) \times 750\Omega$ with ±1% tolerance

A1, A2: Each is 1/2 LM158/LM358A or 1/2 LF353B

A3: LM301A, LM307, or LF13741 only

Q1, Q2: High β such as 2N2484, 2N3565 or similar

Q3: High β such as 2N4250, 2N3906 or similar

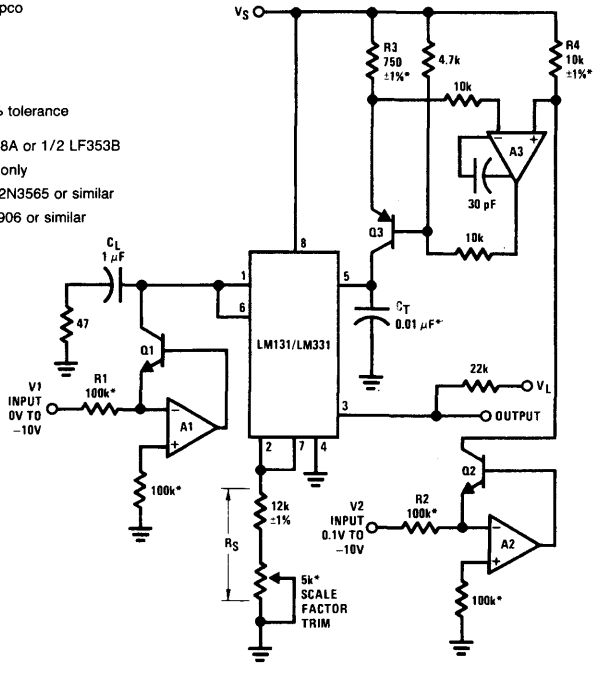

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FIGURE 6. The product of two input voltages becomes an equivalent frequency in this converter. A current pump that includes op amps A2 and A3 controls the pulse duration of the converter's internal one-shot.

VERSATILE PIN FUNCTIONS GIVE DESIGN FLEXIBILITY

Two features—the reference and the one-shot—of the LM131/LM331 V/F converter deserve a closer look because they are the key to its versatility. The simplified schematic of the chip, shown here along with a transducer and the components needed for a basic V/F converter, will help to illustrate how these features work.

The reference circuit, connected to pin 2, is both a constant voltage output and a current setting, scale-factor control input. The constant voltage can supply external circuitry, such as the transducer, that feeds the converter's input.

One great advantage of using the converter's internal reference to supply the external circuitry is that any variation in the reference voltage affects the sensitivities of the converter and the external circuitry by equal and opposite amounts, so the effects of the variation cancel.

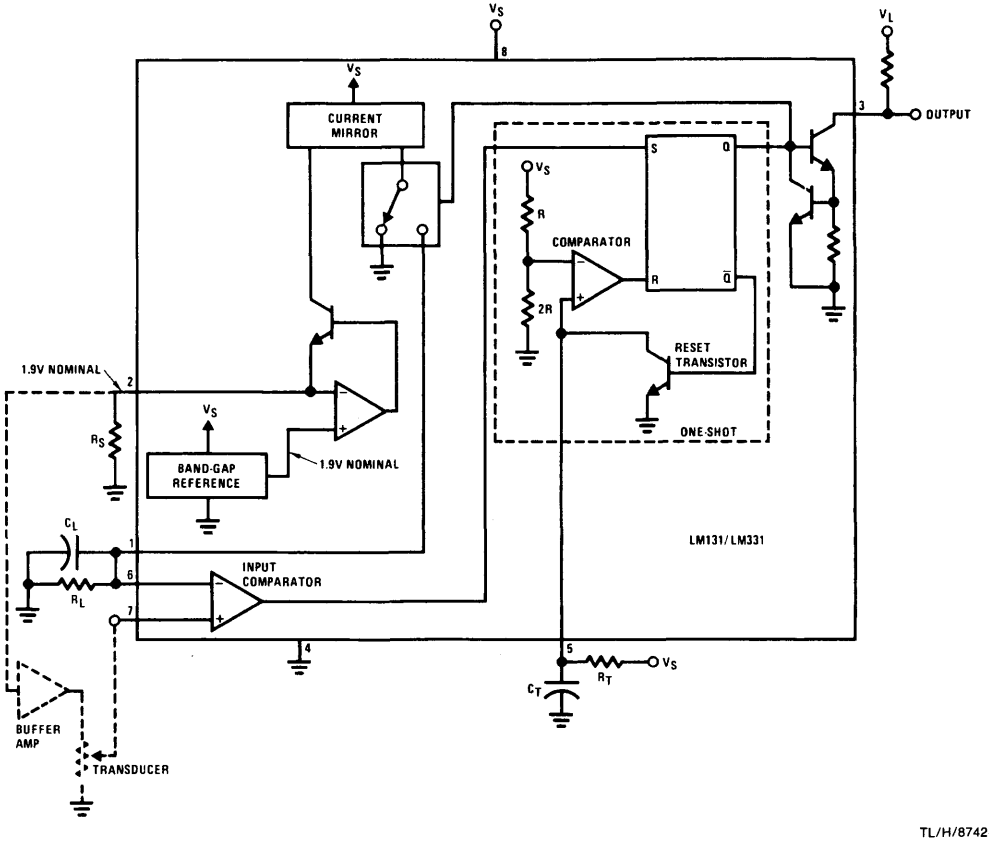
While providing a constant voltage output, pin 2 also provides scale-factor, or sensitivity control for the converter. Current supplied to an external circuit by this terminal comes from the supply (V_S) through the current mirror and the transistor. The op amp drives this transistor to hold pin 2 at a constant voltage equal to the internal reference, which is nominally 1.9V.

The current mirror provides a current to the switch that's essentially identical to that in pin 2. This means that a resistor to ground or a signal from a current source will set the current that is switched to pin 1. In most circuits, a capacitor goes from pin 1 to ground, and the switched current from this pin recharges the capacitor during the pulse from the one-shot.

The one-shot circuit is somewhat like the well known 555 timer's circuit. In the quiescent state, the reset transistor is on and holds pin 5 near ground. When pin 7 becomes more positive than pin 6 (or pin 6 falls below pin 7), the input comparator sets the flip-flop in the one-shot.

The flip-flop turns on the current limited output transistor (pin 3) and switches the current coming from the current mirror to pin 1. The flip-flop also turns off the reset transistor, and the timing capacitor C_T starts to charge toward V_S. This charge is exponential, and C_T's voltage reaches 2/3 of V_S in about 1.1 R_TC_T time constants. (The quantity 1.1 is $-\ln 0.333...$) When pin 5 reaches this voltage, the one-shot's comparator resets the flip-flop which turns off the current to pin 1, discharges C_T, and turns off the output transistor.

If the voltages at pins 6 and 7 still call for setting the flip-flop after pin 5 has reached 2/3 V_S, internal logic not shown in this simplified diagram overrides the reset signal from the one-shot's own comparator, and the flip-flop stays set. In this instance, C_T continues charging past 2/3 V_S.



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ROOT LOOP COMPUTES

The circuit in *Figure 7* is an implicit loop (see "Computing Square Roots Implicitly") that uses IC1 as a voltage-to-frequency converter and divider, and IC2 as a frequency-to-voltage converter. The F/V converter, IC2, and the current pump that includes A1 and the transistor return the output of IC1 to its denominator input. A relatively elaborate feedback circuit like this is needed to convert IC1's frequency output back to a current for its denominator input.

Looking at the circuit in more detail, IC1 puts out a frequency proportional to V_{IN} divided by the feedback voltage, V_X. The current I_1 is generated by a current pump that has V_X as its input *(Figure 5a)*. To develop the feedback IC2 converts the pulse output from IC1 into standard width precision current pulses that charge capacitor C1. This capacitor integrates them into the voltage V_X, thus closing the loop.

Op amp A2, serving as a comparator, ensures that the circuit will always start and continue running. If V_{IN} suddenly jumps to a higher voltage, one pulse from the one-shot in IC1 may not be enough to recharge C_L to a voltage higher than the input. In such a case, the IC's internal logic keeps its internal current switch turned on, and the voltage on C_L ramps up until it exceeds the input. During this time, however, IC1's output hasn't changed state. (Such a temporary hang-up isn't unique to this circuit, and equivalent things happen to other V/Fs besides the LM131/LM331.) What is worse here, though, is that the lack of pulses to IC2 means that V_X and I_1 decay. The recharging current, I_2, is the same as I_1, so it not only becomes progressively harder for the voltage on C_L to catch up with the input, it may even fail to catch up entirely if ($I_2 \times R_L$) is less than the input voltage.

As a sign of this condition, when the converter hangs up, the one-shot's timing node, pin 5, continues to charge well beyond its normal peak of 2/3 V_S. As soon as the comparator A2 detects this rise, it pulls up voltage V_X, current I_1 increases, and the loop catches its breath again.

After all these nonlinear computations, this last circuit is about as linear as it can be. It's a precision, ultralinear V/F converter based on an LM331A *(Figure 8)* that has several detail refinements over previous V/F converter circuits. Choosing the proper components and trimming the tempco give less than 0.02% error and 0.003% nonlinearity for a ±20°C range around room temperature.

This circuit has an active integrator, which includes the op amp and the integrating feedback capacitor, C_F. The integrator converts the input voltage, which is negative, into a positive-going ramp. When the ramp reaches the converter IC's comparator threshold, the one-shot fires and switches a pulse of current to the integrator's summing junction. This current makes the integrator's output ramp down quickly. When the one-shot times out, the cycle repeats.

There are several reasons this converter circuit gives high performance:

- A feedback limiter prevents the op amp from driving pin 7 of the LM331A negative. The limiter circuit arrangement bypasses the leakage through CR5 to ground via R5, so it won't reach the summing junction. Bypassing leakage this way is especially important at high temperatures.
- The offset trimming pot is connected to the stable 1.9V reference at pin 2 instead of to a power supply bus that might be unstable and noisy.

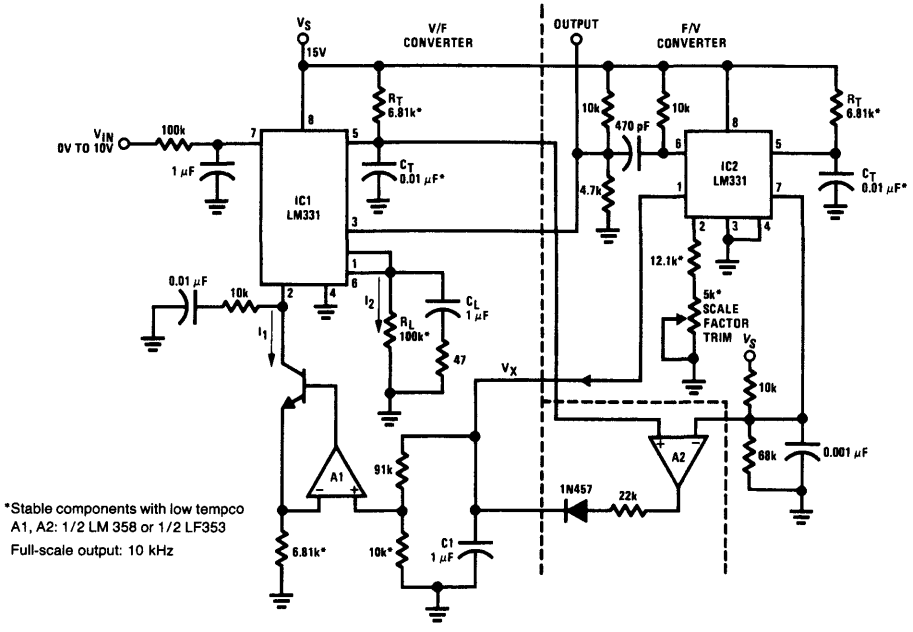

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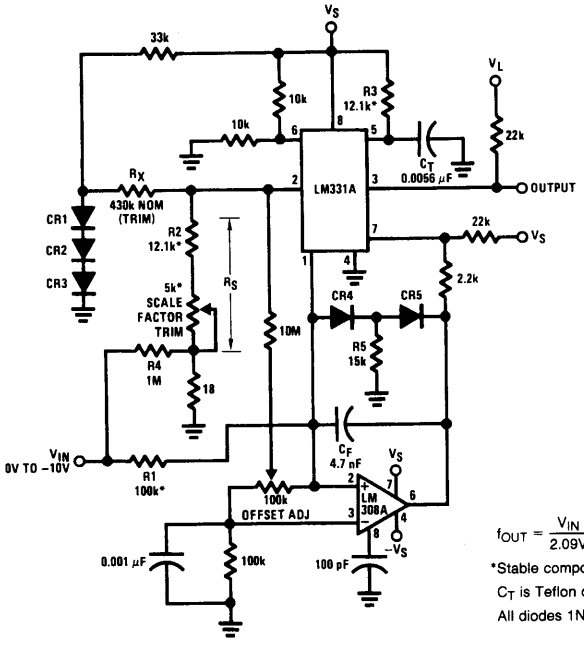
FIGURE 7. Two converter ICs generate an output frequency proportional to the square root of the input voltage. The circuit is an implicit loop in which IC1 serves as a divider and V/F converter. This IC's output goes back to its denominator input through F/V converter IC2 to make the circuit output equal the input's square root.



$$f_{OUT} = \frac{V_{IN}}{2.09V} \times \frac{R_S}{R1} \times \frac{1}{R_3 C_T}$$ Full-scale output 10 kHz

*Stable components with low tempco; see text

C_T is Teflon or Polystyrene

All diodes 1N457, 1N484, or FD333 (low-leakage silicon)

TL/H/8742–12

FIGURE 8. An ultraprecision V/F converter, capable of better than 0.02% error and 0.003% nonlinearity for a ±20°C range about room temperature, augments the basic converter with an external integrator.

- A small fraction (180 μV, full-scale) of the input voltage goes via R4 to the R_S network, which improves the nonlinearity from 0.004% to 0.002%.
- Resistors R2 and R3 are the same value, so that resistors such as Allen-Bradley type CC metal-film types can provide excellent tempco tracking at low cost. (This tracking is very good when equal values come from the same batch.) Resistor R1 should be a low tempco metal-film or wirewound type, with a maximum tempco of ±10 ppm/°C or ±25 ppm/°C.

In addition, C_T should be a polystyrene or Teflon type. Polystyrene is rated to 80°C, while Teflon goes to 150°C. Both types can be obtained with a tempco of −110 ±30 ppm/°C. Choosing this tempco for C_T makes the tempco, due to C_T, of the full-scale output frequency 110 ppm/°C.

Using tight tolerance components results in a total tempco between 0 ppm/°C and 220 ppm/°C, so the tempco will never be negative. The voltage at CR1 and R_X has a tempco of −6 mV/°C, which can be used to compensate the tempco of the rest of the circuit. Trimming R_X compensates for the tempco of the V/F IC, the capacitor, and all the resistors.

A good starting value for selecting R_X is 430 kΩ, which will give the 135 μA flowing out of pin 2 a slope of 110 ppm/°C. If the output frequency increases with temperature, a little more conductance should be added in parallel with R_X.

When doing a second round of trimming, though, note that a resistor of, say, 4.3 MΩ, has about the same effect on tempco when shunted across a 220 kΩ resistor that it does when shunted across one of 430 kΩ, namely, −11 ppm/°C. This technique can give tempcos below ±20 ppm/°C or even ±10 ppm/°C.

Some precautions help this procedure converge:

1. Use a good capacitor for C_T. The cheapest polystyrene capacitors will shift in value by 0.05% or more per temperature cycle. The actual temperature sensitivity would be indistinguishable from the hysteresis, and the circuit would never be stable.
2. After soldering, bake and/or temperature-cycle the circuit (at a temperature not exceeding 75°C if C_T is polystyrene) for a few hours, to stabilize all components and to relieve the strains from soldering.
3. Don't rush the trimming. Recheck the room temperature value, before and after the high temperature data are taken, to ensure that hysteresis per cycle is reasonably low.
4. Don't expect a perfect tempco at −25°C if the circuit is trimmed for ±5 ppm/°C between 25°C and 60°C. If it's been trimmed for zero tempco while warm, none of its components will be linear to much better than 5 ppm/°C or 10 ppm/°C when it's cold.

The values shown in this circuit are generally optimum for ±12V to ±16V regulated supplies but any stable supplies between ±4V and ±22V would be usable, after changing a few component values.

National Semiconductor

APPENDIX H: Standard Resistance Values

The standard 1% (and ½%) resistor values are recommended for ease of design and for best availability when designing precision analog circuits.

Standard Resistance Values for the 10-to-100 Decade

Resistance Tolerance (+%)																		
0.1			0.1			0.1			0.1			0.1			0.1		
0.25	1	2	0.25	1	2	0.25	1	2	0.25	1	2	0.25	1	2	0.25	1	2
0.5		5	0.5		5	0.5		5	0.5		5	0.5		5	0.5		5
10.0	**10.0**	10	14.7	**14.7**	—	21.5	**21.5**	—	31.6	**31.6**	—	46.4	**46.4**	—	68.1	**68.1**	68
10.1	—	—	14.9	—	—	21.8	—	—	32.0	—	—	47.0	—	47	69.0	—	—
10.2	**10.2**	—	15.0	**15.0**	15	22.1	**22.1**	—	32.4	**32.4**	—	47.5	**47.5**	—	69.8	**69.8**	—
10.4	—	—	15.2	—	—	22.3	—	22	32.8	—	—	48.1	—	—	70.6	—	—
10.5	**10.5**	—	15.4	**15.4**	—	22.6	**22.6**	—	33.2	**33.2**	33	48.7	**48.7**	—	71.5	**71.5**	—
10.6	—	—	15.6	—	—	22.9	—	—	33.6	—	—	49.3	—	—	72.3	—	—
10.7	**10.7**	—	15.8	**15.8**	—	23.2	**23.2**	—	34.0	**34.0**	—	49.9	**49.9**	—	73.2	**73.2**	—
10.9	—	—	16.0	—	16	23.4	—	—	34.4	—	—	50.5	—	—	74.1	—	—
11.0	**11.0**	11	16.2	**16.2**	—	23.7	**23.7**	—	34.8	**34.8**	—	51.1	**51.1**	51	75.0	**75.0**	75
11.1	—	—	16.4	—	—	24.0	—	24	35.2	—	—	51.7	—	—	75.9	—	—
11.3	**11.3**	—	16.5	**16.5**	—	24.3	**24.3**	—	35.7	**35.7**	—	52.3	**52.3**	—	76.8	**76.8**	—
11.4	—	—	16.7	—	—	24.6	—	—	36.1	—	36	53.0	—	—	77.7	—	—
11.5	**11.5**	—	16.9	**16.9**	—	24.9	**24.9**	—	36.5	**36.5**	—	53.6	**53.6**	—	78.7	**78.7**	—
11.7	—	—	17.2	—	—	25.2	—	—	37.0	—	—	54.2	—	—	79.6	—	—
11.8	**11.8**	—	17.4	**17.4**	—	25.5	**25.5**	—	37.4	**37.4**	—	54.9	**54.9**	—	80.6	**80.6**	—
12.0	—	12	17.6	—	—	25.8	—	—	37.9	—	—	56.6	—	—	81.6	—	—
12.1	**12.1**	—	17.8	**17.8**	—	26.1	**26.1**	—	38.3	**38.3**	—	56.2	**56.2**	56	82.5	**82.5**	82
12.3	—	—	18.0	—	18	26.4	—	—	38.8	—	—	56.9	—	—	83.5	—	—
12.4	**12.4**	—	18.2	**18.2**	—	26.7	**26.7**	—	39.2	**39.2**	39	57.6	**57.6**	—	84.5	**84.5**	—
12.6	—	—	18.4	—	—	27.1	—	27	39.7	—	—	58.3	—	—	85.6	—	—
12.7	**12.7**	—	18.7	**18.7**	—	27.4	**27.4**	—	40.2	**40.2**	—	59.0	**59.0**	—	86.6	**86.6**	—
12.9	—	—	18.9	—	—	27.7	—	—	40.7	—	—	59.7	—	—	87.6	—	—
13.0	**13.0**	13	19.2	**19.1**	—	28.0	**28.0**	—	41.2	**41.2**	—	60.4	**60.4**	—	88.7	**88.7**	—
13.2	—	—	19.3	—	—	28.4	—	—	41.7	—	—	61.2	—	—	89.8	—	—
13.3	**13.3**	—	19.6	**19.6**	—	28.7	**28.7**	—	42.2	**42.2**	—	61.9	**61.9**	62	90.9	**90.9**	91
13.5	—	—	19.8	—	—	29.1	—	—	42.7	—	—	62.6	—	—	92.0	—	—
13.7	**13.7**	—	20.0	**20.0**	20	29.4	**29.4**	—	43.2	**43.2**	43	63.4	**63.4**	—	93.1	**93.1**	—
13.8	—	—	20.3	—	—	29.8	—	—	43.7	—	—	64.2	—	—	94.2	—	—
14.0	**14.0**	—	20.5	**20.5**	—	30.1	**30.1**	30	44.2	**44.2**	—	64.9	**64.9**	—	95.3	**95.3**	—
14.2	—	—	20.8	—	—	30.5	—	—	44.8	—	—	65.7	—	—	96.5	—	—
14.3	**14.3**	—	21.0	**21.0**	—	30.9	**30.9**	—	45.3	**45.3**	—	66.5	**66.5**	—	97.6	**97.6**	—
14.5	—	—	21.3	—	—	31.2	—	—	45.9	—	—	67.3	—	—	98.8	—	—

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 12.1 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21 kΩ, etc.