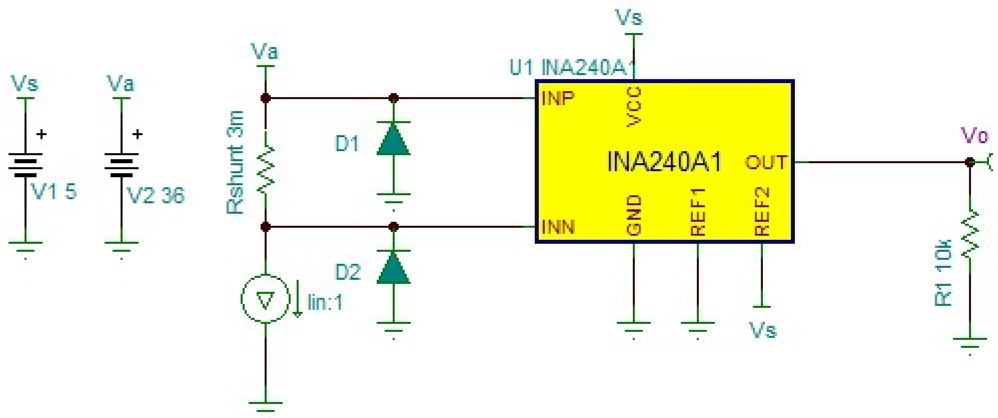
High-side, bidirectional current-sensing circuit with transient protection

Design Goals

Input		Output		Supply			Standoff and Clamp Voltages		EFT Level
I_{inMin}	I_{inMax}	V_{oMin}	V_{oMax}	Vs	GND	V_{ref}	Vwm	Vc	Vpp
–40A	40A	100mV	4.9V	5V	0V	2.5V	36V	80V	2kV 8/20µs

Design Description

This high-side, bidirectional current sensing solution can accurately measure current in the range of –40A to 40A for a 36-V voltage bus. The linear voltage output is 100mV to 4.90V. This solution is also designed to survive IEC61000-4-4 level 4 EFT stress (Voc = 2kV; Isc = 40A; 8/20µs).



Design Notes

1. This solution is targeted toward high-side current sensing.
2. The sense resistor value is determined by minimum and maximum load currents, power dissipation and Current Shunt Amplifier (CSA) gain.
3. Bidirectional current sensing requires an output reference voltage (Vref). Device gain is achieved through internal precision matched resitor network.
4. The expected maximum and minimum output voltage must be within the device linear range.
5. The TVS diode must be selected based on bus voltage, the CSA common-mode voltage specification, and EFT pulse characteristics.

Design Steps

1. Determine the maximum output swing:

   $$VswN = Vref - VoMin = 2.5V - 0.1V = 2.4V$$

   $$VswP = VoMax - Vref = 4.9V - 2.5V = 2.4V$$

2. Determine the maximum value of the sense resistor based on maximum load current, swing and device gain. In this example, a gain of 20 was chosen to illustrate the calculation, alternative gain versions may be selected as well:

   $$Rshunt \le \frac{Vswp}{Iin\_max \times Gain} = \frac{2.4V}{40A \times 20} = 3m\Omega$$

3. Calculate the peak power rating of the sense resistor:

   $$Pshunt = Iin\_max^2 \times Rshunt = 40A^2 \times 3m\Omega = 5W$$

4. Determine TVS standoff voltage and clamp voltage:

   $$Vwm = 36V \quad \text{and} \quad Vc \le 80V$$

5. Select a TVS diode.

   For example, SMBJ36A from Littelfuse™ satisfies the previous requirement, with peak pulse power of 600W (10/1000µs) and current of 10.4A.

6. Make sure the TVS diode satisfies the design requirement based on the TVS operating curve.

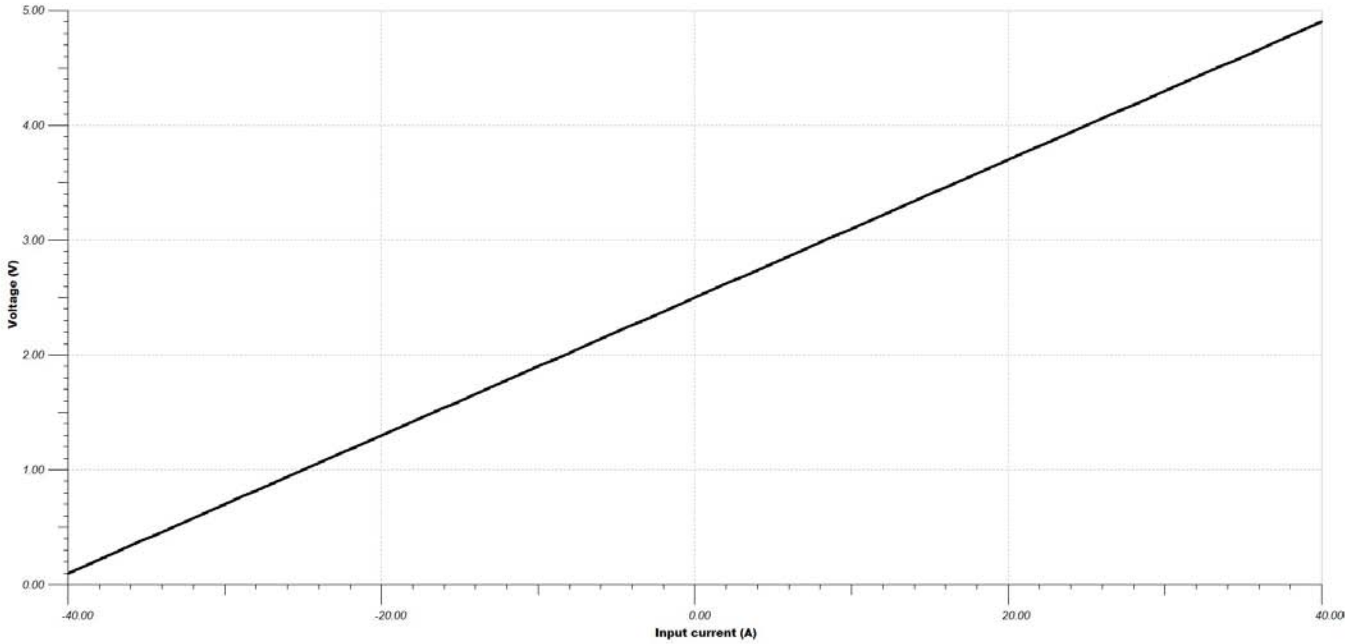
   Peak pulse power at given excitation (8/20µs) is estimated to be around 3.5kW, which translates to peak pulse current:

   $$Ipp = \frac{3.5kW}{600W} \times 10.4A = 60A$$

This is above the maximum excitation (short circuit) current of 40A. The select TVS effectively protects the circuit against the specified EFT strike.

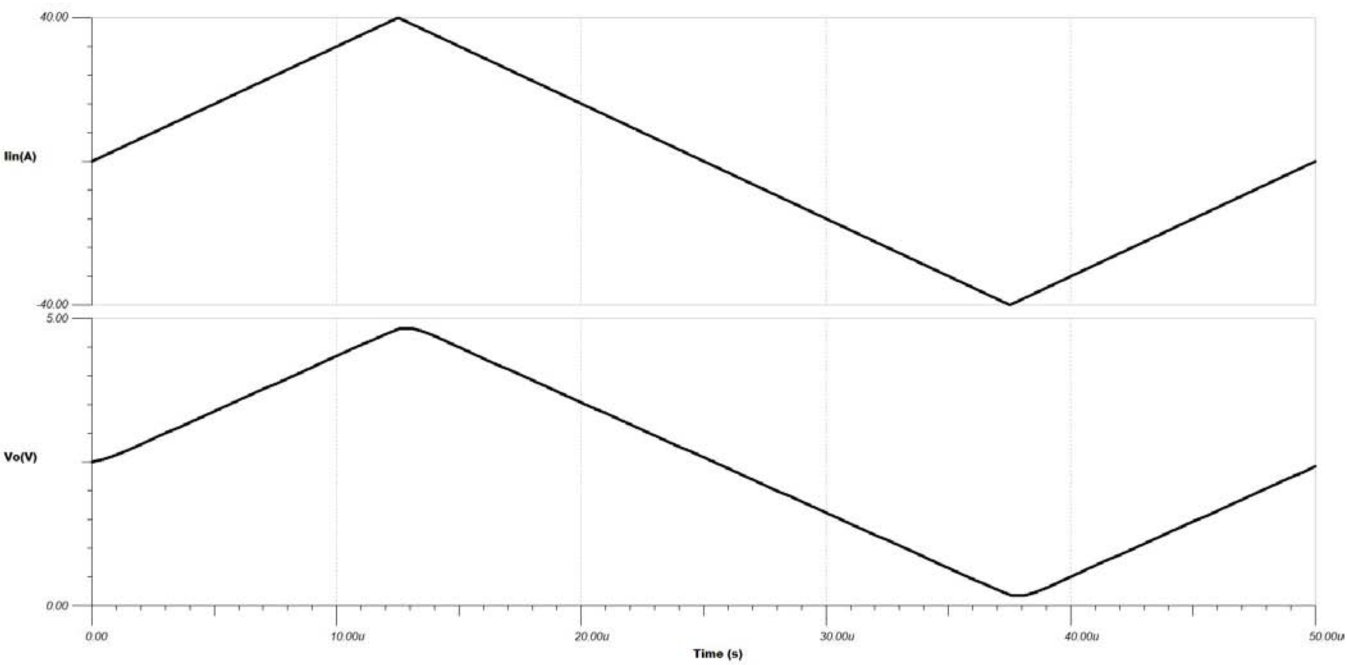
Design Simulations

DC Transfer Characteristics

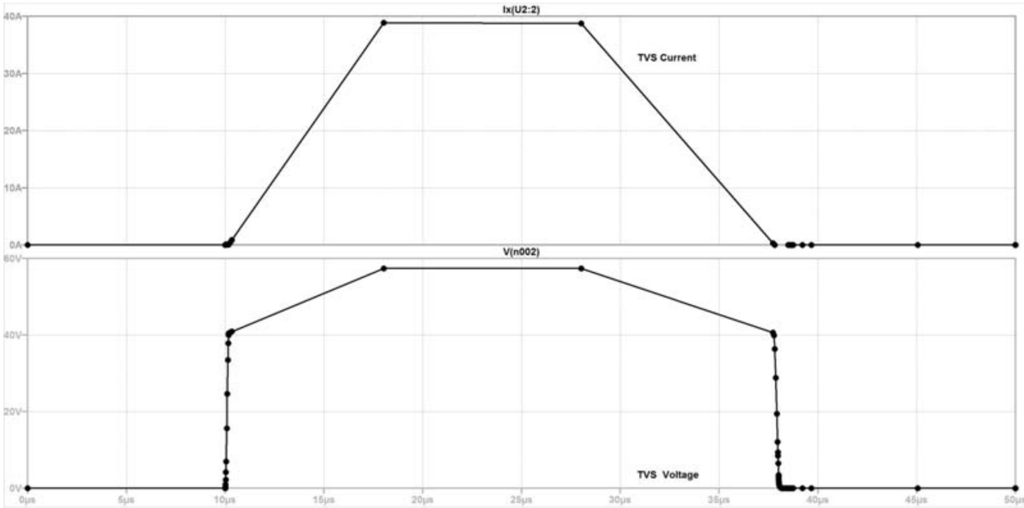


Transient Simulation Results

The output is a scaled version of the input.



TVS Diode Transient Response Under EFT Excitation



Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

For more information on transient protection of the current sense amplifiers, see TIDA-00302 and the Current Sense Amplifier Training Videos.

Design Featured Current Sense Amplifier

INA240A1	
V_s	2.7V to 5.5V
V_{CM}	–4V to 80V
V_{os}	Rail-to-rail
V_{os}	5µV
I_B	80µA
BW	400kHz
Vos Drift	50nV/°C
http://www.ti.com/product/INA240	

Design Alternate

INA282	
V_s	2.7V to 18V
V_{CM}	–14V to 80V
V_{os}	20µV
I_B	25µA
BW	10kHz
Vos Drift	0.3µV/°C
http://www.ti.com/product/INA193	

Revision History

Revision	Date	Change
A	February 2019	Changed VinMin and VinMax in the Design Goals table to IinMin and IinMax, respectively.

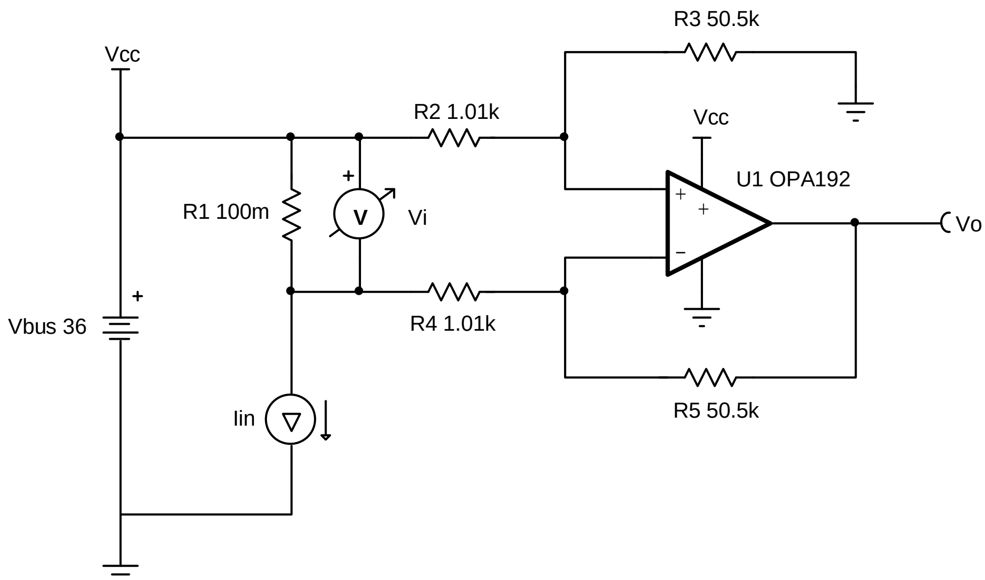
High-side current-sensing circuit design

Design Goals

Input		Output		Supply	
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
50mA	1A	0.25V	5V	36V	0V

Design Description

This single–supply, high–side, low–cost current sensing solution detects load current between 50mA and 1A and converters it to an output voltage from 0.25V to 5V. High–side sensing allows for the system to identify ground shorts and does not create a ground disturbance on the load.



Design Notes

1. DC common mode rejection ratio (CMRR) performance is dependent on the matching of the gain setting resistors, R_2-R_5.
2. Increasing the shunt resistor increases power dissipation.
3. Ensure that the common–mode voltage is within the linear input operating region of the amplifier. The common mode voltage is set by the resistor divider formed by R_2, R_3, and the bus voltage. Depending on the common–mode voltage determined by the resistor divider a rail–to–rail input (RRI) amplifier may not be required for this application.
4. An op amp that does not have a common-mode voltage range that extends to V_{cc} may be used in low–gain or an attenuating configuration.
5. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability, and help reduce noise.
6. Use the op amp in a linear output operating region. Linear output swing is usually specified under the A_{OL} test conditions.

Design Steps

1. The full transfer function of the circuit is provided below.

   $$V_o = I_{in} \times R_1 \times \frac{R_5}{R_4}$$

   Given $R_2 = R_4$ and $R_3 = R_5$

2. Calculate the maximum shunt resistance. Set the maximum voltage across the shunt to 100mV.

   $$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{100mV}{1A} = 100m\Omega$$

3. Calculate the gain to set the maximum output swing range.

   $$Gain = \frac{V_{oMax} - V_{oMin}}{(I_{iMax} - I_{iMin}) \times R_1} = \frac{5V - 0.25V}{(1A - 0.05A) \times 100m\Omega} = 50\frac{V}{V}$$

4. Calculate the gain setting resistors to set the gain calculated in step 3.

   Choose $R_2 = R_4 = 1.01k\Omega$ (Standard value)

   $$R_3 = R_5 = R_2 \times Gain = 1.01k\Omega \times 50\frac{V}{V} = 50.5k\Omega \text{ (Standard value)}$$

5. Calculate the common–mode voltage of the amplifier to ensure linear operation.

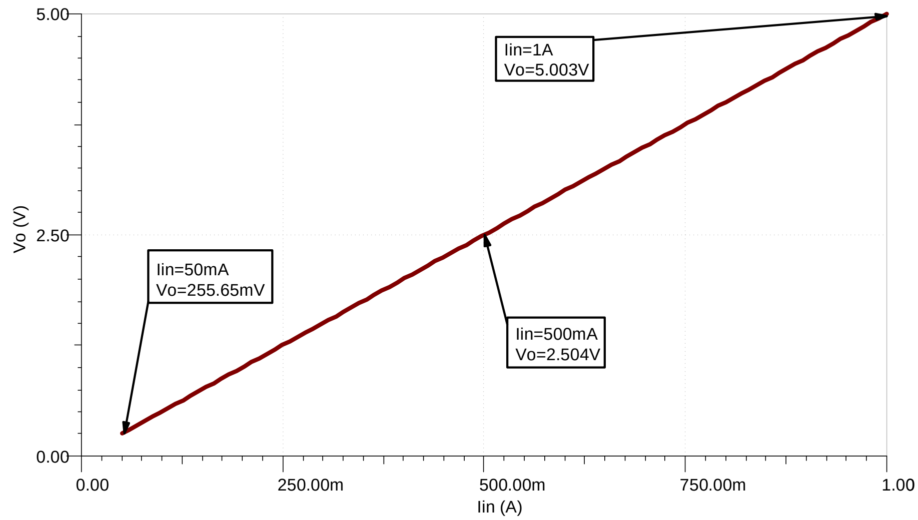
   $$V_{cm} = V_{CC} \times \frac{R_3}{R_2 + R_3} = 36V \times \frac{50.5k}{1.01k + 50.5k} = 35.294\ V$$

6. The upper cutoff frequency (f_H) is set by the non–inverting gain (noise gain) of the circuit and the gain bandwidth (GBW) of the op amp.

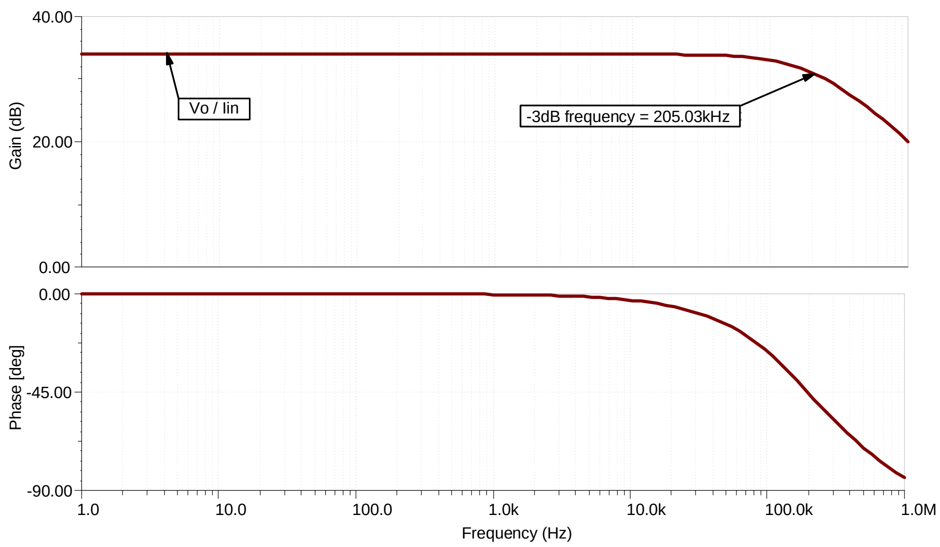
   $$f_H = \frac{GBW}{Noise\ Gain} = \frac{10MHz}{51\frac{V}{V}} = 196.1\ kHz$$

Design Simulations

DC Simulation Results



AC Simulation Results



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOMAV4
3. TI Precision Labs

Design Featured Op Amp

OPA192	
V_{cc}	4.5V to 36V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	5µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/OPA192	

Design Alternate Op Amp

OPA2990	
V_{cc}	2.7V to 40V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	250µV
I_q	120µA
I_b	10pA
UGBW	1.25MHz
SR	5V/µs
#Channels	2
www.ti.com/product/OPA2990	

Revision History

Revision	Date	Change
A	February 2019	Downstyle title. Added Design Alternate Op Amp table.