Simple circuit controls the rate of voltage change across a capacitor or another load

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The circuit in this Design Idea lets you set a well-controlled voltage rate of change, often expressed as the differential dV/dt (instantaneous rate of voltage change over time in volts per second). You can vary the sensitivity with a potentiometer. Set the dV/dt from 1V/200 nsec to 1V/3 msec. The input voltage can range from a few volts to 30V. Higher-voltage transistors can be used to increase the upper voltage limit. The circuit precharges a capacitor with a slow and controllable dV/dt to avoid a large inrush current during power-up. You can also use the circuit to create a high dV/dt for susceptibility testing on other circuits.

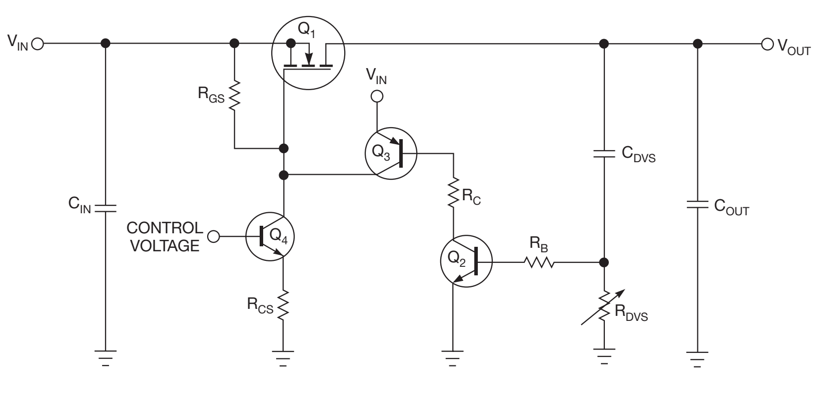

Figure 1 This circuit creates a fixed dV/dt based on the control voltage and the setting of R_{DVS}.

The circuit uses a P-channel MOSFET, Q_1, to control the rate of change of the output voltage (**Figure 1**). You drive the MOSFET with a constant-current source comprising Q_4 and R_{CS}, which feeds gate-to-source resistor R_{GS}. Applying a positive control voltage to the base of Q_4 draws a current that creates a voltage across R_{GS}. This voltage occurs across the gate and source of Q_1, turning it on. The circuit uses capacitor C_{DVS} as a sensing device of the rate of change of the output voltage. Voltage variations across C_{DVS} generate a current that creates a current proportional to the dV/dt, as the following **equation** shows:

$$I_{CS}=C_{DVS}\times\frac{dV_{OUT}(t)}{dt}.$$

Resistor R_{DVS} converts this current into a voltage signal. When that voltage reaches approximately 0.67V, it turns on Q_2, which turns on Q_3. The current that Q_3 supplies from the input tends to lower the Q_1 gate-to-source voltage and reduces its drive. You use R_B to limit the base current of Q_2. This servo action puts the gate-to-source voltage of the MOSFET in the Miller plateau, a constant-current region of the FET's characteristic curve. The FET has an internal Miller capacitance, C_{GD}, between the gate and the drain pins.

TABLE 1 CIRCUIT PART NUMBERS

Component	Description	Manufacturer	Part no.
C_{IN}	10-µF, 50V tantalum capacitor	AVX	TPSE106K050R0500
C_{OUT}	1-µF, 50V ceramic capacitor	AVX	12065C105KAT2A
C_{DVS}	10-nF, 50V ceramic capacitor	AVX	08055C103KAT2A
Q_2 and Q_4	40V, 0.6A NPN transistor	On Semiconductor	MMBT2222ALT1G
Q_3	60V, 1.2A PNP transistor	On Semiconductor	MMBT2907ALT1G
Q_1	100V, 4A power MOSFET	Vishay	IRF9510SPBF
R_B	1-kΩ, 0603, 1% resistor	Vishay	CRCW12061K00FKEA
R_C	1-kΩ, 0603, 1% resistor	Vishay	CRCW12061K00FKEA
R_{CS}	10-kΩ, 0603, 1% resistor	Vishay	CRCW120610K0FKEA
R_{DVS}	10-kΩ trimming potentiometer	Bourns	3362W-1-503LF
R_{GS}	10-kΩ, 0603, 1% resistor	Vishay	CRCW120610K0FKEA

The circuit's constant-current source controls the charge current of this Miller capacitance. As transistor Q_3 injects current to the gate, Miller current I_{GD} decreases and the slope of the output voltage decreases accordingly, as the following **equation** shows:

$$\frac{dV_{dS}(t)}{dt} = \frac{I_{GD}}{C_{GD}}.$$

The feedback loop keeps the dV/dt ratio constant. The rate of change of the output voltage is a function of the base-emitter voltage of Q_2, R_{DVS}, and C_{DVS}, as the following **equation** shows:

$$\frac{dV_{OUT}(t)}{dt} \simeq \frac{V_{BEQ1}}{R_{VDS} \times C_{DVS}}.$$

You can build the circuit with the part numbers in **Table 1**.EDN