How to Design an Isolated, High Frequency, Push-Pull DC/DC Converter

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A simple push-pull DC/DC converter with a fixed 50% duty cycle is often used as a low noise transformer driver in communication systems, medical instruments and distributed power supplies. This simple scheme provides no voltage regulation—requiring a low dropout (LDO) post regulator—a combination that presents potentially serious problems. First, any significant variation in the driver's input voltage, along with the fixed 50% duty cycle, can increase the differential voltage across the LDO, resulting in significant power losses and high temperature rise in the LDO. Second, low switching frequency requires relatively bulky transformers, sometimes occupying 30% to 50% of the converter space.

The LT3999 monolithic DC/DC push-pull driver avoids these issues with two important features: duty cycle control and high frequency operation:

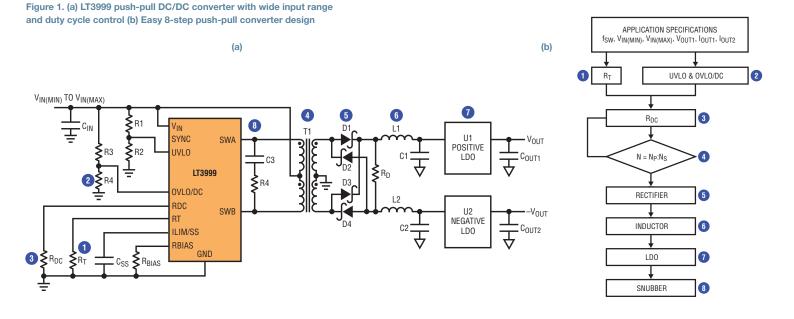
- *Duty cycle control* allows compensation for wide V_{IN} variation—something standard fixed duty cycle transformer drivers cannot do—greatly reducing LDO loss when facing a wide input range.
- *High switching frequency*, up to 1MHz, leads to smaller transformers and lower output ripple.

The LT3999 combines these two features with high 36V input voltage and 1A input current capabilities, making it a high power and flexible low noise push-pull converter IC.

This article presents two step-bystep design procedures: One for a push-pull DC/DC converter with a wide input range, the other for a compact high frequency transformer driver with fixed input voltage.

PUSH-PULL DC/DC CONVERTER DESIGN FOR WIDE RANGING INPUT

The flowchart in Figure 1b shows how a push-pull converter can be designed in eight simple steps. These steps produce the LT3999 10V-15V input, ±12V output, 200mA 1MHz pushpull converter shown in Figure 1a.



The LT3999 is a monolithic DC/DC transformer driver, which features duty cycle control, high frequency and high power. It allows a wide input voltage range and low loss at the LDO, while using small passive components due to the high frequency operation. It also features input voltage up to 36V and input current up to 1A.

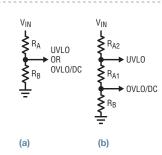


Figure 2. Setting the precision UVLO and OVLO/ DC via resistor divider using either (a) a 2-resistor method or (b) a 3-resistor method.

Step 1: Set the Switching Frequency (R_T)

First, set the switching frequency with R_T ; the value chosen from Table 1 in the LT3999 data sheet.

 $R_T = 12.1k$ sets $f_{SW} = 1MHz$.

Step 2: Set the Input Voltage Range (UVLO, OVLO/DC)

The UVLO (undervoltage lockout) and OVLO/DC (overvoltage lockout/ duty cycle) pins are used to set input voltage range. Either a 2- or 3-resistor method can be used. For the 2-resistor method shown in Figure 2a, R_B is calculated using equations 1 and 2 for UVLO and OVLO/DC, respectively. For low loss, we can assume $R_A = 1M\Omega$.

For UVLO:

$$R_{B(UVLO)} = \frac{R_{A}}{\left(\frac{V_{IN(MIN)}}{1.25} - 1\right)}$$
(1)
For UVLO:

$$R_{B(OVLO)} = \frac{R_{A}}{\left(\frac{V_{IN(MAX)}}{1.25} - 1\right)}$$
(2)

For the 3-resistor method shown in Figure 2b, R_{A1} and R_B are

calculated by equations 3 and 4 for UVLO and OVLO/DC, respectively. R_{A2} can be chosen around 1M Ω .

$$R_{A1} = R_{A2} \frac{\left(1 - \frac{V_{IN(MIN)}}{V_{IN(MAX)}}\right)}{\left(\frac{V_{IN(MIN)}}{1.25} - 1\right)}$$
(3)
$$R_{B} = R_{A2} \frac{\left(\frac{V_{IN(MIN)}}{V_{IN(MAX)}}\right)}{\left(\frac{V_{IN(MIN)}}{1.25} - 1\right)}$$
(4)

For the 2-resistor method used in Figure 1a:

 $V_{IN(MIN)} = 10V, R_A = 1M, R_B = 143k.$

 $V_{IN(MAX)} = 15.5V$, $R_A = 1M$, $R_B = 86.6k$.

Step 3: Set the Maximum Duty Cycle (R_{DC(MAX)})

The maximum duty cycle (DC_{MAX}) is determined by the switching period $(T_S = 1/f_{SW})$ and non-overlap time $(T_{D(MIN)})$ between the two power switches, as shown in equation 5. For the 2-resistor method, R_{DC} is calculated by equation 6. For the 3-resistor method, substitute $R_A = R_{A1} + R_{A2}$ in equation 6.

$$DC_{MAX} = \frac{T_{S} - 2T_{D(MIN)}}{2T_{S}}$$
(5)

 R_DC

$$=\frac{V_{\text{IN}(\text{MIN})} \bullet \frac{R_{\text{B}}}{R_{\text{A}} + R_{\text{B}}} \bullet R_{\text{T}} \bullet \text{DC}_{\text{MAX}} \bullet 4}{1.25}$$
(6)

In the Figure 1(a) example, $T_S = 1 \mu s$, $T_{D(MIN)} = 70ns$ (typical value in the data sheet), $V_{IN(MIN)} = 10V$, $R_A = 1M$, $R_B = 143k$. Calculations 5 and 6 give $DC_{MAX} = 0.43$, and $R_{DC} = 13.3k$.

Step 4: Select the Transformer (T1)

The transformer turns ratio is represented in equation 7.

$$N = \frac{N_{s}}{N_{p}}$$

$$= \frac{|V_{0UT1}| + |V_{0UT2}| + V_{LD01} + V_{LD02} + 2V_{F}}{2(V_{IN(MIN)} - V_{SW}) \cdot 2DC_{max}}$$
(7)

 V_{SW} is the switch saturation voltage for internal switches. V_F is the forward voltage of the rectifier diodes. V_{LDO1} and V_{LDO2} are the dropout voltages of the positive and negative LDOs. $V_{SW} = 0.4V$, $V_F = 0.7V$, $V_{LDO1} = V_{LDO2} = 0.8V$ are good rules of thumb. If a commercial transformer with an exact calculated turns ratio cannot be found, select one that is close and calculate DC_{MAX} in equation 7 accordingly. Then, recalculate R_{DC} in equation 6 based on new DC_{MAX} .

In the Figure 1(a) example, $V_{OUT1} = -V_{OUT2} = 12V$ and $V_{IN(MIN)} = 10V$, so choose Wurth 750314781(N = 2) for DC_{MAX} = 0.43.

Step 5: Design the Rectifier (D1, D2, D3 and D4)

The peak voltage across the rectifier bridge is composed of the transformer secondary side voltage (V_{SEC}) plus any ringing voltage spikes. V_{SEC} is calculated using equation 8. The ringing voltage spike, however, is difficult to predict, as it depends on the loop resistance, the leakage inductance of the transformer, and the junction capacitance of the rectifiers. As general rule, the rectifier voltage rating (V_{REC}) should be at

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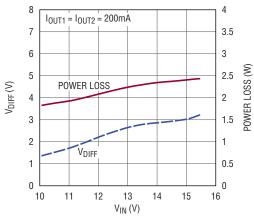


Figure 3. LDO (U2) V_{IN} – V_{OUT} differential and power loss vs input voltage

least 1.5 times the transformer turns ratio multiplied by the maximum input voltage. Because the two secondary windings are connected across the rectifier bridge, a factor of two is required, producing the formula for the rectifier voltage rating:

(8)

$$V_{\text{REC}} \ge 1.5 \bullet 2\text{N} \bullet V_{\text{IN(MAX)}}$$

The current rating of the rectifier $\left(I_{REC}\right)$ should be greater than the load current.

When $V_{IN(MAX)} = 15.5V$, N = 2, $V_{REC} \ge 93V$, $I_{REC} \ge 200$ mA: a Central CMSH1-200HE (200V, 1A) satisfies these requirements.

Step 6: Select the Inductors (L1, L2)

The minimum inductor value (L_{MIN}) is set by the peak current limit of internal switcher (I_{LIM}) as shown by equation 9.

L_{MIN}

$$=\frac{2N \bullet V_{IN(MAX)} \bullet (1-2DC_{MIN}) \bullet DC_{MIN} \frac{T_{S}}{2}}{2\left(\frac{I_{LIM}}{2N} - I_{OUT1}\right)}$$
(9)

Higher inductance produces better regulation and lower voltage ripple, but requires a correspondingly greater volume part. The optimum inductor value is determined by taking into account both output noise and solution volume requirements.

When $V_{IN(MAX)} = 15.5V$, $DC_{MIN} = 0.28$, $T_S = 1\mu s$, N = 2, $I_{LIM} = 1A$, $I_{OUT1} = I_{OUT2} = 200$ mA, $L_{MIN} = 38.3\mu$ H: A Coilcraft XFL3012-393MEC (39.3 μ H)

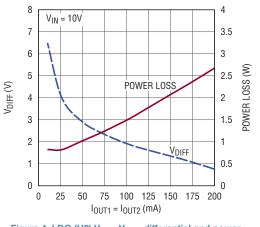


Figure 4. LDO (U2) $V_{IN} - V_{OUT}$ differential and power loss vs load

satisfies these requirements without adding unnecessary size.

Step 7: Select the Low Dropout Linear Regulator (U2, U3)

The maximum voltage of LDO occurs at maximum input voltage under no load, when V_{SEC} equals $V_{IN(MAX)} \bullet N$. The current rating of the LDO should be greater than the load current.

When $V_{IN(MAX)} = 15.5V$, N = 2, the voltage rating for the LDOs should be 31V and -31V, satisfied by the LT3065 (45V, 500mA) and LT3090 (-36V, 400mA), respectively.

Step 8: Add a Snubber (Cs and Rs)

The recommended approach for designing an RC snubber (C_s and R_s in Figure 1) is to measure the period of the ringing at the LT3999's SWA and SWB pins when its switchers turn off without the snubber, and then add capacitance—starting with something in the range of 100pF—until the ringing period lengthens by 1.5x to 2x.

The change in period determines the value of the parasitic capacitance (C_{PAR}) , from which the parasitic inductance (L_{PAR}) can be determined from the initial period. Similarly, initial values can be estimated using data sheet values for switch capacitance and transformer leakage inductance.

Once the value of the drain node capacitance and inductance are known, a series resistor can be added to the snubber capacitance to dissipate power and critically dampen the ringing. The equation for deriving the optimal series resistance using the observed periods $(t_{PERIOD}, and t_{PERIOD(SNUBBED)})$ and snubber capacitance (C_S) is below. Refer to the LT3748 data sheet for more details.

$$C_{PAR} = \frac{C_{S}}{\left(\frac{t_{PERIOD}(SNUBBED)}{t_{PERIOD}}\right)^{2} - 1}$$
(10)
$$L_{PAR} = \frac{\left(t_{PERIOD}\right)^{2}}{C_{PAR} \cdot 4\pi^{2}}$$
(11)

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}}$$
(12)

RESULTS

The measured results in Figures 3, 4 and 5 show that duty cycle control in the push-pull converter of Figure 1 maintains a low $V_{IN} - V_{OUT}$ differential across the LDOs, resulting in minimized power loss and temperature rise. Figure 3 shows that at 200mA per LDO, V_{DIFF} , remains under 2.5V over the entire input voltage range of 10V–15V. Figure 4 shows power loss remains low across the load current range. Figure 5 and Figure 6 show the thermal results.

For comparison, Figure 7 shows the efficiency comparison of the design with duty cycle control disabled and duty

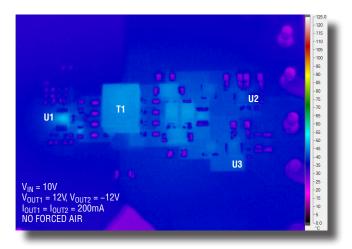


Figure 5. Thermal image of the design in Figure 1 in action, $V_{IN} = 10V$

cycle control enabled. The efficiency drops dramatically when input voltage increases. Figure 8 shows the differential voltage across the positive LDO with duty cycle control disabled and duty cycle control enabled. Figures 9 and 10 show the thermal results. It is evident that the duty cycle control reduces the differential voltage and improves the efficiency and thermal performance

COMPACT TRANSFORMER DRIVER FOR A FIXED INPUT VOLTAGE

Normally, the output voltage of the basic unregulated transformer driver converter changes significantly with changes in load current. To produce a regulated voltage, an LDO on the output is strongly recommended. Figure 6a shows the schematic of low part count transformer driver using the LT3999. Figure 6b shows the design flowchart.

The four simple steps in the flowchart can be used to design a 1MHz, low parts count, 5V input, 5V output 400mA output transformer driver as an example. Step 1: Set the Switching Frequency (R_{T})

The switching frequency of the LT3999 is set by a single R_T resistor selected based on the table in the LT3999 data sheet (frequency range is from 50kHz to 1MHz).

In the design example, for high frequency f_{SW} = 1MHz, R_T = 12.1k.

Step 2: Select the Transformer (T1)

The transformer turns ratio is determined by:

$$N = \frac{N_S}{N_P} = \frac{V_{OUT} + V_{LDO(OPTIONAL)} + V_F}{V_{IN} - V_{SW}}$$
(13)

where v_{sw} is the switch saturation voltage for internal switchers, and v_F is the forward voltage of a rectifier diode.

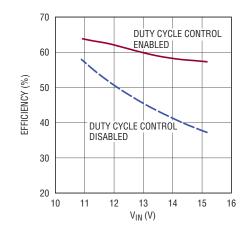


Figure 7. Efficiency comparison of the design with duty cycle control disabled and duty cycle control enabled, $I_{OUT1} = I_{OUT2} = 200$ mA

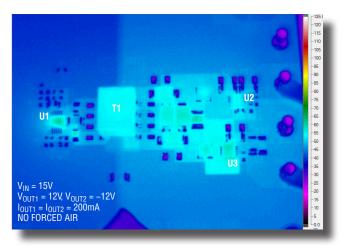


Figure 6. Thermal image, V_{IN} = 15V

 V_{LDO} is the drop from the unregulated transformer driver output to the post regulated low noise output. V_{LDO} is the drop at highest current, so it should be minimized. 0.8V provides enough drop to avoid dropout without the LDO getting hot. A good rule of thumb assumption is $V_{SW} = 0.4V$, $V_F = 0.7V$, $V_{LDO} = 0.8V$.

The current rating of the transformer should be $20\% \sim 50\%$ larger than the output current to leave some room.

The sum of the peak magnetizing current $(I_{M(PEAK)})$ and the full load current reflected to the primary side $(N \bullet I_{OUT})$ should less than the peak current limit of the internal switcher (I_{LIM}) . Based on this, minimal L_M $(L_{M(MIN)})$ is required.

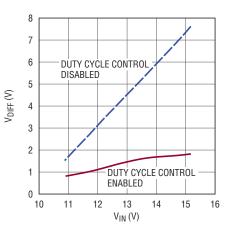


Figure 8. LDO (U2) $V_{IN} - V_{OUT}$ differential vs V_{IN} at full load with duty cycle control disabled and with duty cycle control enabled, $I_{OUT1} = I_{OUT2} = 200$ mA

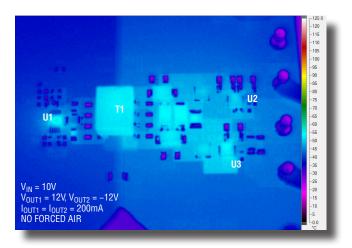


Figure 9. Thermal image of the design with duty cycle control disabled in circuit of Figure 1, $V_{\rm IN}$ = 10V

$$I_{M(PEAK)} + N \bullet I_{OUT}$$

$$= \left(\frac{V_{IN} - V_{SW}}{L_{M}} \bullet \frac{T_{S}}{4}\right) + N \bullet I_{OUT}$$
(14)
< I_{LIM}

$$L_{M} > \frac{V_{IN} - V_{SW}}{I_{LIM} - N \bullet I_{OUT}} \bullet \frac{T_{S}}{4} = L_{M(MIN)}$$
(15)

For $V_{OUT} = V_{IN} = 5V$, the Coilcraft PA6383-AL (N = 1.5) is a good fit.

Step 3: Rectifier (D1, D2)

Choose the rectifier diodes based on voltage and current. The voltage across the diodes is more than twice that of the transformer secondary voltage because of its center tap structure. The voltage rating of the rectifier should be larger than $2N \cdot V_{IN} = 15V$, maybe by 20%.

The CMSH1-20M (20V, 1A) satisfies these requirements.

Step 4: Low Dropout Linear Regulator (U2, Optional)

The maximum input voltage of the optional post-regulating LDO $(V_{LDO_IN(MAX)})$ occurs at no load, where it equals $V_{IN} \bullet N = 7.5V$. The current rating of the LDO should be larger than the load current (>400mA in the case of the design example).

A good LDO for the 5V, 400mA output is the LT1763 (20V, 500mA).

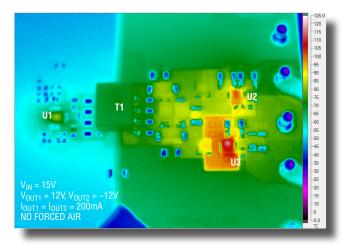


Figure 10. Thermal image of the design with duty cycle control disabled in circuit of Figure 1, $V_{\rm IN}$ = 15V

CONCLUSION

The LT3999 is a monolithic DC/DC transformer driver, which features duty cycle control, high frequency and high power. It allows a wide input voltage range and low loss at the LDO, while using small passive components due to its high frequency operation. It also features input voltage up to 36V and input current up to 1A.

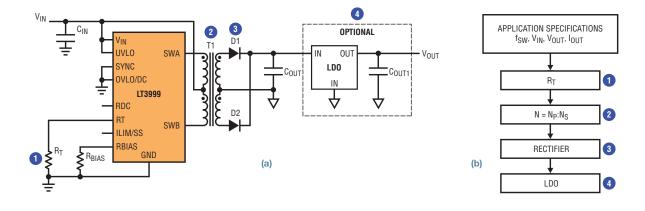


Figure 11. (a) Low parts count, fixed input voltage transformer driver. (b) Design flowchart for the transformer driver