Application Note AN-4147

Design Guidelines for RCD Snubber of Flyback Converters

Abstract

This article presents some design guidelines for the RCD snubber of flyback converters. When the MOSFET turns off, a high-voltage spike occurs on the drain pin because of a resonance between the leakage inductor (L_{lk}) of the main transformer and the output capacitor (C_{OSS}) of the MOSFET. The excessive voltage on the drain pin may lead to an avalanche breakdown and eventually damage the MOSFET. Therefore, it is necessary to add an additional circuit to clamp the voltage.

Introduction

One of the most simple topologies is a flyback converter. It is derived from a buck-boost converter by replacing filter inductors with coupled inductors, such as gapped core transformers. When the main switch turns on, the energy is stored in the transformer as a flux form and is transferred to output during the main switch off-time. Since the transformer needs to store energy during the main switch on-time, the core should be gapped. Since flyback converters need very few components, it is a very popular topology for low- and medium-power applications such as battery chargers, adapters, and DVD players.

Figure 1 shows a flyback converter operating in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) with several parasitic components, such as primary and secondary leakage inductors, an output capacitor of MOSFET, and a junction capacitor of a secondary diode.

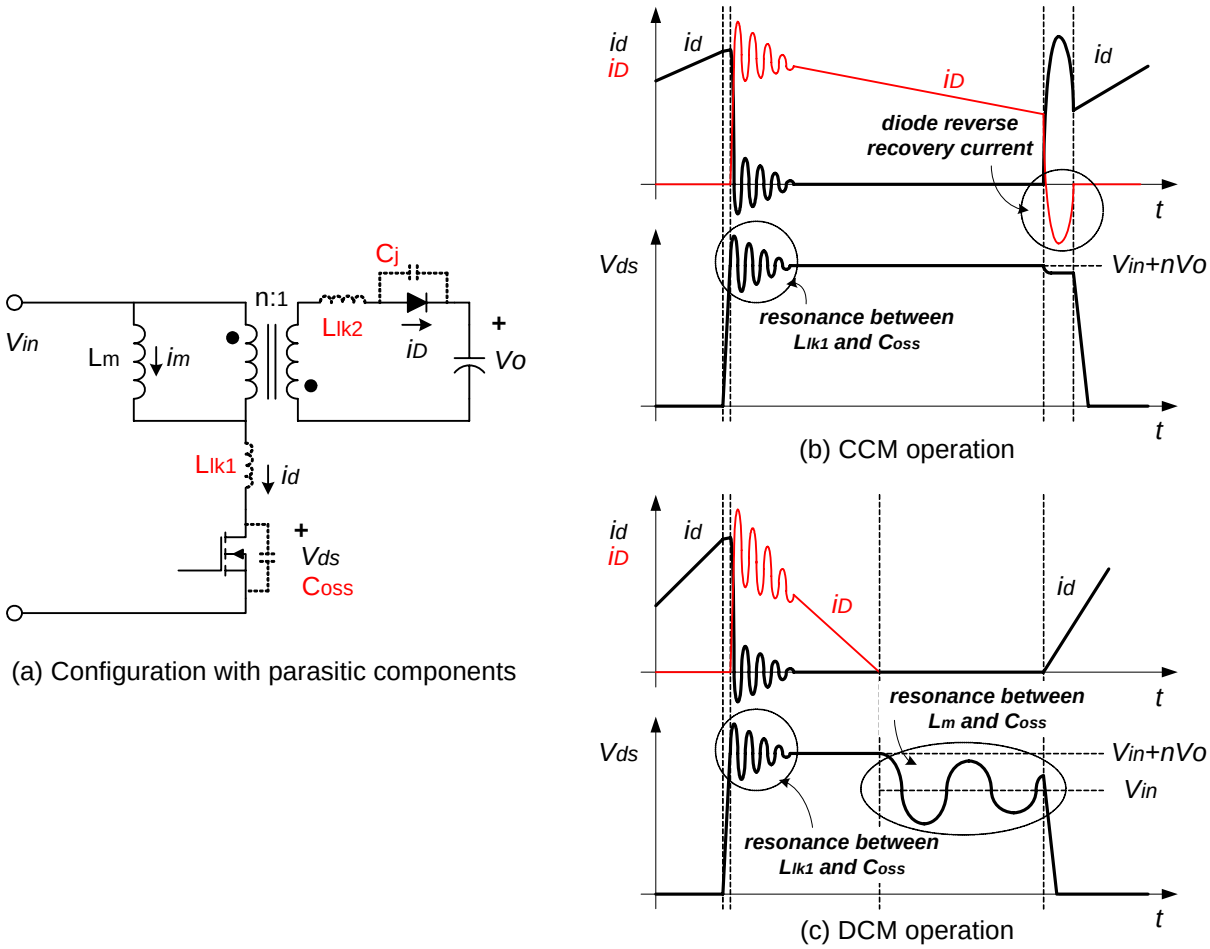

Figure 1. Flyback Converter; (a) Configuration with Parasitic Components, (b) CCM Operation, (c) DCM Operation

When the MOSFET turns off, the primary current (i_d) charges C_{OSS} of the MOSFET in a short time. When the voltage across C_{OSS} (V_{ds}) exceeds the input voltage plus reflected output voltage ($V_{in}+nV_o$), the secondary diode turns on, so that the voltage across the magnetizing inductor (L_m) is clamped to nV_o. There is, therefore, a resonance between L_{lk1} and C_{OSS} with high-frequency and high-voltage surge. This excessive voltage on the MOSFET may cause failure. In the case of the CCM operation, the secondary diode remains turned on until the MOSFET is gated on. When the MOSFET turns on, a reverse recovery current of the secondary diode is added to the primary current, and there is a large current surge on the primary current at the turn-on instance. Meanwhile, since the secondary current runs dry before the end of one switching period in the case of the DCM operation, there is a resonance between L_m and C_{OSS} of the MOSFET.

Snubber design

The excessive voltage due to resonance between L_{lk1} and C_{OSS} should be suppressed to an acceptable level by an additional circuit to protect the main switch. The RCD snubber circuit and key waveforms are shown in Figures 2 and 3. The RCD snubber circuit absorbs the current in the leakage inductor by turning on the snubber diode (D_{sn}) when V_{ds} exceeds $V_{in}+nV_o$. It is assumed that the snubber capacitance is large enough that its voltage does not change during one switching period.

When the MOSFET turns off and V_{ds} is charged to $V_{in}+nV_o$, the primary current flows to C_{sn} through the snubber diode (D_{sn}). The secondary diode turns on at the same time. Therefore, the voltage across L_{lk1} is $V_{sn}-nV_o$. The slope of i_{sn} is as follows:

$$\frac{di_{sn}}{dt} = -\left(\frac{V_{sn} - nV_o}{L_{lk1}}\right) \quad (1)$$

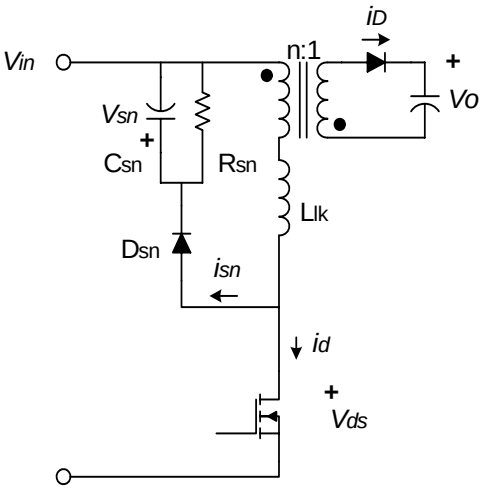

Figure 2. Flyback Converter with RCD Snubber

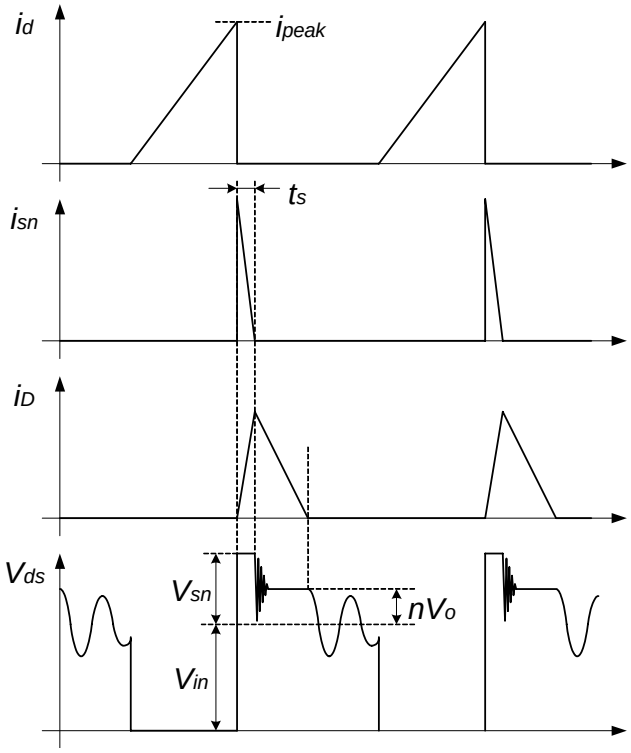

Figure 3. Key Waveforms of the Flyback Converter with RCD Snubber in DCM Operation

where i_{sn} is the current that flows into the snubber circuit, V_{sn} is the voltage across the snubber capacitor C_{sn}, n is the turns ratio of the main transformer, and L_{lk1} is the leakage inductance of the main transformer. The time t_s is obtained by:

$$t_s = \frac{L_{lk1}}{V_{sn} - nV_o} \times i_{peak} \quad (2)$$

where i_{peak} is the peak current of the primary current.

The snubber capacitor voltage (V_{sn}) should be determined at the minimum input voltage and full-load condition. Once V_{sn} is determined, the power dissipated in the snubber circuit at the minimum input voltage and full-load condition is obtained by:

$$P_{sn} = V_{sn}\frac{i_{peak} \cdot t_s}{2} f_s = \frac{1}{2} L_{lk} {i_{peak}}^2 \frac{V_{sn}}{V_{sn} - nV_o} f_s \quad (3)$$

where f_s is the switching frequency of the flyback converter. V_{sn} should be 2~2.5 times of nV_o. Very small V_{sn} results in a severe loss in the snubber circuit, as shown in the above equation.

On the other hand, since the power consumed in the snubber resistor (R_{sn}) is V_{sn}^2/R_{sn}, the resistance is obtained by:

$$R_{sn} = \frac{V_{sn}^2}{\frac{1}{2} L_{lk1} i_{peak}^2 \frac{V_{sn}}{V_{sn} - nV_o} f_s} \quad (4)$$

The snubber resistor with the proper rated power should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as follows:

$$\Delta V_{sn} = \frac{V_{sn}}{C_{sn} R_{sn} f_s} \quad (5)$$

In general, 5~10% ripple is reasonable. Therefore, the snubber capacitance is calculated using the above equation.

When the converter is designed to operate in CCM, the peak drain current, together with the snubber capacitor voltage, decreases as the input voltage increases. The snubber capacitor voltage under maximum input voltage and full-load condition is obtained as follows:

$$V_{sn2} = \frac{nV_o + \sqrt{(nV_o)^2 + 2R_{sn} L_{lk1} f_s (I_{peak2})^2}}{2} \quad (6)$$

where f_s is the switching frequency of the flyback converter, L_{lk1} is the primary-side leakage inductance, n is the turns ratio of the transformer, R_{sn} is the snubber resistance, and I_{peak2} is the primary peak current at the maximum input voltage and full-load condition. When the converter operates in CCM at the maximum input voltage and full-load condition, the I_{peak2} is obtained as follows:

$$I_{peak2} = \frac{P_{in}(V_{DC}^{max} + nV_o)}{V_{DC}^{max} \times nV_o} + \frac{V_{DC}^{max} \times nV_o}{2L_m f_s (V_{DC}^{max} + nV_o)} \quad (7)$$

When the converter operates in DCM at the maximum input voltage and full-load condition, the I_{peak2} is obtained by:

$$I_{peak2} = \sqrt{\frac{2P_{in}}{f_s L_m}} \quad (8)$$

where P_{in} is the input power, L_m is the magnetizing inductance of the transformer, and V_{DC}^{max} is the rectified maximum input voltage in DC value.

Verify that the maximum value of V_{ds} is below 90% and 80% of the rated voltage of the MOSFET (BV_{dss}), at the transient period and steady-state period, respectively. The voltage rating of the snubber diode should be higher than BV_{dss}. Usually an ultra-fast diode with 1A current rating is used for the snubber circuit.

Example

An adapter using FSDM311 has following specifications: $85V_{ac}$ to $265V_{ac}$ input voltage range, 10W output power, 5V output voltage, and 67kHz switching frequency. When the RCD snubber uses a 1nF snubber capacitor and 480kΩ snubber resistor, Figure 4 shows several waveforms with $265V_{ac}$ at the instance of the AC switch turn-on.

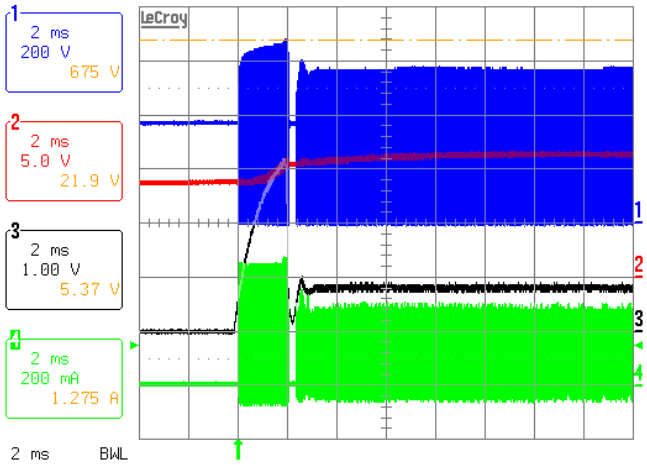

Figure 4. Start-up Waveforms with 1nF Snubber Capacitor and 480kΩ Snubber Resistor

In Figures 4-7, Channel 1 through 4 stand for the drain voltage (V_{ds}, 200V/div), the supply voltage (V_{CC}, 5V/div), the feedback voltage (V_{fb}, 1V/div), and the drain current (I_d, 0.2A/div), respectively. The maximum voltage stress on the internal SenseFET is around 675V, as shown in Figure 4. The voltage rating of FSDM311 is 650V, according to the datasheet. There are two reasons for the excess of the voltage ratings: the wrong transformer design and/or the wrong snubber design. Figure 5 shows the reason.

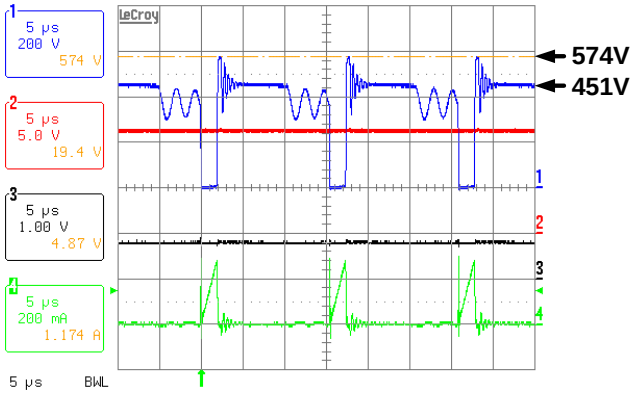

Figure 5. Steady-State Waveforms with 1nF Snubber Capacitor and 480kΩ Snubber Resistor

For the reliability, the maximum voltage stress at the steady state should be equal to 80% of the rated voltage (*650V * 0.8 = 520V*). Figure 5 shows the voltage stress on the internal SenseFET is above 570V with V_{in} = 265V_{ac} at steady state. However, the fact that V_{in}+nV_o is around 450V (= *375V + 15 * 5V*) implies the turns ratio of the transformer is 15, which is a reasonable value. Therefore, the snubber circuit should be redesigned.

Let V_{sn} be twice that of nV_o, 150V, and L_{lk1} and i_{peak} is 150 µH and 400mA by measuring, respectively. Obtain the snubber resistance as follows:

$$R_{sn} = \frac{V_{sn}^{\ 2}}{\frac{1}{2} L_{lk1} i_{peak}^{\ 2} \frac{V_{sn}}{V_{sn} - nV_o} f_s} = \frac{150^2}{\frac{1}{2} \times 150\mu \times 0.4^2 \times \frac{150}{150-75} \times 67k} = 14k \quad (9)$$

The power emission from R_{sn} is calculated as follows:

$$P = \frac{V_{sn}^{\ 2}}{R_{sn}} = \frac{150^2}{14k} = 1.6W \quad (10)$$

Let the maximum ripple of the snubber capacitor voltage be 10% and the snubber capacitance is obtained as follows:

$$C_{sn} = \frac{V_{sn}}{\Delta V_{sn} R_{sn} f_s} = \frac{150}{15 \times 14k \times 67k} = 10nF \quad (11)$$

The results with 14kΩ (3W) and 10nF are shown in Figures 6 and 7.

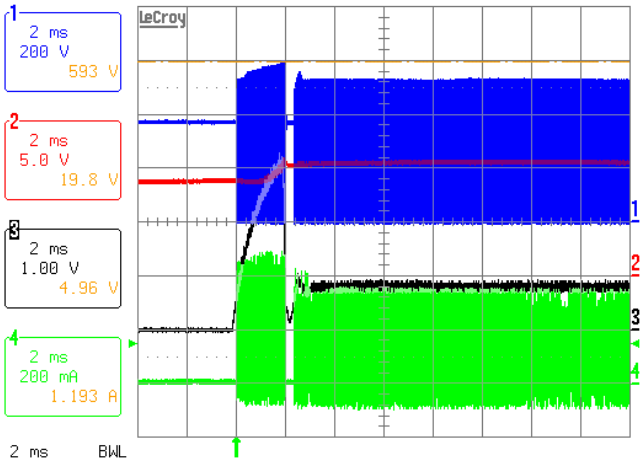

Figure 6. Start-up Waveforms with 10nF Snubber Capacitor and 14kΩ Snubber Resistor

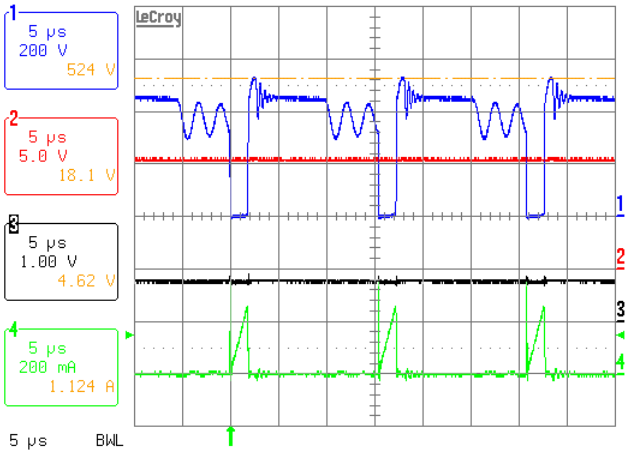

Figure 7. Steady-State Waveforms with 10nF Snubber Capacitor and 14kΩ Snubber Resistor

The voltage stresses on the internal SenseFET are 593V and 524V at the startup and steady state, respectively. These are around 91.2% and 80.6% of the rated voltage of FSDM311, respectively.

by Gwan-Bon Koo/ Ph. D

FPS Application Group / Fairchild Semiconductor
Phone +82-32-680-1327
Fax +82-32-680-1317
E-mail koogb@fairchildsemi.co.kr