A New Gate Charge Factor Leads to Easy Drive Design for Power MOSFET Circuits

By B. R. PELLY

Designers unfamiliar with MOSFET characteristics begin drive circuit design by determining component values based on the gate-to-source, or input, capacitance listed on the data sheet. While RC values derived in this manner do serve as a starting point in design, they can only be considered as a first-order benchmark.

If the designer wants to switch the MOSFET in 100 nanoseconds, an RC value based on the gate-to-source capacitance is determined to provide a suitable, theoretical time constant. The RC value does not solve the entire problem because the gate-to-drain capacitance must also be accounted for in charge time.

Although the gate-to-source capacitance is an important value, the gate-to-drain capacitance is actually more significant — and more difficult to deal with — because it is a non-linear capacitance affected as a function of voltage; the gate-to-source capacitance is also affected as a voltage function, but to a much lesser extent. This gate-to-drain capacitance function is similar to that found in vacuum tube amplifiers.

The gate-to-drain capacitance effect is akin to the "Miller" effect, a phenomenon by which a feedback path between the input and output of an electronic device is provided by the interelectrode capacitance. This affects the total input admittance of the device which results in the total dynamic input capacitance generally being greater than the sum of the static electrode capacitances. The phenomenon of the effects of the plate impedance and voltage gain on the input admittance was first studied in vacuum tube triode amplifier circuits by John M. Miller.

Essentially, at high frequencies where the grid-to-plate (gate-to-drain) capacitance is not negligible, the circuit is not open but involves a capacitance that is a function of the voltage gain.

Solving for the "Miller" effect is not exactly a straightforward process, even with vacuum tubes where much is known, but is even more difficult in MOSFETs. In actuality, the gate-to-drain capacitance though smaller in static value than the gate-to-source capacitance, goes through a voltage excursion that is often more than 20 times that of the gate-to-source capacity. Therefore, the gate-to-drain or "Miller" capacitance typically requires more actual charge than the input capacitance.

To account for both gate-to-source and gate-to-drain capacitance in a way readily usable by designers, each HEXFET from International Rectifier is tested to yield a specification termed "gate charge," that can be used to calculate drive circuit requirements.

A typical test circuit that can be used to measure the gate charge is

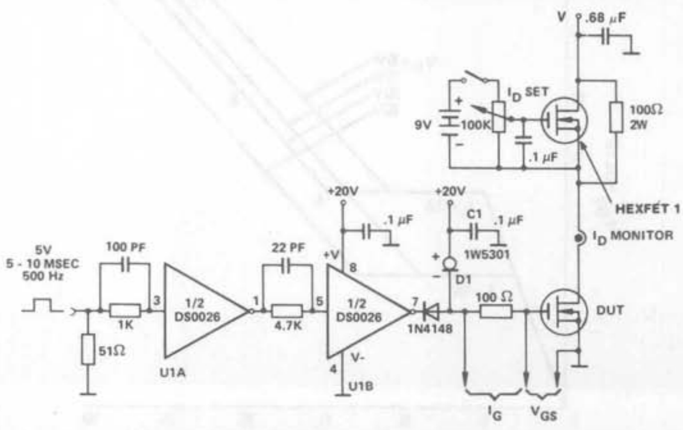

Figure 1. HEXFET Gate Charge Circuit.

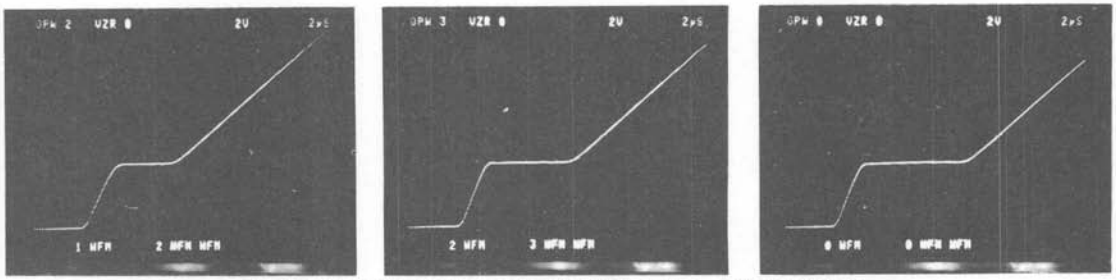

Figure 2. Gate Charge Waveform for Different Values of Drain Voltage
(IRF130: I_G = 1.5 mA, I_D = 1A, V_{DD} = 10, 40 and 80 Volts).

shown in Figure 1. In this circuit, an approximately constant current is supplied to the gate of the device-under-test from the 0.1 μF capacitor C1, through the regulator diode D1. A constant current in the drain circuit is set by setting the voltage on the gate of HEXFET 1, so the net measurement of the charge consumed by the gate is relative to a given current and voltage in the source-to-drain path.

An oscillogram of the gate-to-source voltage during testing, shown in Figure 2, relates the gate voltage to time. Since a constant current is supplied to the gate, the horizontal time scale is directly proportional to the charge supplied to the gate. With a suitable scaling factor, therefore, this oscillogram is a plot of gate voltage versus charge.

The point on the oscillogram of the second voltage rise indicates where the device is fully switched on. During the first voltage rise, the gate-to-source capacitance is charging, and during the flat portion, the gate-to-drain capacitance is charging. This oscillogram therefore clearly differentiates between the charge required for the gate-source and gate-to-drain ("Miller") capacitances. At the second voltage rise, both capacitances are charged to the extent needed to switch the given voltage and current. A more detailed explanation of the interpretation of this data is given later.

The graph in Figure 3 represents gate voltage versus gate charge in nanocoulombs for an IRF130. Although the second voltage rise indicates the point at which the switching operation is completed, normal design safety margins will dictate that the level of drive voltage applied to the gate is greater than that which is just required to switch the given drain current and voltage. The total charge consumed by the gate will therefore in practice be higher than the minimum required — but not necessarily significantly so. For example, the gate charge required to switch 12 A at 80 V is 15 nanocoulombs (point A), and the corresponding gate voltage is about 7 V. If the applied drive voltage has an amplitude of 10 V (i.e. a 3 V margin), then the total gate charge actually consumed would be about 20 nanocoulombs, (point B).

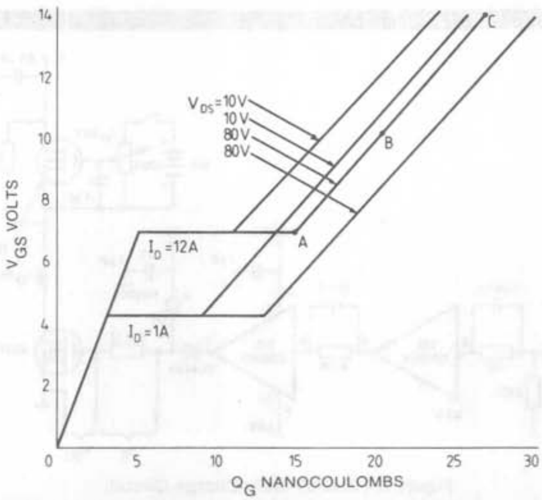

Figure 3. Gate Voltage Versus Gate Charge for the IRF130.

As shown on the graph, whether switching 10 or 80 volts in the drain circuit, there is a much less than proportional difference in the charge required. This is because the "Miller" capacitance is a nonlinear function of voltage, and decreases with increasing voltage.

The importance of the gate charge data to the designer is illustrated as follows. Taking the previous example, about 15 nanocoulombs of gate charge are required to switch a drain voltage of 80 V and a drain current of 12 A. Since the 15 nC gate charge is the product of the gate input current and the switching time, if 1.5 A is supplied to the gate, the device will be switched in 10 ns. It follows that if 15 mA is supplied to the gate, then switching occurs in 1 μs, and so on.

These simple calculations immediately tell the designer the trade-offs between the amount of current available from the drive circuit and the achievable switching time. With gate charge known, the designer can develop a drive circuit appropriate to the switching time required.

Consider a typical practical example of a 100 kHz switcher, in which it is required to achieve a switching time of 100 nanoseconds. The required gate drive current is derived by simply dividing the gate charge, 15×10^{-9}, by the required switching time, 100×10^{-9}, giving 150 mA. From this calculation, the designer can further arrive at the drive circuit impedance. If the drive circuit applies 14 V to the gate, for instance, then a drive impedance of about 50 ohms would be required. Note that throughout the "flat" part of the switching period (Figure 3), the gate voltage is constant at about 7 V. The difference between the applied 14 V and 7 V is what is available to drive the required current through the drive circuit resistance.

The gate charge data also lets the designer quickly determine average gate drive power. The average gate drive power, P_{DRIVE}, is $Q_G V_G f$. Taking the above 100 kHz switcher as an example, and assuming a gate drive voltage V_G of 14 V, the appropriate value of gate charge Q_G is 27 nanocoulombs (point C on Figure 3). The average drive power is therefore $27 \times 10^{-9} \times 14 \times 10^5 = 0.038$ Watts. Even though the 150 mA drive current which flows during the switching interval may appear to be relatively high, the average power is miniscule (0.004%) in relation to the power being switched in the drain current. This is because the drive current flows for such a short period that the average power is negligible.

Thus actual drive power for MOSFETs is minute compared to bipolar requirements, which must sustain switching current during the entire ON condition. Average drive power, of course, increases at higher frequencies, but even at 5 MHz it would be only 1.9 W.

The Gate Charge Curve

The oscillograms of the gate-to-source voltage in Figure 2 neatly delineate between the charge required for the gate-to-source capacitance, and the charge required for the gate-to-drain, or "Miller" capacitance. The accompanying simplified test circuit and waveform diagram (Figures 4 and 5 respectively) give the explanation.

Before time t_0, the switch S is closed; the device under test (DUT) supports the full circuit voltage, V_{DD}, and the gate voltage and drain current are zero. S is opened at time t_0; the gate-to-source capacitance starts to charge, and the gate-to-source voltage increases. No current flows in the drain until the gate reaches the threshold voltage.

During period t_1 to t_2, the gate-to-source capacitance continues to charge, the gate voltage continues to rise and the drain current rises proportionally. So long as the actual drain current is still building up towards the available drain current, I_D, the freewheeling rectifier stays in conduction, the voltage across it remains low, and the voltage across the DUT continues to be virtually the full circuit voltage, V_{DD}. The top end of the drain-to-gate capacitance C_{GD} therefore remains at a fixed potential, whilst the potential of the lower end moves with that of the gate. The charging current taken by C_{GD} during this period is small, and for practical purposes it can be neglected, since C_{GD} is numerically small by comparison with C_{GS}.

At time t_2, the drain current reaches I_D, and the freewheeling rectifier shuts off; the potential of the drain now is no longer tied to the supply voltage, V_{DD}. The drain current now stays constant at the value I_D enforced by the circuit, whilst the drain voltage starts to fall. Since the gate voltage is inextricably related to the drain current by the intrinsic transfer characteristic of the DUT (so long as operation remains in the "active" region), the gate voltage now stays constant because the "enforced" drain current is constant. For the time being, therefore, no further charge is consumed by the

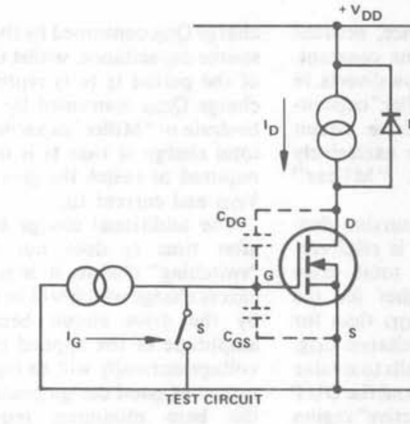

Figure 4. Basic Gate Charge Test Circuit

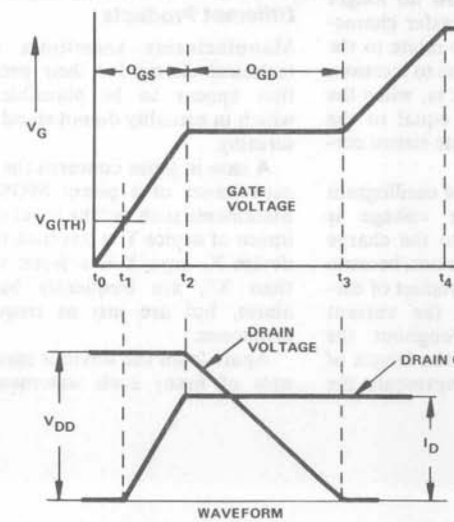

Figure 5. Basic Gate Charge Waveforms

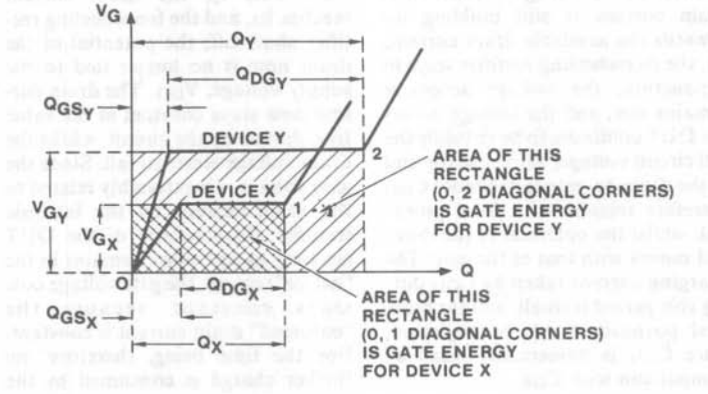

Figure 6. Comparison of Gate Charge Characteristics of Different Device Types.

gate-to-source capacitance, because the gate voltage remains constant. Thus the drive current now diverts, in its entirety, into the "Miller" capacitance C_{GD}, and the drive circuit charge now contributes exclusively to discharging the "Miller" capacitance.

The drain voltage excursion during the period t_2 to t_3 is relatively large, and hence the total drive charge is typically higher for the "Miller" capacitance C_{GD} than for the gate-to-source capacitance C_{GS}. At t_3 the drain voltage falls to a value equal to $I_D \times R_{DS(ON)}$, and the DUT now comes out of the "active" region of operation. (In bipolar transistor terms, it has reached "saturation.") The gate voltage is now no longer constrained by the transfer characteristic of the device to relate to the drain current, and is free to increase. This it does, until time t_4, when the gate voltage becomes equal to the voltage "behind" the gate circuit current source.

The time scale on the oscillogram of the gate-to-source voltage is directly proportional to the charge delivered by the drive circuit, because charge is equal to the product of current and time, and the current remains constant throughout the whole sequence. Thus the length of the period t_0 to t_1 represents the charge Q_{GS} consumed by the gate-to-source capacitance, whilst the length of the period t_2 to t_3 represents the charge Q_{GD} consumed by the gate-to-drain or "Miller" çapacitance. The total charge at time t_3 is the charge required to switch the given voltage V_{DD} and current I_D.

The additional charge consumed after time t_3 does not represent "switching" charge; it is simply the excess charge which will be delivered by the drive circuit because the amplitude of the applied gate drive voltage normally will be higher (as a matter of good design practice) than the bare minimum required to accomplish switching.

Beware When Comparing Different Products

Manufacturers sometimes make technical claims for their products that appear to be plausible, but which in actuality do not stand up to scrutiny.

A case in point concerns the input capacitance of a power MOSFET. Statements such as "the input capacitance of device Y is less than that of device X, ergo Y is a faster switch than X", are frequently bandied about, but are just as frequently erroneous.

Apart from the obvious speciousness of many such statements — "apples" are frequently not compared with "apples", and obviously larger chips have more self capacitance than smaller ones — the more basic fundamentals are generally overlooked.

As this application note shows, of "bottom line" importance is the total gate charge required for switching. The lower the charge, the lower is the gate drive current needed to achieve a given switching time.

A general comparison between hypothetical MOSFETs brands "X" and "Y" is illustrated in the Figure. Device X has a higher input capacitance; hence the initial slope of its gate charge characteristic is less than that of device Y. Q_{GS} of device X is, however, about the same as that of device Y, because it has a higher transconductance and therefore requires less voltage on its gate for the given amount of drain current (V_{GX} is less than V_{GY}). The "Miller" charge consumed by device X is considerably less than that consumed by device Y. The overall result is that the total charge required to switch device X, Q_X, is considerably *less* than that required to switch device Y, Q_Y.

Had the comparison between devices X and Y been made on the more superficial basis of input capacitances, it would have been concluded — erroneously — that Y is "better" than X.

Another consideration is the energy required for switching. Again, device X scores handsomely over device Y in this example. The energy is the product of the gate charge and the gate voltage, and is represented by the area of the rectangle whose corner lies at the "switching point". (Point 1 for device X, and point 2 for device Y.) It is obvious that X requires significantly less gate energy than Y.

To summarize: beware of superficial comparisons. Check the full facts before deciding which MOSFET really has the edge in switching performance.□