A NEW ISOLATED GATE DRIVE for Power MOSFETs and IGBTs

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INTRODUCTION

Isolated power switches are very often used for applications in motor drives, uninterruptible power supplies, and AC switches. It allows the safety norms to be met and provides the operating isolation required when the switch is floating with respect to ground. Today, the isolated base drive design of bipolar power transistors is well understood (see bibliography), whilst those for Power MOSFET designs are less well known and are still improving. This paper highlights and uses the specific behaviour of a Power MOSFET, and area often neglected: the gate drive described capitalises on the opportunity to use the gate input capacitor as an no-state memory. Driving a transistor requires supplying signals and energy. If switch isolation is needed, optical links and /or transformers are used according to the specified norms and operating dV/dt. This paper proposes an innovative isolated gate drive using the memory effect of the Power MOSFET input capacitor and an associated pulse transformer that provides both signal and energy to this capacitor.

GENERAL CHARACTERISTICS OF A POWER MOSFET ISOLATED DRIVER

Safety norms impose a minimum creepage distance and clearance as well as insulation resistance between control circuit and power switches. These isolation requirements have to be respected by any opto-coupler, pulse transformer or auxiliary power supplies. Electrically, its power switches often float above ground and any isolation must withstand a dV/dt above 20V/nsec. Because a high dV/dt induces a large Miller effect, a low gate drive impedance has to be used during the off-state to avoid any spurious unwanted turn-on of the power switch. As these switches are generally used in PWM circuits, the minimum ON or OFF time must be as low as possible, so enabling a large duty cycle range to be available. Short circuit detection that, via the control circuit, ensures safe operation.

THE NEW CONCEPT

The basic principle consists in using the Power MOSFET input Capacitor to memorize its ON-state, another auxiliary MOSFET to memorise the OFF-state and give a low gate drive impedance. Isolation is provided by a pulse transformer which charges or discharges the transistor input capacitance. The pulse transformer is used as a bi-directional energy/signal channel as follows:

- During the primary pulse, energy is transmitted and the state of the Power MOSFET gate is defined.
- After primary pulse and during the steady state, an alarm signal is transmitted from secondary to primary if a short circuit occurs in the power circuit.

The main advantages of this isolated gate drive are:

A High Operating Frequency Range: This driver is able to operate from d.c. to several hundreds of kiloHertz because the transformer delivers very short pulses:

- Continuous ON and OFF states are possible when automatic refresh pulses at about 1 kHz are used.
- High frequency operation is possible because pulse time and delay time are less than 1 msec.

Duty cycle is not limited. For the same reasons as in 3.1, the duty cycle range is large: the minimum ON time or OFF time is about 500nsec enabling the duty cycle to range from 0.01 to 0.99 at 20kHz.

No floating auxiliary supply: All the switch driving energy is supplied by the pulses from the transformer, the driver does not require an auxiliary power supply.

Low energy requirement. The energy supplied by the pulse transformer is, on averange, twice the gate capacitor stored energy. The global driver energy consumption is very small, hence the cost of the gate drive voltage supply is low.

Good ground-to-gate drive isolation: Because the pulse transformer provides the isolation, the creepage distance and clearance are easily adjusted to suit the requirements of the application.

Perfect dV/dt immunity: The pulse transformer is sized so as to sustain 15 Volts for 500 nsec. This can be achieved by using a small ferrite torroid with just a few turns. The primary-secondary electrostatic coupling effects are negligible and the immunity to voltage fluctuations is perfect. An additional benefit is that a torroid of less than 10mm external diameter can be used - possibly a surface mounting version.

Low Gate Drive output impedance during OFF state: During the OFF-state, a low impedance is maintained across the gate-source of the Power MOSFET which avoids any unwanted turn on should any external dV/dt be experienced.

Short circuit protection: The secondary circuit has an automatic short circuit protection; this protection is inhibited during turn-on pulses in order to mask the diode recovery current of the power circuit. It can operate with current sensing or a shunt resistor.

Alarm signal: When the short circuit protection operates, it discharges the Power MOSFET input capacitor through the pulse transformer. Then, it operates in reverse mode and transmits an alarm signal from the secondary to primary of the pulse transformer.

FUNCTIONAL DESCRIPTION

Figure 1 shows a block diagram of the circuit. It is made up of a primary pulse generator, a pulse transformer and an isolated secondary circuit operating without any auxiliary supply.

***Secondary Circuit*:** Figures 2a to 2e allow a step by step analysis of the secondary circuit to be made as follows.

Turn ON pulse: Figure 2a shows the charge current, I_1, of the Power MOSFET T_p input capacitor when a positive pulse is applied to the pulse transformer primary. The gate voltage, V_g, rises to V_1, depending on the resistance R_C. When the primary pulse disappears, V_1 is about zero and the diode D prevents C_g from being discharged. The Power MOSFET keeps its gate charge and remains in the conducting state.

Turn OFF pulse: Figure 2b shows the Power MOSFET input capacitor discharge current, I_3, through R_d and T_d. The discharge occurs when the capacitor, C_m, is charged through D_2 by means of circuit W biased by V_2. Zener diode, D_z, is required to limit the gate-source voltage of T_d at the beginning of the negative pulse, V_2. Details of the circuit W are given in figure 2c.

Figure 1: Block Diagram

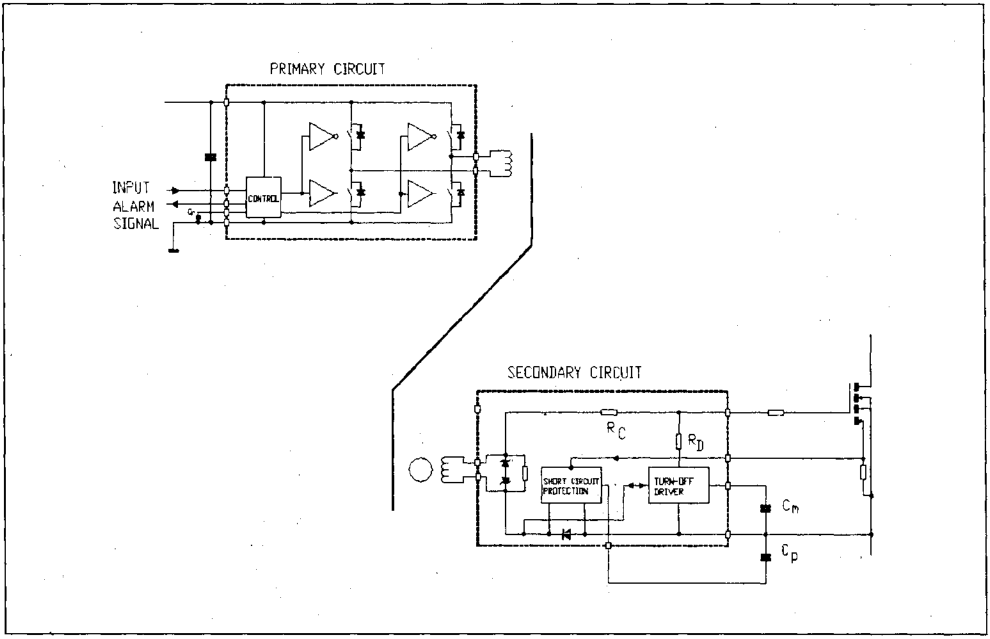


Figure 2a: Charge current for the Power MOSFET, Tp, input capacitor when a positive pulse is applied to the transformer

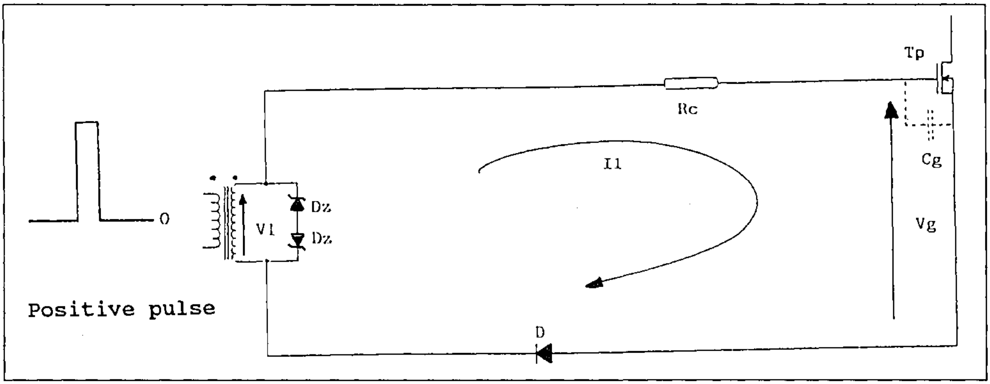
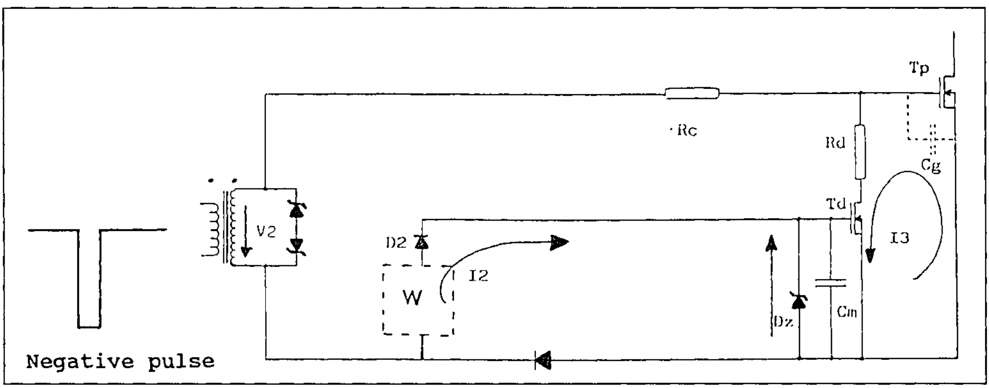


Figure 2b: Power MOSFET, T_p, input capacitor discharge current



Short circuit protection: A short circuit can be detected by means of a shunt resistor, or current sense (see figure 2d and 2e). It induces a rise of V_S which charges C_p which in turn makes T_3 conduct. The power transistor input capacitor is discharged through the pulse transformer and the transistor T_3. It produces a current pulse in the transformer secondary enabling a short circuit to be detected via the primary winding.

Diode recovery current: Generally, power switches have an associated diode recovery current at turn-on. This creates a brief over-current in the switch that requires masking from the short circuit detection circuit during this recovery time.

Due to the Miller effect, the current I_1 lasts for as long as the collector/drain voltage falls. Inhibiting short circuit detection by means of I_1 masks all the diode recovery current.

This function is carried out by T_5 which detects I_1 through R_c and makes T_4 conduct. The current I_5 flows through T_4 instead of charging C_p during the diode recovery time, avoiding spurious cunduction of T_3.

Application: Figure 3 shows the short circuit behaviour of the STHI20N50 (20A/500V IGBT). Note that the short circuit protection acts immediately after a 400nsec delay, that is, after the turn-on pulse.

Primary circuit: The primary circuit can be made by simply using a full bridge with a single primary winding. The primary control sequence is described in Figure 4.

A pair of sense diodes are located at the bottom of the left hand half-bridge; they control the demagnetisation current used to detect the short circuit alarm signal.

Figure 2c: Details of the circuit W from fig. 2b

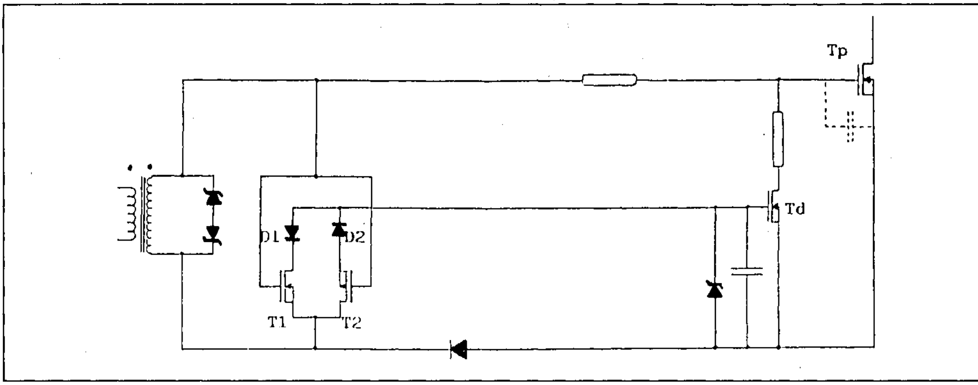


Figure 2d: Over current detection and short circuit protection

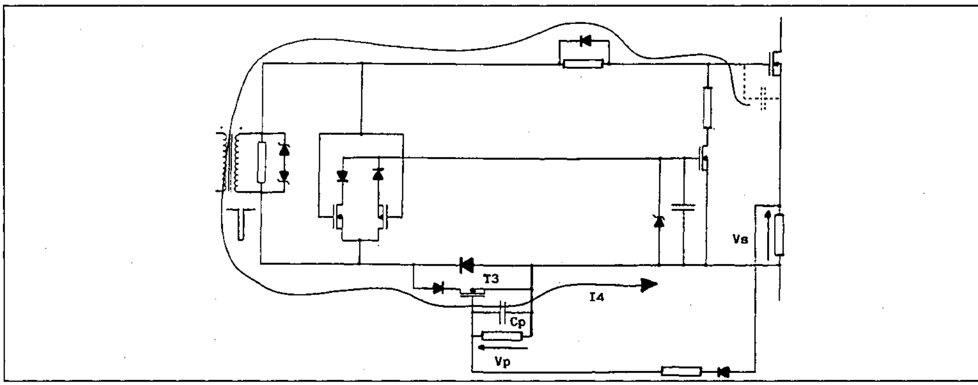


Figure 2e: Protection inhibition during diode recovery current

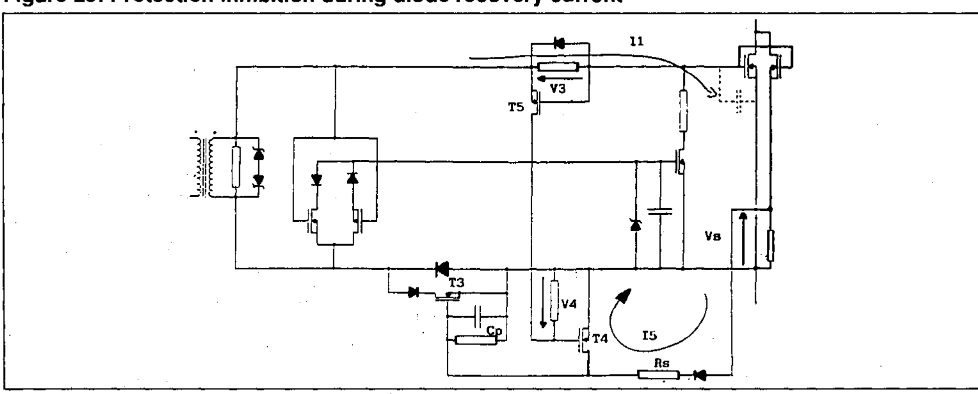


Figure 2a-2e: A step-by-step analysis of the secondary circuit

Figure 3: Short circuit behaviour at turn ON with a 20A/500V IGBT - STHI20N50.

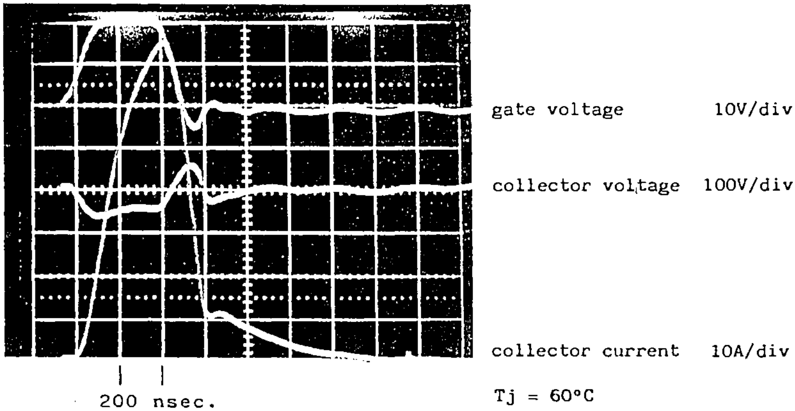


Figure 4: The primary circuit control sequence.

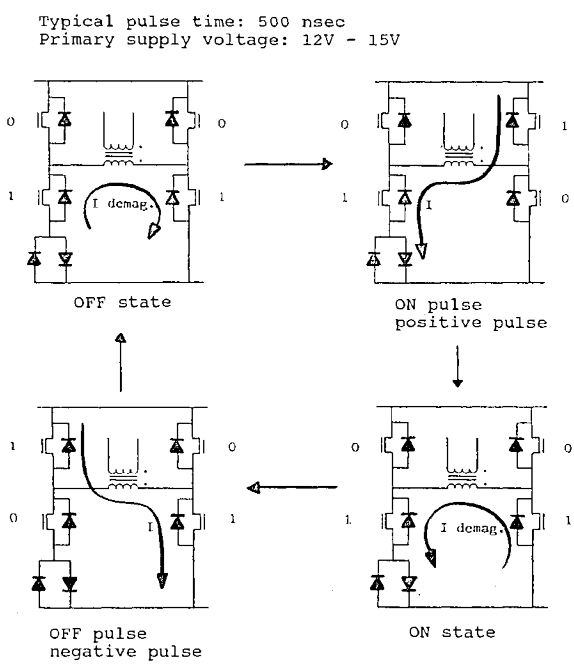


Figure 5 : The primary alarm signal - pulsed controlled driver with memory effect.

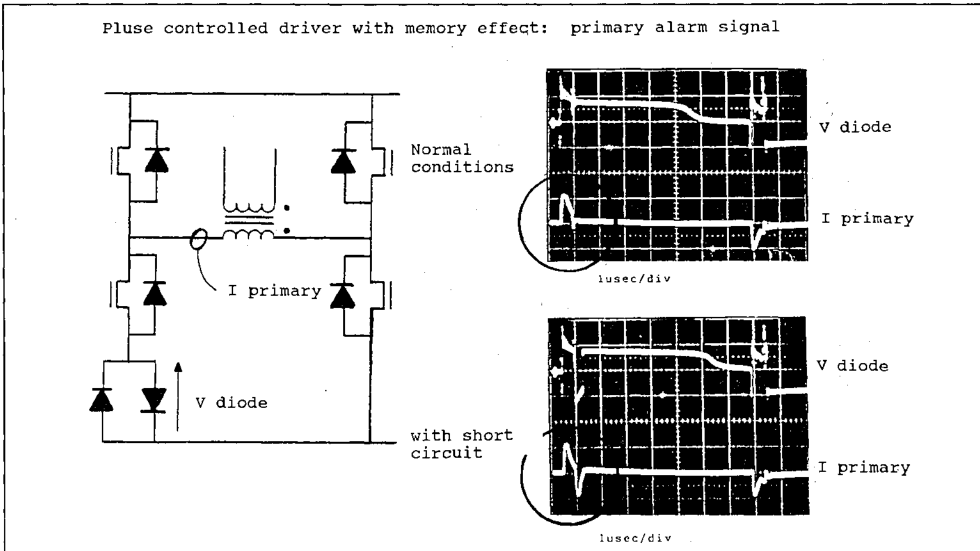


Figure 5 shows the primary circuit behaviour under normal conditions and with the power stage short circuited.

Normal conditions: The positive current pulse corresponds to the turn ON signal and is followed by the demagnetisation current. The negative current pulse is due to the turn OFF signal. It is possible to see that the voltage across the sense diode is always positive during the turn ON pulse and the corresponding demagnetisation.

Short circuit conditions: The waveforms are similar to the previous ones, except for the current after the positive pulse. Due to the discharge of the input capacitor, T_p, through the transformer secondary, a negative current pulse occurs at across the primary at the beginning of the demagnetisation, inverting the voltage across the sense diode. By sampling and latching this voltage 100nsec after the end of the turn-ON pulse, it is simple to provide an alarm signal.

If the alarm signal is not required the integrated circuit L293D, can be used to drive the pulse transformers. This is contains two full bridge drivers enabling it to drive 2 transformers. It makes an excellent interface between a digital control circuit and the two pulse transformers of an isolated bridge leg.

CONCLUSION

This new concept for a Power MOSFET driver is perfectly suited to drive floating and/or isolated switches. Moreover, it also provides important cost reduction compared to standard solutions.

Its operating mode permits a large duty cycle range, requires no floating auxiliary supply, has perfect dV/dt immunity and a short circuit protection feature that provides an alarm signal to the grounded control circuit. Lastly, it is now feasable to make a fully SMD circuit due to the availability of SMD pulse transformers.

BIBLIOGRAPHY

1) *Power semiconductors for high frequency AC/DC converters supplied on the 380/440V mains.* - L. Perier J M Charreton - Application Notes - SGS-THOMSON Microelectronics.

2) *Optimised power stages for high frequency 380/440Vac medium power switch mode supplies.* - C K Patni L Perier - Application Note - SGS-THOMSON Microelectronics.

3) *Improved transistorised high power chopper* - PCI 83 GENEVEA K Rischmuller SGS-THOMSON Microelectronics.

4) *Simplified switch mode base drive circuit with the L4974 Smart Power I.C.* - K Rischmuller Application Note - SGS-THOMSON Microelectronics.

5) *Power Transistor Application Manual* - SGS-THOMSON Microelectronics.