CHIP PAIR PROVIDES ISOLATED DRIVE FOR POWER MOSFETS IN PWM DRIVES REQUIRING 0% TO 100% DUTY CYCLE

UNITRODE'S UC3724 AND UC3725

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INTRODUCTION

Designers of power drives for PWM motor controls and switching power supplies often have to face the problem of how to drive the high-side transistor in a totem-pole MOSFET output stage. In most cases there are several of these to implement, and the problems of cost, complexity, and low efficiency tend to be discouraging. For many reasons, it is usually desirable to use N-channel MOSFET devices exclusively, and the need to drive the high-side transistor's gate to a voltage ten to fifteen volts above the upper rail can lead to complicated and often unreliable schemes.

The new chip pair UC3724/UC3725 from Unitrode offers an elegant, compact, and comparatively inexpensive way out of this dilema. To put it briefly, the two chips—together with a small pulse transformer which supplies the required isolation—employ a modulated carrier to convey both the switching power and the ON/OFF information to the MOSFET gate. The circuit of Fig. 1 shows all that is needed for fast switching of a power transistor at any of the voltages commonly found in motor control or power supply applications.

The primary chip (UC3724) generates a carrier signal, usually at a frequency of several hundred kilohertz, and applies it to the transformer primary with one of two possible duty cycles, determined by a TTL-level logic input. The output signal is delivered to the transformer by a current-sensing circuit which ascertains that the primary current reaches zero before starting each new cycle, thus preventing direct current buildup in the winding. This is done continually, at both high and low duty cycles, and has the significant consequence that the average voltage of the output signal is always zero. A properly designed transformer (see below) cannot saturate under these conditions, and there are no severe transients that can affect the response at each duty cycle change.

Because of the high carrier frequency and constantly monitored primary current, the transformer can be constructed using a high permeability ferrite core of no more than 0.5in OD. Though very small, the transformer can easily provide more than 1000V of isolation, with minimal capacitance between windings, and very low leakage inductance.

On the power circuit side, the secondary chip (UC3725) rectifies the steady carrier with an efficient full-wave Schottky bridge and stores in a small capacitor the energy needed to run its internal circuits and to deliver the husky one ampere current pulses required to charge the power MOSFET gate in a fraction of a microsecond. The incoming duty cycle, which may be either low (about 33%) or high (about 67%), is sensed by the internal circuit to determine the high or low state of the output drive. Furthermore, the same secondary IC contains a local current-sensing feature that can be used to terminate an ON command if the load current exceeds a given value. This extremely fast current-limiting circuit works in a hickcup mode, with both the current level and the fixed off-time selected by the user.

DRIVING THE MOSFET GATE

It should be noted that although the instantaneous power needed to charge the MOSFET gate from zero to 15V is relatively large if the switching time is short, the long-term average power is quite low. This is because the switching time, during which gate current flows, is necessarily small compared to the period of the PWM signal. The isolation transformer needs to transfer power to the secondary side at the average rate only, and this is why it can be of very small size.

By way of illustration, consider a large MOSFET with an equivalent gate charge of about 200 nanocoulombs. For an ON voltage of 15V, we calculate an equivalent capacity of 13nF. With the 15 ohm resistor shown in Fig. 1 in series with the gate (to limit the peak current to the rated 1A maximum), we can approximate the gate voltage as a rising exponential function of time, of the usual RC variety with which we are familiar. Thus, the gate voltage starts from zero and approaches 15V with a time constant of 10 * 13 = 130 nanoseconds.

Now, it so happens that the efficiency of charging a capacitor through a resistor is 50%, so that the energy required to charge the gate fully is equal to twice the amount stored. Consequently,

1) Energy used to charge the gate = $C * V^2$.

Using Eq.1, the energy needed per cycle turns out to be 3 microjoules, a result which could also be obtained by simply multiplying the equivalent gate charge by the gate source voltage. At a switching frequency of 30KHz, this amounts to an average gate drive power of only 90mW, even though the instantaneous peak value is actually 15W. The small transformer must be rated to handle the average 90mW—plus the low power needed to run the chip, while the secondary storage capacitor C1 supplies the high instantaneous peaks. Not that no additional energy is required to discharge the gate capacitance at the end of each ON time; at these times, the stored energy is simply dissipated locally.

THE PRIMARY SIDE: UC3724

A block diagram of the UC3724 is shown in Fig. 2. The carrier signal is generated by a retriggerable monostable multivibrator working in conjunction with the current sensing circuits of the output stages. The timing components Rt and Ct can be chosen for any frequency from 3.3KHz to 600KHz by referring to the curves supplied in the data sheet. If the chip is energized without a transformer primary connected across the two output terminals, the oscillator will not run, and the voltage at pin 1 (Ct) will remain fixed at about 2.9V. This is a normal condition, caused by the absence of current at the output dirvers. In this state the differential output voltage VA - VB is positive if pin 7 is high, and negative if pin 7 is low.

With the transformer connected to pins 3 and 5, the primary magnetizing current is sensed by one of the two current-sensing comparators to generate the signal required to trigger the multivibrator. This causes the oscillator to run, and the waveform appearing at pin 1 will be as shown in the timing diagram of Fig. 3. If we observe the output signals at pins 4 and 6 differentially, we will see the waveform labelled Va-Vb in the diagram. It has two main characteristics:

1. The duty cycle is either 1/3 (33%) or 2/3 (67%) approx.:
2. The average voltage is always zero.

While the capacitor Ct is charging, the voltage Va-Vb is just 2V lower than Vcc. During this time, the magnetizing current increases linearly with slope

2) di/dt = (Va-Vb)/L amperes per second,

where L is the primary magnetizing inductance. When the timing capacitor voltage reaches the threshold value of 2.5V, the output voltage (Va-Vb) is reversed in polarity and, at the same time reduced by one-half. With this now opposing voltage, the magnetizing current begins to decrease with a slope equal to half the value given by Eq.2, towards zero. At zero current, one of the two current-sense comparators triggers the multivibrator to start another cycle. This resets the core once per cycle, preventing saturation and protecting the chip from uncontrolled output currents.

From the above description, it is clear that the generation of the output signal depends heavily on the shape of the magnetizing current waveform. But the output current contains another component, namely the current that carries the power needed at the secondary side. The bridge rectifier at the input of the UC3725 works in our favor here, because it is essentially OFF during the half-voltage part of the cycle. For this reason, the total primary current looks like the Iprim trace in Fig. 3. For best results, the primary inductance should be chosen so as to obtain a peak magnetizing current of between 20mA and 40mA. If the chosen PWM frequency is f,

3) L = 10(Vcc-2)/f henries. (for 33mA peak Imag)

With Vcc=22V and f=200KHz, this gives L=1mH. A Ferroxcube toroidal core 204T250-3E2A, with an OD of 0.5in has the following specifications:

A1 = 3uH/turn squared; equivalent length = Le = 3.12cm.

We calculate N^2 = L/A1; N = 18 turns, and

4) Imax = H*Le/1.25*N = 69mA.

Here the current Imax has been calculated for H = 0.5 oersteds, or B = 2800 gauss approximately (see Ferroxcube Linear Ferrite catalog). With these values, this core can be used at temperatures well above 70C.

THE SECONDARY SIDE: UC3725

It can be seen from the block diagram of Fig. 4 that the transformer secondary winding supplies power to the chip through the internal full-wave rectifier bridge of high efficiency Schottky diodes. A small storage capacitor must be connected from pin 3 to pin 1 to filter out the carrier frequency and to supply peak output currents; in most cases, a 1uF ceramic type with low ESR will be adequate. The signal from the transformer is also applied to a high hysteresis comparator where the two possible incoming duty cycles are recognized.

In this discussion we will refer to pin 1 as GROUND and give all voltages with pin 1 as the reference point, even though it is rarely used at ground potential. In most applications, this pin is connected to the source terminal of a high-side power MOSFET transistor, and the UC3725 with its external circuit components ride with the load between power ground and the positive rail.

With the transformer output applied to pins 7 and 8, the circuit is ready to drive the power MOSFET if:

A. The voltage Vcc (at pin 3) is 12.6V < V3 < 35V:

B. ENABLE (pin 6) is low:

C. The voltage Vcs (at pin 4) is OV < V4 < 0.5V;

D. The voltage Vt (at pin 5) is high (about 7.2V).

If these conditions are satisfied, the OUTPUT voltage Vo (pin 2) will be controlled by the duty cycle of the signal received from the transformer and sensed by the input comparator.

The transformer cannot pass DC, and therefore the voltage Va-Vb, measured between pins 7 and 8 must have an average value of zero volts. If the duty cycle is "low" (about 1/3), the positive excursion has a shorter duration and, consequently must have a higher amplitude. This means that current will flow into pin 7 and out of pin 8 during these short pulses, and not at all during the remaining 2/3 of the period. The comparator output stays high as long as the duty cycle does not change, and the output voltage (pin 2) is held low: the power MOSFET is held OFF. Conversely, if the differential voltage Va-Vb has a "high" duty cycle, the negative voltage excursion will be higher, and the power transistor will be ON.

CURRENT LIMIT: By applying to pin 4 a voltage proportional to the current flowing through the power transistor, as shown in Fig. 1, it is possible fo turn OFF the device with a minimum of delay, thus protecting it from damage in case of shorts or other mishaps. The chip itself is capable of reacting in less than 50ns, so that the time constant of the RC filter between the MOSFET source and pin 4 will be responsible for most of the turn-off delay. This filter is usually required to prevent false triggering of the current sense comparator.

The two components Rt and Ct at pin 5 set the time during which the power device is held in the OFF state after an overcurrent condition is detected. The OFF time is

4) t = 1.28*Rt*Ct seconds.

If the current limit feature is not required, pin 4 should be grounded, and pin 5 should be left open.

LAYOUT PRECAUTIONS

Because of the high performance requirements of the applications for which the UC3724 and UC3725 were designed, these ICs offer extremely fast circuits with low propagation times. For this reason, the circuit layout in breadboarding and in the final product design should be done with care, if unnecessary problems and delays are to be avoided. A good ground plane over the circuit area—which is relatively small anyway—is always helpful. Good quality ceramic filter capacitors for Vcc in both primary and secondary circuits are mandatory. Ground loops must be shunned like the plague: it is easier to avoid them from the start than to eliminate them later.

NOTE: The name "ground loop" is an unfortunate misnomer. It has led some to believe it is enough to avoid closed loop circuits in which ground currents could conceivably circulate and cause all kinds of trouble. But the problem is quite different, and requires a different solution.

Refer to the UC3725 circuit in Fig. 1. There are several components connected to "ground", such as the capacitors from pins 3, 4, and 5, for example, You will have a ground loop if you return any of these to a point in the ground bus that is remote from the chip's ground pin, or pin 1 in this case. Depending on the current level and switching speed, even a fraction of an inch can be too far. The reason is that the ground wires (or traces) always have some small but finite amount of resistance and inductance, and it is the voltage drops due to these can often cause malfunctions.

CONCLUSIONS

With the UC3724 and UC3725, the problem of driving an N-channel power MOSFET with high voltage isolation between the low level and the power circuits can be easily handled. The chips are suitable for use in PWM amplifiers at switching rates of over 50KHz, which makes them suitable for most motor applications, as well as many power supply designs. A number of novel configurations not specifically described here will surely come to mind to experienced designers. For example, using a transformer with multiple secondaries, it is possible to have one UC3724 commutating two or more UC3725, each controlling its own power transistor.

The devices are useful also in "off the line" power stages, where all of the power transistors must be driven with isolated drivers in order to meet UL or other specifications.

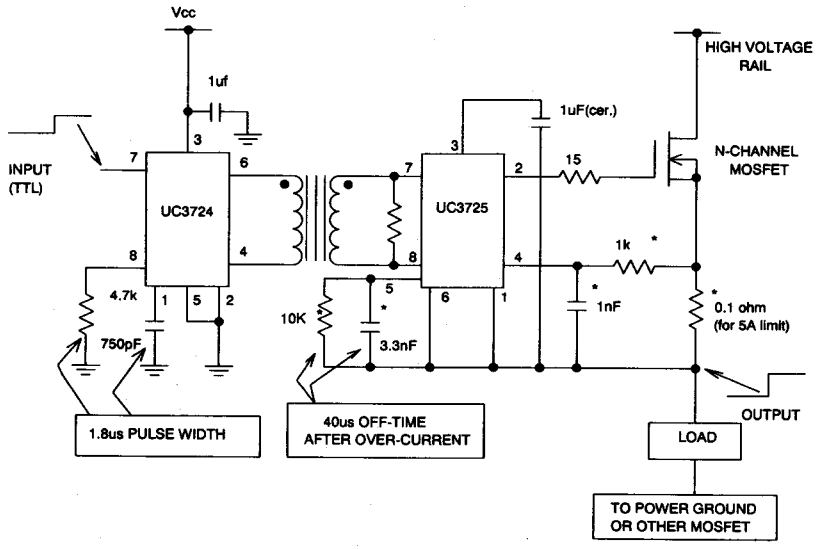

FIGURE 1: Isolated MOSFET driver. The five current-sensing components (*) can be omitted if this feature is not required.

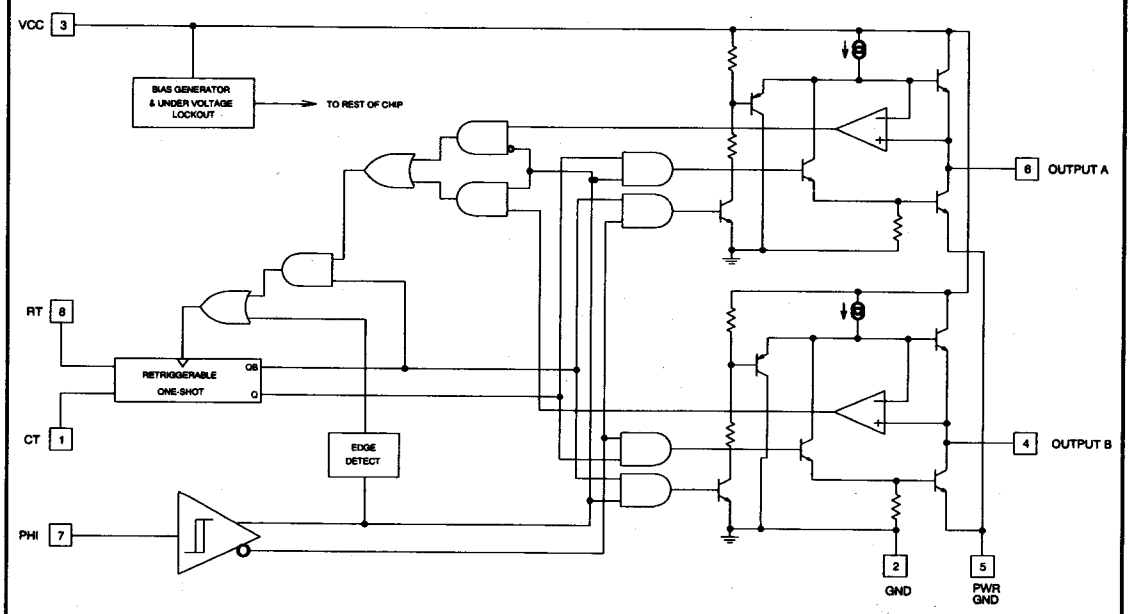

FIGURE 2: UC3724 Block Diagram

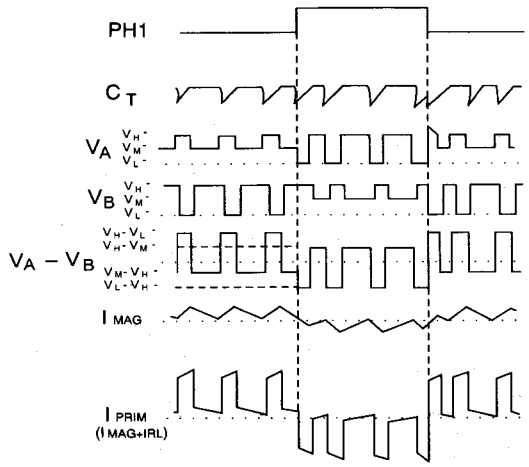

FIGURE 3: UC3724 Timing Diagram

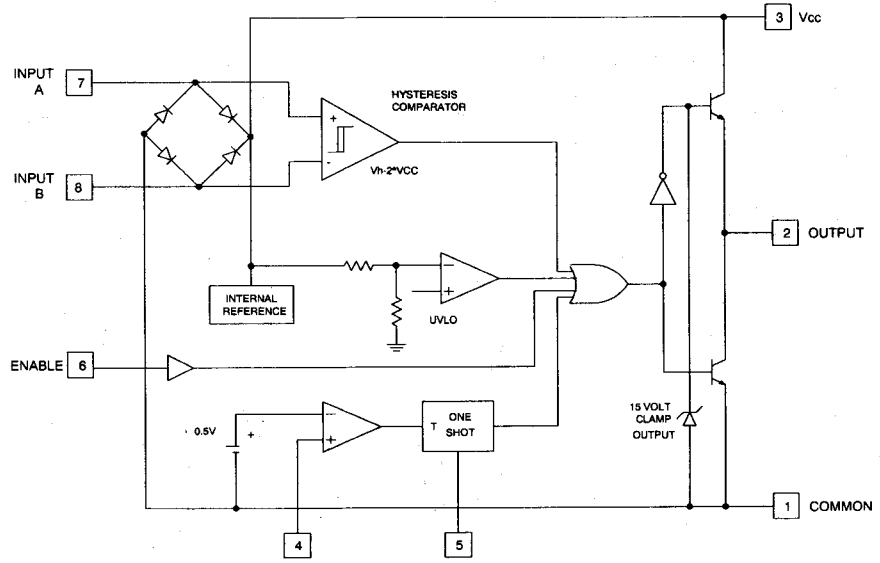

FIGURE 4: UC3725 Block Diagram

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