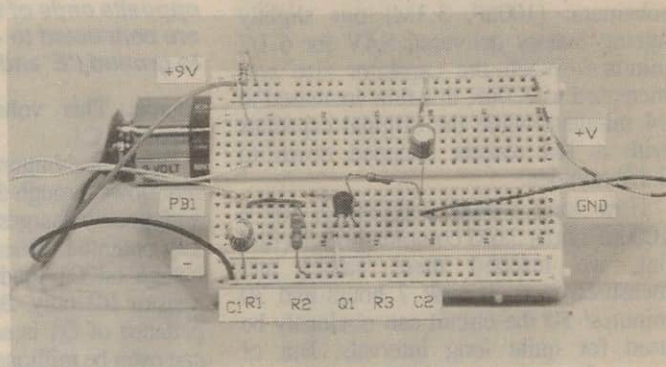


# Experimenting with Electronics

by PETER MURTAGH

## A simple battery saver

Battery-driven circuits can quickly flatten your battery, especially when you forget to turn them off! Not to worry. Attach our simple 'battery saver', and about six minutes after pressing the pushbutton it will automatically shut down the main circuit. To extend the time, just re-press the button and re-charge its 'memory'.



The photo shows how few components are needed for our auto power-off circuit. The power remains on for about six minutes after button PB1 is pressed.

Our circuits in this series have been steadily getting more complicated, so we thought it was time to produce a really simple one. At the same time we had a request from a grandfather who builds our circuits for his grandchildren. He wanted to cut down on having often to replace accidentally flattened batteries — we all know how easy it is to forget to switch off! Hence, this month's design.

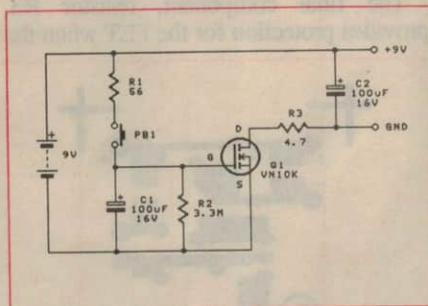
For a practical 'auto power-off' function, we need a circuit which will need negligible current in its standby mode and which can easily be kept switched fully on for intervals measured at least in minutes. Such a circuit can be built around a component called a FET (Field Effect Transistor).

Unlike normal bipolar transistors in which the load current is controlled by the base current, FETs control the load current by their gate voltage. (More about this later, in the 'Some theory' section.) This method of control means that FETs have an input impedance of around 10 billion ( $10^{10}$ ) ohms, instead of around the normal 2-3k for bipolars. So the driving circuit of a FET has only to supply negligible current — which lets us satisfy the two main requirements for our battery saver.

So, press pushbutton PB1 and charge up capacitor C1. This keeps the FET Q1 switched on for around six minutes, during which time close to the full 9V is consistently supplied to the main circuit. After switch-off, the total current drawn from the battery is so minute that it measures only a few microamps.

### Construction

A 9V battery snap is obviously the easiest way to connect the battery to the



The charge stored in capacitor C1 keeps the MOSFET Q1 turned on. Because Q1 is voltage-controlled (rather than current-controlled), Q1 discharges only through resistor R2. Hence a large discharge time-constant is possible.

circuit, and we opted for two leads with alligator clips for the output. These leads were connected to the board via PCB pins.

Solder the resistors, capacitors and FET. Refer to Fig.3 for the polarity of the two capacitors (electrolytics) and to identify the pins of the FET.

Unfortunately, the pin order on the VN10K (SGD) is the exact opposite to that on a BC548 (CBE). In the top diagram of Fig.3, it is the left hand pin (C) of the BC548 which connects to the positive rail, but the right hand pin (D) of the VN10K. Similarly, the right hand pin (E) of the NPN and the left hand pin (S) of the FET connect to ground.

Note that FET names refer to 'electron' flow — not conventional 'current' flow. That's why the drain (D) connects to the positive rail, and the source (S) to ground. Once you realise this, you can think of an N-channel FET as operating similarly to an NPN bipolar transistor, with the drain, gate and source corresponding to the collector, base and emitter.

With the FET pins sorted out, connect the pushbutton, the battery snap and the output leads. It is probably worth mounting the circuit more permanently in a box — this will make it more convenient to



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power up any other projects that you wish to use. And because the VN10K is rated at 0.8A, the battery saver can be used with many other projects, as well as those from the 'Experimenting' series.

## Changes

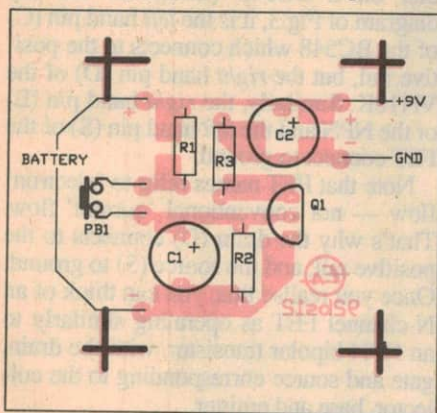
If you want to alter the time that the battery saver delivers full voltage, simply change the values of capacitor C1 and/or resistor R2. These determine the time constant (which will be further explained later in 'Some theory'). We tried several combinations:

With the values shown on the schematic (100uF, 3.3M) our slightly ageing battery delivered 8.4V for 6-1/2 minutes. When the capacitor size was increased to 220uF, this time increased to 14 minutes; while the original capacitor with a 1M resistor dropped down to 2-1/2 minutes.

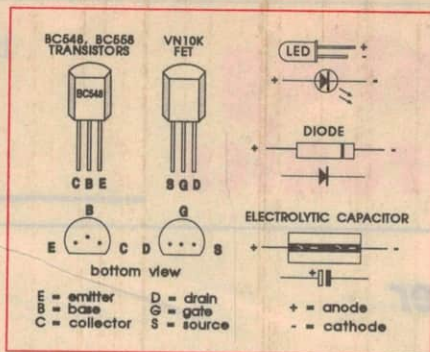
How long would you expect for a 1000uF and a 5.6M combination? To find out, we inserted these values and measured it — it took 2 hours and 30 minutes! So the circuit can obviously be used for quite long intervals. But of course for such extended times, you must allow longer for the circuit to shut down. Once the voltage started to drop after the 150 minutes, it took another 15 minutes before the load current had dropped to 500uA. Compare this with the one minute it took the original circuit to effectively switch off.

## How it works

The main role of FET Q1 is to act as a switch, to connect the output ground to the battery negative. To do this, a voltage must be applied between its gate and



**Fig.1: The component layout for the PCB.** This simple circuit has only three polarised components — the two electrolytic capacitors and the MOSFET.



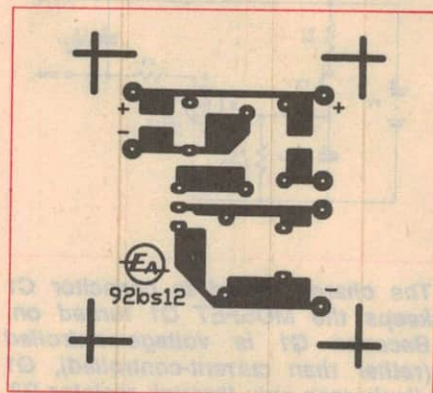
**Fig.3: The component leads identification diagram for the polarised components used in the circuit.** Note the reversed order of the leads on the BC548 and VN10K — the pins at opposite ends of the two components are connected to +V ('C' and 'D'), and to ground ('E' and 'S').

source. This voltage is provided by capacitor C1.

When pushbutton PB1 is pressed, current flows through the limiting resistor R1 and quickly charges up C1 to the full battery potential. When PB1 is released, the charge on C1 gradually leaks away via resistor R2 only. Because the input impedance of Q1 is so extremely high, R2 can even be millions of ohms in value and still be very much smaller than Q1's gate-source resistance. So we can ignore Q1 when calculating the time constant for the discharging of C1.

The second capacitor C2 is included in the circuit to reduce the output impedance of the battery, which is made even more desirable because of the presence of the series resistor R3. The capacitor smoothes the output, by acting as a reservoir to top up brief high-current demands. The battery can only deliver quite a small steady or average current, but by placing the capacitor in parallel, it becomes capable of supplying quite large — though brief — pulses.

The final component, resistor R3, provides protection for the FET when the



The PCB pattern is shown actual size to allow you to etch your own board.

circuit is first turned on. If the load circuit has bypass capacitors (like C2), these will provide an effective shortcircuit until they charge up. The 4.7 ohm value of R3 has been chosen to limit the startup current to about 2A (at 9V), which is the pulsed current rating for the VN10K FET.

Any other FET can replace the one we used, provided that it is an N-channel, enhancement mode power FET. Ours was chosen simply because it was the cheapest we could find. (In fact, DSE sold us a VN0106, which is an equivalent of the VN10K.)

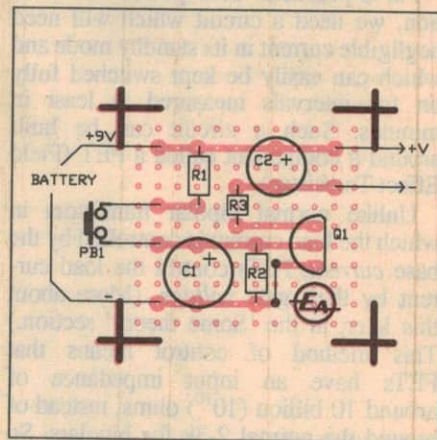
## Some theory

First of all, a little more about the differences between the working of a bipolar NPN transistor and an N-channel FET.

In an NPN transistor, two types of charge carrier are involved. Holes are injected into the base, and these holes induce many electrons to flow in the collector (or load) circuit. The main electron flow (which is really the current) is from the emitter to the collector, and this is controlled by the much smaller current that enters by the control electrode, the base.

However, in an N-channel FET, only one type of charge carrier (electrons) is involved. The electron flow is from source to drain, along a channel of N-type material. This channel is sandwiched between two P-regions which form the gate, and can be used to alter the depletion layer and 'pinch off' the current. It is actually an electric field applied between the gate and the source that controls the load current.

If you use a reverse-biased N-channel FET (a JFET), you actually have to make the gate more negative than the source, to pinch off the main current. This means that without any gate bias the FET



**Fig.2: The stripboard layout.** Since all resistors are shown as smaller than 0.4", it is easier to mount these components vertically.



remains on. But with the enhancement mode MOSFET that we have used, a positive gate voltage is required to turn the transistor on.

Now for our second bit of theory — time constants. A capacitive time constant is the time it takes a capacitor to charge up via a resistor to 63% of its total potential, or discharge to 37% of its starting potential. Because C1 charges up very rapidly via the 56-ohm resistor R1, we will consider only its slower discharge via R2.

If you were wondering where the above percentages come from, remember that capacitor C1 discharges exponentially. And the value of  $e^{-1}=0.37$ ! In practical terms, an exponential discharge means that the capacitor's stored charge decreases very quickly to start with, but this drop-off rate becomes continually slower as the discharge continues. After one time constant, the remaining charge is down to 37% of the original value.

To calculate the numerical value of a time constant (in seconds), simply multiply the value of the capacitor (in Farads) by the value of the resistor (in ohms). Use the values shown on the schematic, and you will find that this give a time constant of 5m 30s.

Measurements made on our circuit

## PARTS LIST

### Miscellaneous

PCB 38x36mm, coded 92bs12  
9V battery  
9V battery snap  
2 alligator clips  
hookup wire, solder, etc.

### Resistors

All 1/4W, 5%  
1 56 ohm R1 green-blue-black  
2 3.3M R2 orange-orange-green  
1 4.7 ohm R3 yellow-purple-gold

### PC-mount electrolytics

2 100uF, 16V C1,C2

### Semiconductors

1 VN10K N-channel FET Q1

showed that the capacitor had to drop from its original 8.2V down to 2.0V before the FET started noticeably to turn off. This means that the capacitor had to discharge to 24.4% of its original voltage, which is more than one time constant. By calculating the natural log of 8.2V/2.0V, we find that it is actually 1.4 time constants —  $\ln 4.1=1.4$ .

Calculate the theoretical times for the various R/C combinations, and compare them with the actual measured times (in brackets):

220uF/3.3M 16m56s (14m)  
100uF/3.3M 7m42s (6m30s)  
100uF/1.0M 2m20s (2m30s)

Because of the high input impedance of the FET the two columns of results are very close. We can blame the difference on the leakage from the electrolytic capacitors. This shortens the longer time intervals, especially with larger capacitor values.

Why not do the calculations for our very extended timeout? — remember that our measured time for a 1000uF capacitor and a 5.6M resistor was 2-1/2 hours. Check that the theoretical time for the capacitor to drop from 9.0V to 2.0V is  $2h20m23s$ , or 1.5 time constants.

I hope you have found this extra bit of theory interesting. Normally the editor doesn't give me enough space to diverge like this!

## Transparencies

As usual, a high contrast, actual size transparency (negative) for the PCB used in this circuit is available for only \$2. This will allow you to etch your own printed circuit board. This special price applies for transparencies for all projects in this series only. Write to EA's reader services division.

Happy experimenting — and please send us your comments on the circuits we have published, as well as ideas for future projects. ♦