Two bright ideas for solar panels

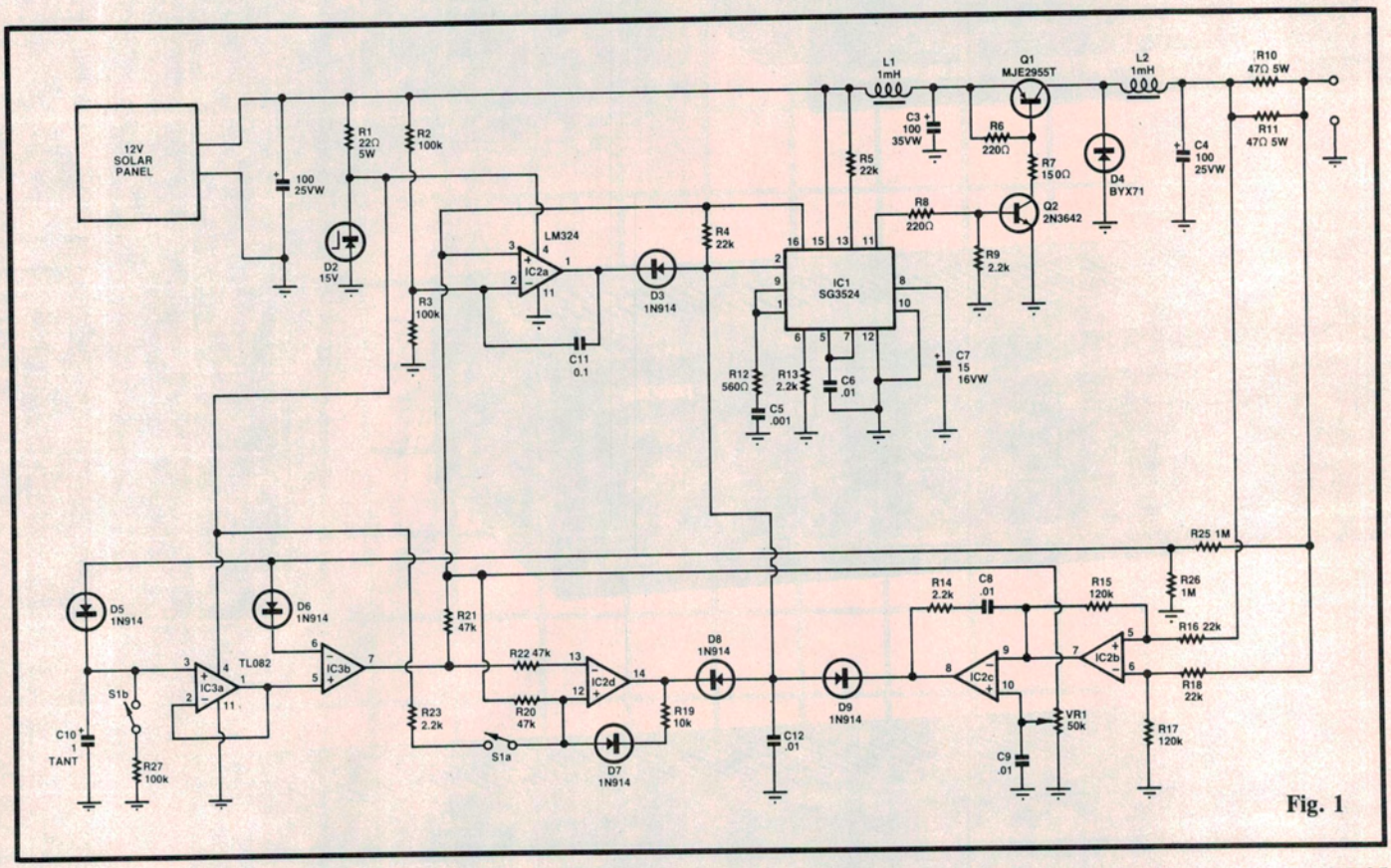

Fig. 1

Solar powered NiCd charger

This efficient charger circuit will allow a 12V solar panel to charge any number of NiCd cells (up to 10 in series) at a preset current level. One 1.1Ah cell can be charged in about 15 minutes at 3.3A while six cells will take approximately 1.5 hours.

by PAUL THOMPSON

In this circuit an SG3525 pulse width modulation control IC, configured with current feedback, is used to vary the output current. Because the switching circuit has negligible losses, almost all the available power can be transferred to low impedance loads.

Fig. 1 shows the circuit diagram. The output of the panel is fed to R1 and ZD1 which limits the maximum IC supply rail to 15V. Note that R1 must be small to limit its voltage drop when the main rail falls below about 15V.

With no load applied to the charger, most of the panel's output will be dissipated in R1 and ZD1 which will limit the main rail to about 18V.

Automatic cutout

The automatic cutout circuit is based on a voltage divider consisting of R25 and R26, which charges capacitor C10 via D5. During the charging cycle, the NiCd cell voltage rises to a certain point and then begins to fall as the cell is overcharged. It is at this point that the voltage on C10 becomes larger than the divider voltage.

This voltage is applied via voltage follower IC3a to pin 5 of comparator IC3b. This switches the output of IC2d low which, in turn, pulls the control line to pin 2 of IC1 low via D8, thus shutting off the charger. Positive feedback via D7 and R19 now holds the output of IC2d low until it is reset by S1a.

The other pole of S1 (S1b) is used to discharge C10 in readiness for the next charging cycle.

In operation, S1 may be closed and the output current adjusted into a short circuit using VR1. The NiCd cells can

then be connected and S1 opened.

In addition to the zener regulator, the main rail is further regulated by the action of comparator IC2a. This limits the pulse width so that the load cannot drag the main rail below 10V.

The third control circuit is based on IC2b and IC2c, and provides adjustable current limiting. Differential amplifier IC2b monitors the voltage across R10 and R11. When its output voltage at pin 7 exceeds the voltage preset by VR1, pin 8 of IC2c goes low and pulls pin 2 of IC1 low via D9.

In the absence of a control signal, the SG3525 (IC1) has its control pin (pin 2) pulled high via R4 so that it can provide the maximum pulse width to drive Q2 and Q1. Note that LEDs can be used in place of the diodes to give a status display. Note also that only one of the control circuits will pull pin 2 of IC1 low at any given time.

The supply to the main switching transistor (Q1) is prefiltered by L1 and C3 to prevent noise from affecting the control circuitry. Q1 dumps current into L2 which free wheels via D2 when Q1 is off. C4 provides filtering for the output. To ensure stability of the current loop (the primary control loop), the error amplifier (IC2c) is compensated by R14 and C8.