Programmable charger fills capacitor banks

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Designed for the use with a pyrotechnic pulse generator, the charger in **Figure 1** uses low-cost components to charge the C_1 capacitor bank to a voltage as high as 75V, or to 25V in a few seconds. A 555 timer, IC_1, controls a flyback converter via the Q_1 transistor switch. The converter draws its charging current from a 5V supply. The 555 turns Q_1 on until T_1's primary current reaches approximately 3A, as detected by comparator IC_{2A}, which turns IC_1 off. Then, Q_2 also turns off, and C_2 charges through R_1 and R_2, thereby setting the off-time of the charger cycle. IC_{2D} starts the new cycle by triggering IC_1.

Because R_1 connects to the charger output (V_C), as C_1 charges, the off-time decreases. The secondary conduction time decreases as V_C opposes T_1's flux. But the flyback converter transfers no charge when T_1 is not conducting current. To minimize this no-charge time, the off-time decreases with V_C. R_2 is necessary for start-up, when V_C is 0V and cannot charge C_2. A digital input (charge) turns the charger on and off.

The target voltage on C_1 depends on the duty cycle of a 5V CMOS-level pulse applied to the PWM input. A 5-kHz PWM waveform has a scale factor of 0.75V/%. A 100% duty cycle produces a 75V target voltage. IC_{2C} detects when this voltage is reached and turns the charger off through D_1. IC_{2C}'s output ($\overline{\text{Charged}}$) can also indicate the completion of charging. If you use this output as a computer input, you should monitor it in a loop, because it is unasserted during recharge. R_3 provides hysteresis, and, as C_1 leaks charge and V_C decreases, IC_{2C} changes output state and charging commences, to keep C_1 "topped off." (DI #2260). EDN

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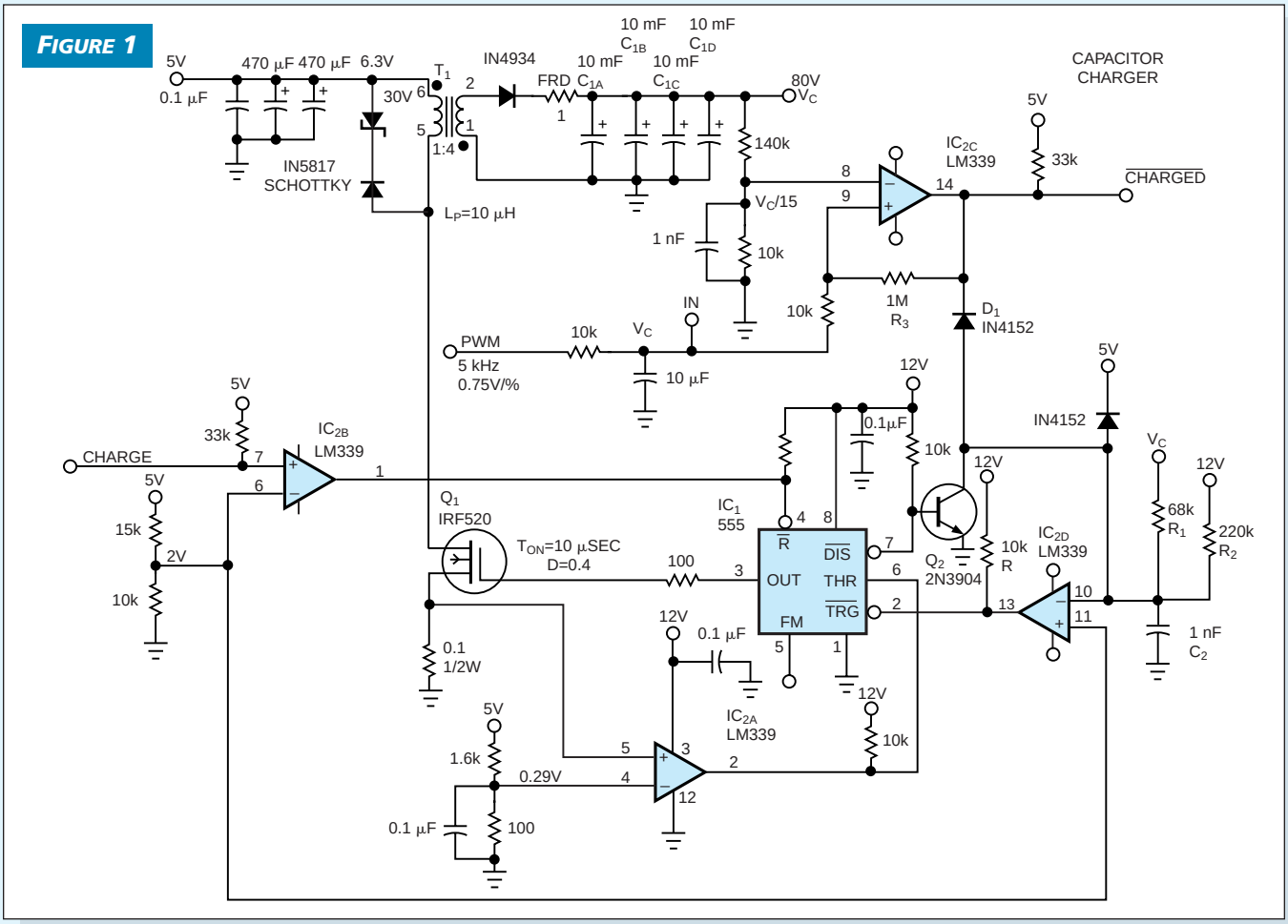
FIGURE 1



The duty cycle of a CMOS pulse train determines the target charged voltage for a bank of high-energy capacitors.