Application Note AN2309

Low-Cost, Two-Cell Li-Ion/Li-Pol Battery Charger with Cell-Balancing Support

Author: Oleksandr Karpin
Associated Project: Yes
Associated Part Family: CY8C24x23A, CY8C24794, CY8C27x43, CY8C29x66
PSoC Designer Version: 4.2 SP2
Associated Application Notes: AN2107, AN2258, AN2267, AN2294

Abstract
This Application Note describes a low-cost, two-cell Li-Ion/Li-Pol battery charger. An effective cell-balancing algorithm during both charge and discharge phases is presented. This charger can be used either as a standalone application to charge a battery pack with two serial connected Li-Ion/Li-Pol batteries or embedded in residential, office, and industrial applications.

Introduction
A modern portable system requires more operating voltage than a single-cell Lithium-ion (Li-Ion) or Lithium-polymer (Li-Pol) battery can provide. A serial connection results in a pack voltage equal to the sum of the cell voltages. To increase the battery pack capacity, the cells are connected in parallel. For many applications, two cells in series are sufficient, with one or more cells in parallel. This combination gives nominal voltage and the necessary power for laptop computers as well as medical and industrial applications. Problems can occur when the cells have different capacities or charge levels. During charging or discharging, the cells in the battery pack do not have matched voltage per cell. Therefore, the battery pack is not balanced. The unbalanced charge between cells causes the following problems:

- Reduced overall battery pack capacity to the value of the cell with the least capacity. During the charge process, this cell reaches the maximum charge level before the other cells, and during the discharge process this cell will be depleted before the other cells in the pack.
- Reduced overall battery pack life. The charge or discharge of cells at different values increases pack imbalance.
- Cell damage, which occurs if the charger monitors only the summary voltage. For example, if the lower cell has a capacity deficiency of at least 10 percent, its cell voltage begins to rise into the dangerous area above 4.3 volts. This can result in additional degradation of the cell or a safety system response that greatly reduces pack capacity.

This Application Note describes a two-cell Li-Ion/Li-Pol battery charger. An effective cell-balancing algorithm is designed. It avoids the issues that appear in battery packs with two cells in series. Through modification of the configuration parameters, the cell-balancing algorithm can easily be adapted for various applications and selected batteries. The unique architecture of the PSoC® device provides an integrated hardware solution for a two-cell battery charger and a flexible *µC*-based, cell-balancing algorithm with minimal external components at a very affordable price. The CY8C24x23A PSoC device family used in this implementation reduces the total device cost even further.

When the user wants to use algorithms for the latest charging or cell-balancing technologies, only the firmware has to be modified. PSoC Designer's in-circuit and self-programming capabilities make these operations simple.

Specifications for a two-cell Li-Ion/Li-Pol battery charger with cell-balancing support are given in Table 1.

Table 1. Specifications for Two-Cell Li-Ion/Li-Pol Battery Charger with Cell-Balancing Support

Item	Item Value
Battery Charger Parameters	
Built-In Battery Charger Type	Two-cell Li-Ion/Li-Pol battery charger
Power Supply Voltage	10…14V
Power Consumption	35 mA
Battery Current Measurement Error (Not Calibrated)	5 percent
Battery Voltage Measurement Error (After Calibration)	0.5 percent
Battery Thermistor Resistance Measurement Error	5 percent
User Interface	2 LEDs
PC Communication Interface	RS232
PC Communication Speed	115200
Cell-Balancing Parameters	
Cell-Balancing Algorithms	1. During charge phase 2. During discharge phase
Cell-Balancing Configuration Parameters	o Cell-balance circuit resistors nominal o Cell-balance interval parameter o Minimum cell-balance parameter for charge phase o Minimum cell-balance parameter for discharge phase o Minimum charge current value when cell balancing is allowed o VMID value for discharge phase (voltage of middle charged state)
Minimum Cell Balancing During Charge Phase	Equal to the voltage measurement error value (15 mV-30 mV)
Minimum Cell Balancing During Discharge Phase	Equal to the voltage measurement error value (15 mV-30 mV) plus the internal impedance error (10 mV-30 mV)

Cell-Balancing Foundation

This section describes the fundamentals of cell-balancing techniques. Cells are considered balanced when:

$$Q_{cell1} = Q_{cell2} \quad \textbf{(1)}$$

The value Q_{cellN} is the charge of cell N. The equation for the charge is:

$$Q = I \times t = C \times V \quad \textbf{(2)}$$

Therefore, Equation (1) can be transformed into the following equation:

$$C_{cell1} \times V_{cell1} = C_{cell2} \times V_{cell2} \quad \textbf{(3)}$$

The value V_{cellN} is the electro chemical potential of the fully charged cell. The V_{cellN} potential for a given set of electrodes is fixed and does not change from cell to cell. When two cells are unbalanced, the following is true:

$$Q_{cell1} \neq Q_{cell2} \quad \textbf{(4)}$$

$$C_{cell1} \times V_{cell1} \neq C_{cell2} \times V_{cell2} \quad \textbf{(5)}$$

But V_{cell} does not change from cell to cell. Therefore, the cells are unbalanced if:

$$C_{cell1} \neq C_{cell2} \quad \textbf{(6)}$$

Equation (6) shows two cells that have different capacities, which is one cause of cell imbalance. A difference in cell-charge levels, which can be identified by using Equation (4), is the second cause of cell imbalance. For both kinds of mismatches in the battery pack – different cell capacities and difference cell charge levels – the highest voltage cell shows relative charge redundancy and must be shunted during the charging/discharging process. This is the heart of the cell-balancing issue.

The main reasons for variation in cell capacity are the following:

- Variations in cell assembly. Today's factory manufacturing of cells produces Li-Ion battery backs with cell capacity matched to 3 percent.
- Different rates in cell degradation. The self-degradation rate is 30 percent at 500 cycles, which equals 0.06 percent per cycle. But individual cells degrade differently depending on temperature, charge voltage, and the particular self-degradation process. For example, a cell with a lower capacity is exposed to a higher charge voltage, which degrades it faster, further reducing its capacity and increasing the pack imbalance.
- Temperature gradient across the battery pack. Temperature mismatches of 15 degrees Celsius can cause up to 5-percent capacity differential among cells. Such a temperature gradient is relatively common in densely packed products where multiple heat sources are located close to the battery pack. An example of this is a laptop computer.

The main causes of variation in cell charge levels are:

- Variations in self-discharge rates. Even at room temperature, two similar cells will self-discharge at different rates, resulting in a mismatch. For example, one cell could lose 3 percent per month, while another cell loses a different amount.
- Variations in internal cell impedance. These impedance variations cause otherwise similar battery cells to have different charge acceptance levels. This error is very minute (about 0.1 percent).

Cell balancing is accomplished by connecting a parallel load to each cell that must be balanced. Typically, a series combination of a power transistor (MOSFET) and a current-limiting resistor are connected in parallel to each cell. If a cell has a higher voltage than the other cells, the bypass load to the cell is connected by closing the MOSFET so that a fraction of the charging current bypasses that cell. It is possible to balance the cells during the discharge phase, the charge phase, or both phases.

Balancing the charge levels among cells must be done during the charge or discharge phase. This balancing process is simple and has been well investigated. Balancing the cells' capacity variation must be done during both the charge and discharge phases. Cells with different capacities must be charged or discharged by using an absolute value rather than a relative value. The process of balancing cell capacity variation is difficult to implement in practice and is not intuitively obvious.

The charge in dV/dQ for Li-Ion batteries has a maximum level when the cells are nearly fully charged or discharged. It takes less time to correct voltage mismatch during this period of complete or nearly complete charge/discharge than during the middle period of battery charge/discharge. Thus, it is advisable to perform the balancing routine when the cells are nearly fully charged or nearly fully discharged. See also Cell-Balancing Algorithm.

The cell-balancing technique is shown in Figure 1.

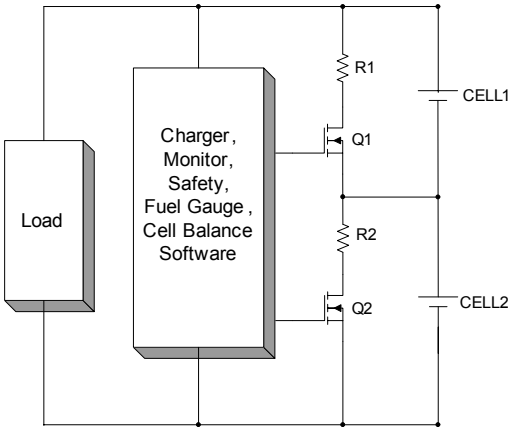


Figure 1. Cell-Balancing Technique Schematic

The balancing circuit is represented by (R1, Q1) and (R2, Q2). These transistors and resistors dissipate energy and control the amount of balancing current.

If cell balancing is performed during the charge phase, the charge current on the balanced cells is reduced on the shunted current value (Equations (7) and (8)) and remain unchanged on other cells:

$$I_{balN} = \frac{V_{cellN}}{R_N + R_{QN}} \quad \textbf{(7)}$$

$$I_{chargeN} = I_{charge} - I_{balN} \quad \textbf{(8)}$$

The value I_{balN} is the current that flows through the balancing circuit of the cell N, and V_{cellN} is the battery electro chemical potential. The value R_N is the balancing resistor, and R_{QN} is the transistor resistance. The value $I_{chargeN}$ is the charge current of cell N, and I_{charge} is the battery pack charge current.

If cell balancing is performed during the discharge phase, the current that flows through the balancing circuit depends on the system load resistance. If the load resistance is high, by comparison with a balancing circuit resistance, most of the discharge current flows through the balancing circuit. But if the load resistance is low, most of the discharge current flows through the load, making the balancing operation less efficient.

The current that flows through the balancing circuit is shown in Equation (7) and the equivalent discharge resistance is equated as follows:

$$R_{dischargeN} = \frac{(R_N + R_{QN}) \times R_{load}}{R_N + R_{QN} + R_{load}} \quad \textbf{(9)}$$

The value $R_{dischargeN}$ is the equivalent discharge resistance of the balanced cell N, and R_{load} is the load resistance.

Components for the cell-balancing circuit are selected by taking the following factors into account:

- **Amount of Imbalance**: This factor is described earlier in this section and consists of variations in capacity and charge level. Typically, cell imbalance is about 1 percent. An imbalance as great as 5 percent to 15 percent can occur only with a high temperature gradient or if a battery pack has been stored and not used for a long period of time.
- **Cell Balancing Time**: If *C* is the cell capacity and V_b is the battery voltage, and the requirement is to eliminate the amount of imbalance φ (in percent) in 1 hour of balancing time, then the power dissipation on balancing circuit P_{bal} is as follows:

$$P_{bal} = \frac{C \times V_b \times \varphi}{100\%} \quad \textbf{(10)}$$

For example, balancing the cells for 1 hour with a battery capacity of 2000 mAh and an imbalance of 15 percent results in the following approximate amount of power dissipation on the balancing circuit:

$$P_{bal} \approx \frac{2000mAh \times 4.2V \times 15\%}{100\%} = 1.26W \quad \textbf{(11)}$$

Thus, there is a trade-off between the rate of balancing and power dissipation. Faster balancing provides more options and flexibility, but it also results in increased power dissipation, which increases cost and board space. The one charge/discharge period can be selected as a favorable time for cell balancing.

- **Cell Capacity**: If *n* is the count of cells connected in parallel, *C* is the cell capacity, and δ is the amount of imbalance in percent (capacity and charge level variation), then the highest required balancing current during 1 hour is the following:

$$I_{bal} = \frac{C \times n \times \delta}{100\%} \quad \textbf{(12)}$$

For example, the initial balancing level is:

$$I_{bal} = \frac{2000mAh \times 2 \times 15\%}{100\%} = 600mA \quad \textbf{(13)}$$

If the balancing circuit resistance is set to equal 100Ω, then:

$$I_{bal} = 4.2V / 100 = 42mA \quad \textbf{(14)}$$

$$P = 4.2V \times 0.042A = 0.1764W \quad \textbf{(15)}$$

Using a 4-hour discharge time and a 2-hour charge time during one complete discharge/charge cycle with full time cell balancing on both phases, $42\ mA*(4+2)=252\ mA$ is removed from one unbalanced cell. Therefore, the balancing level from this example can be removed during three discharge/charge cycles with a balancing circuit resistance of 100Ω or during one complete cycle with 40Ω.

For maximum cell balancing, use a balancing circuit resistance of 40Ω to 200Ω and perform cell balancing during both charge and discharge phases. Note that the overnight conditioning cell-balancing algorithm is not implemented in this project. The reason is that the CY8C24xxxA device used in this implementation does not have enough ROM memory space. If the user chooses another PSoC device family for the same project, the overnight conditioning cell-balancing algorithm can easily be added (see AN2258, "Cell Balancing in a Multi-Cell Li-Ion/Li-Pol Battery Charger"). But for most applications it is not necessary to use this algorithm.

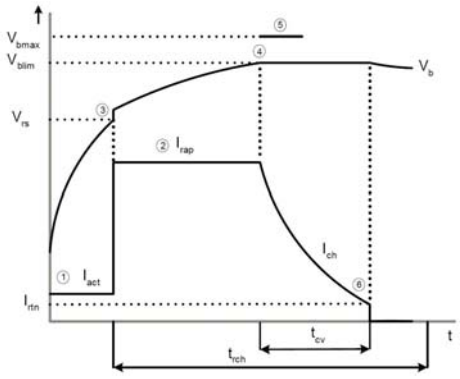
The cell-balancing technique is explained in detail in AN2258, "Cell Balancing in a Multi-Cell Li-Ion/Li-Pol Battery Charger."

Two-Cell Battery Charger Hardware

Li-based batteries use a two-stage charge profile (activation and rapid-charge). If the battery voltage is less than 2.9 to 3.0 volts per cell, the battery must be activated first. In the activation stage, the battery is charged with a constant current (0.05-0.15 CA, where CA is the nominal battery capacity) until the battery voltage reaches a predefined level. The activation charge time-out is set to 1.5 to 2 hours. The activation charge can diagnose battery health and identify troubles such as damaged or shorted cells.

The rapid-charge stage starts after the activation charge finishes without error. This stage consists of two modes: *constant current* and *constant voltage*. When the battery voltage is less than the predefined level (4.1V or 4.2V depending on battery type), the charge is processed in constant current mode (0.5-1.0 CA). When the battery voltage reaches this level, the charge source switches to constant voltage mode and the charge process is terminated when the current drops below a predefined limit (0.07-0.2 CA).

The rapid-charge stage must be protected by time limits. The rapid-charge time is limited to 3 hours. The charge profile for Li-Ion/Li-Pol batteries is shown in Figure 2. The technique to charge Li-Ion and Li-Pol batteries is explained in detail in AN2107 "A Multi-Chemistry Battery Charger."



Legend:

I_{ch} - Battery charge current
① I_{act} - Battery activation charge current, 0.1-0.2 CA
② I_{rap} - Battery rapid charge current 0.7-1 CA
V_b - Battery voltage
③ V_{rs} - Rapid start voltage, typically 3 V/cell
④ - Constant-current / constant voltage switching point
⑤ V_{max} - Emergency shutdown voltage, 4.3 V/cell
⑥ - Rapid charge termination current typically 0.1 CA
⑦ T_{rmax} - Battery rapid charge maximum temperature, 45 °C
⑧ T_{rmin} - Battery rapid charge minimum temperature, 0 °C
T_b - Battery temperature
t_{rch} - Rapid charge termination time
t_{cv} - Constant voltage charge time

Figure 2. Li-Ion/Li-Pol Battery Charge Profile

A two-cell battery charger structure with cell-balancing support is shown in Figure 3. Similar battery charger structures are explained in detail in AN2258, AN2294, and AN2267. Note that the fuel gauge function can easily be added to this project without changing any hardware: It is only necessary to switch from the CY8C24423A to a PSoC device with more program memory. The main fuel gauge calculation parameters are described in AN2294, “The Li-Ion/Li-Pol Battery Charger with Fuel Gauge Function.”

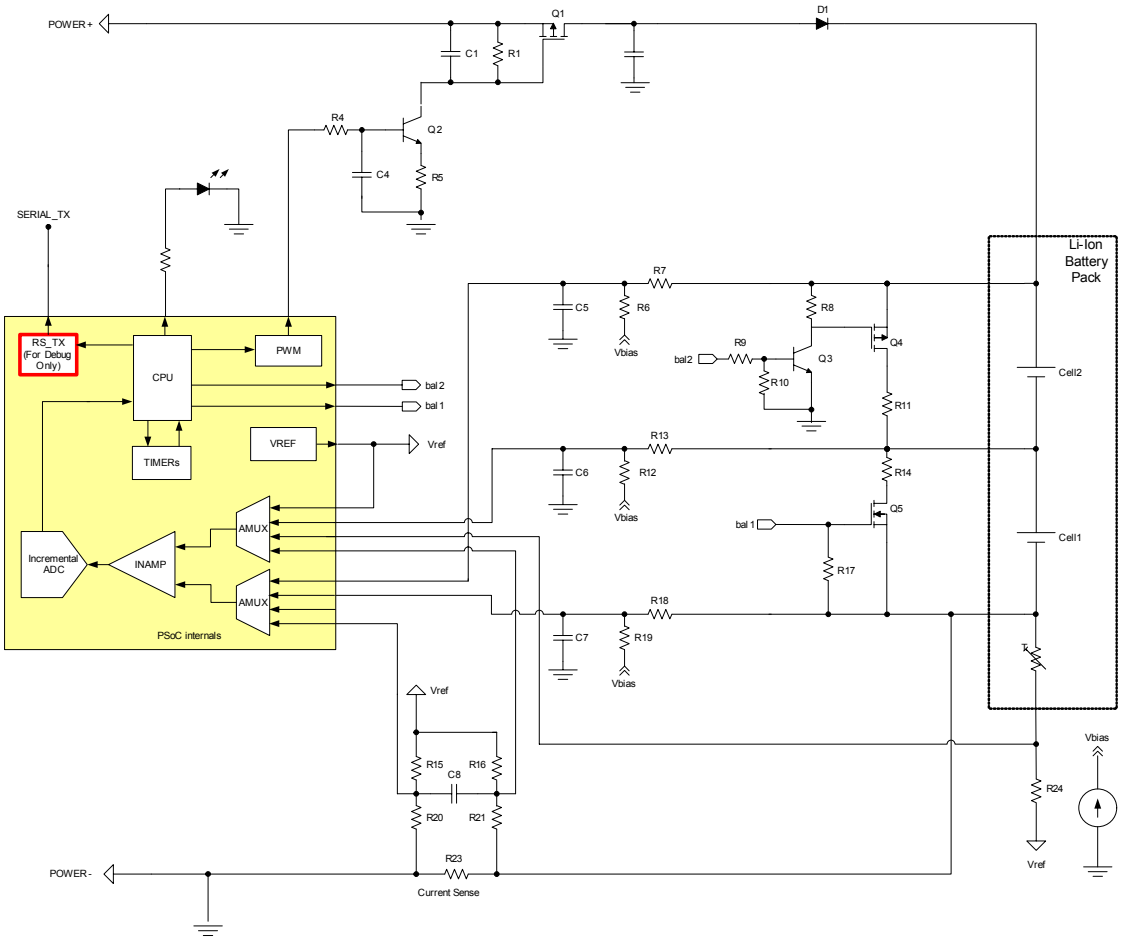


Figure 3. Two-Cell Battery Charger with Cell-Balancing Support

The following abbreviations are used in Figure 3:

RS_TX – RS232 transmitter for debug purposes (uses external level translator). It monitors temperature, voltage, current and cell-balancing statistics. RS_TX is used only in the debug stage and may be removed in the released product.
CPU – Central processor to implement charge and cell-balancing algorithms, and perform charge control functions.
PWM – Pulse width modulator to regulate the charge current.
VREF – Reference voltage source.
TIMERs – Several timers are used by the CPU in charge and cell-balancing algorithms.
Incremental ADC – Analog-to-digital converter to digitize the analog signals.
INAMP – Instrumentation amplifier to measure charge voltage, current and temperature.
AMUX – Analog multiplexers.

Figure 3Figure 3 also contains a two-cell Li-Ion battery pack, a linear regulator (based on Q1, Q2), a cell-balancing circuit (based on Q4, Q5), a current-sense resistor, and other elements that allow the PSoC device to use and interpret battery current, voltage, and temperature.

Device Schematic

The schematics shown in Figure 4 and Figure 5 constitute a complete two-cell battery charger.

A signal from the PWM goes to the RC-filter, which consists of resistor R4 and capacitor C4. A constant voltage signal proportional to the PWM duty cycle value forms at the Q2 gate. Therefore, the PWM and RC-filter is a simple implementation of a PWM-DAC. The bipolar transistor Q2 is driven by an analog signal from the PWM-DAC. This bipolar transistor and resistors R1 and R5 form a resistive divider. Therefore, the voltage drop on the resistor R1 is directly dependent on the Q2 base voltage; that is, on the PWM-DAC level. The MOSFET transistor Q1 is driven by the voltage drop on resistor R1 and regulates the battery charge current. The PWM period was set to 2048 for an accurate current level setting, and can easily be adjusted in the firmware.

Note that the charger proposed in this Application Note is based on a linear current regulator. The advantages of this regulator are low cost and small size. But to charge a battery with a capacity of over 1000 mAh with a charge current of 1 CA, where CA is the nominal battery capacity, the linear regulator can be non-optimal due to the large voltage drop on the MOSFET and the consequent high MOSFET temperature. In this case, a step-down regulator is preferable to a linear current regulator. The step-down regulator is explained in detail in Application Notes AN2107 and AN2258.

Diode D1 is used to prevent a reverse current that can discharge the battery when the charger is disconnected from the supply voltage. The cell-balancing circuit is represented by MOSFETs Q4 and Q5, and by balancing resistors R11 and R14. The MOSFETs are directly controlled from the PSoC device port (high level - close, low level - open). The resistors R8-R10 and the bipolar transistor Q3 act as a level translator and allow opening of the MOSFET Q4 by means of a logic signal from the PSoC.

The resistive network (R6, R7, R12, R13, R15, R16, and R18-R22) and the reference voltage V_{bias} from the divider on R29 and D8, allow transformation of the battery current, voltage, and temperature into signals suitable for the PSoC device. The 100-mΩ resistor R23 is a current-sense resistor that is in the battery pack current path.

The two-cell charger user interface uses two LEDs to display internal status. In this application configuration, the green LED indicates the charge phase, and the yellow LED indicates the discharge phase. The **Error** state is indicated when both LEDs are on and the idle status is indicated when both LEDs are off.

To provide a processor power supply from a high voltage level, the linear current regulator U2 is used. Alternatively, a switching regulator can be used, as explained in AN2258. Or, the regulated step-down converter from an internal SMP can be used, as explained in AN2180, “Using the PSoC Switch Mode Pump in a Step-Down Converter.” An external voltage supply is applied to the connector J4. The SW1 switch allows the device to be disconnected from the external power supply. Two diodes in the D6 package allow the processor to operate during the charge phase from the external power supply and during the discharge phase from the battery pack power supply. The external load is connected to the connector J3 LOAD. The diodes D4 and D5 provide an uninterrupted power supply (UPS) to the LOAD connector, much as D6 provides power to the processor. The switch-on transistors Q6 and Q7 allow the power supply to be disconnected from the LOAD connector and protect the battery from overdischarge. This switch is optional and can be removed to reduce total device cost further. The ground level is connected to the external ground level POWER (during the charge phase or discharge phase) and to the battery pack ground that follows the current-sense resistor. Only in this way can the charge battery pack current and the total battery pack discharge current pass through the current-sense resistor. This ground-level position is used to supplement the battery fuel gauging functionality in the PSoC software, as shown in AN2294.

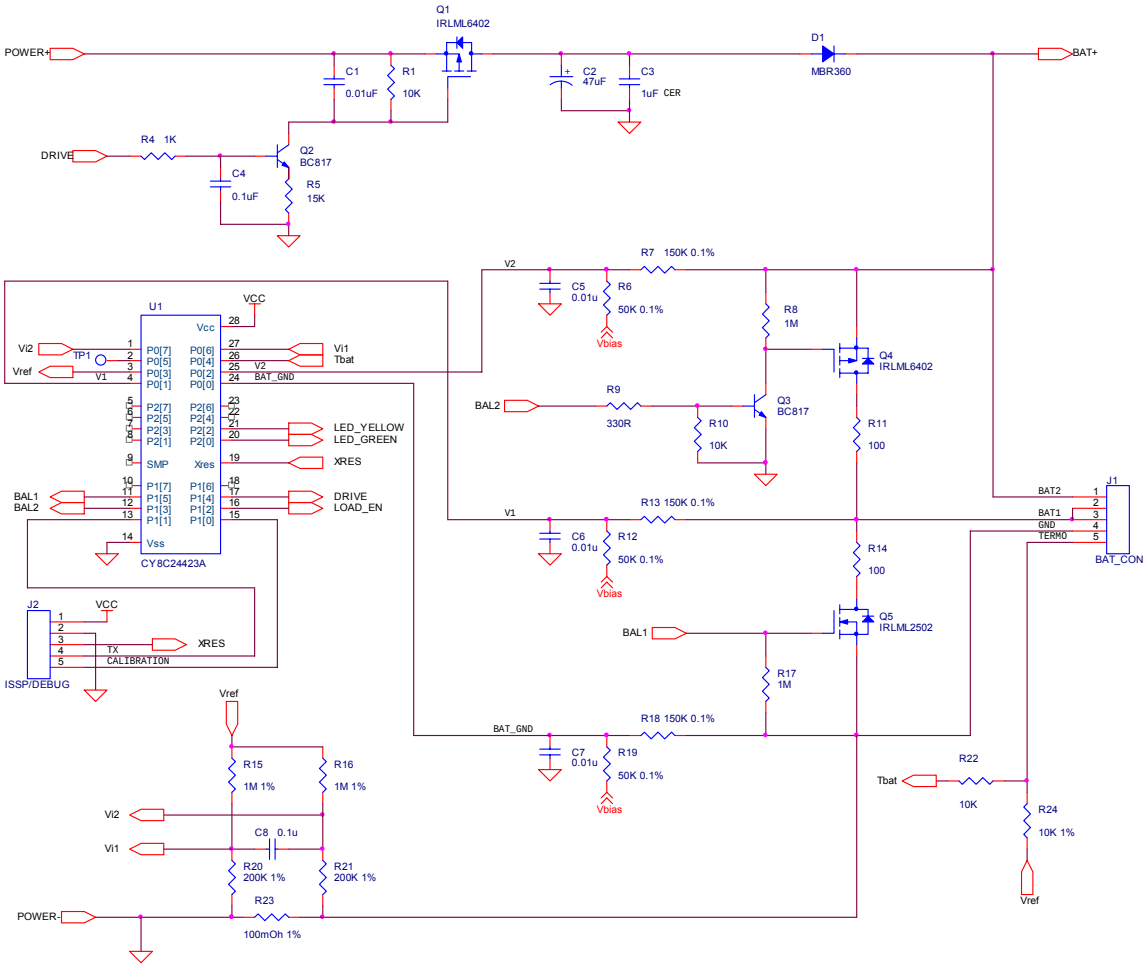


Figure 4. Two-Cell Battery Charger Schematic – CPU, Cell Balancing, and Measuring Equipment

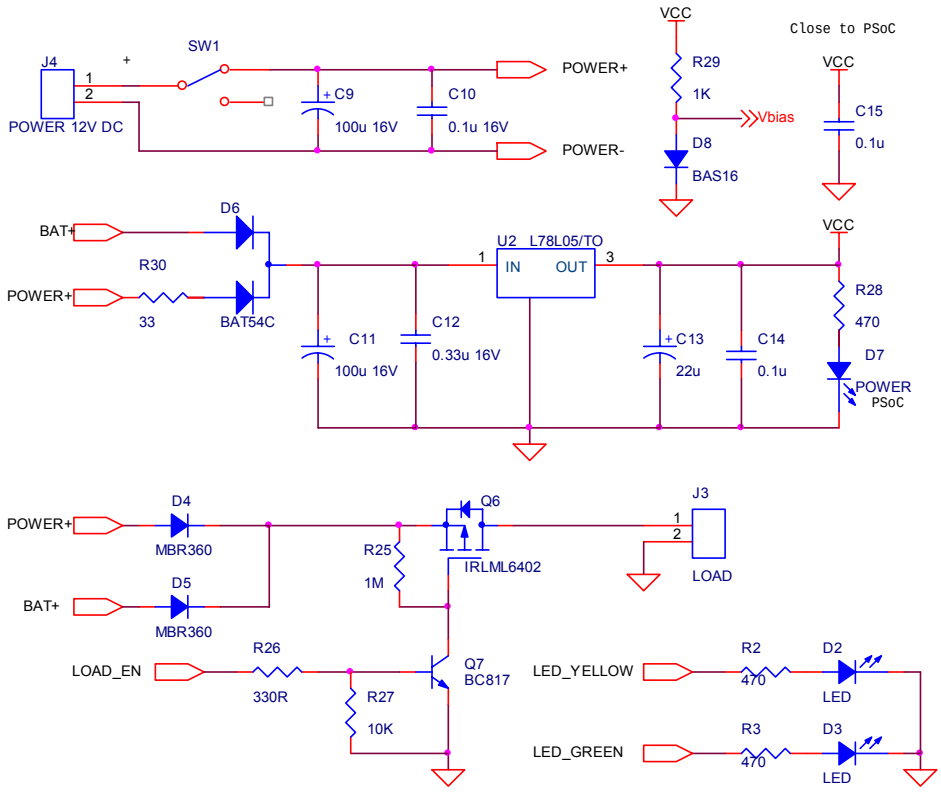


Figure 5. Two-Cell Battery Charger Schematic – Power Supply and User Interface

PSoC Device Internals

The internal structure of the PSoC device is shown in Figure 6. The PWM has been placed on DBB01 and DCB02. The module is configured in the software as an 11-bit PWM, which provides for a sufficient number of regulation steps. The TIMER User Module is based on the internal sleep timer and configured to generate interrupts every 1 second. This real clock is used to calculate other time intervals. The serial transmitter is placed into DCB03. The default exchange speed is set to 115200 baud.

The cell-balancing MOSFETS Q4, Q5 are controlled directly from the CPU (high level - close, low level - open).

The three-opamp topology of the instrumental amplifier (INA) is used in this implementation. The INA is placed in ACB00, ACB01, and ASD11. The incremental ADC is placed in the ASC10 and DBB00 blocks.

The ADC resolution is set to 12 bits, and the integration time is adjusted to be precisely equal to the integer number of the PWM signal. All of the switched capacitor user modules use the same column frequency in order to eliminate aliasing problems. In this project, the analog ground bias was set to bandgap or 1.3V (RefMux is BandGap ± BandGap).

Note that if users require more program memory and analog pins, or require USB support, in their user-defined projects, they can import this charger to the CY8C24794 or the CY8C27x43 PSoC device family. The CY8C24794 device includes a full-featured, full-speed (12 Mbps) USB port and can have up to seven I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and six analog blocks. For additional information, see “Products: PSoC Mixed-Signal Controllers: PSoC Mixed-Signal Array: CY8C24794” on www.cypress.com.

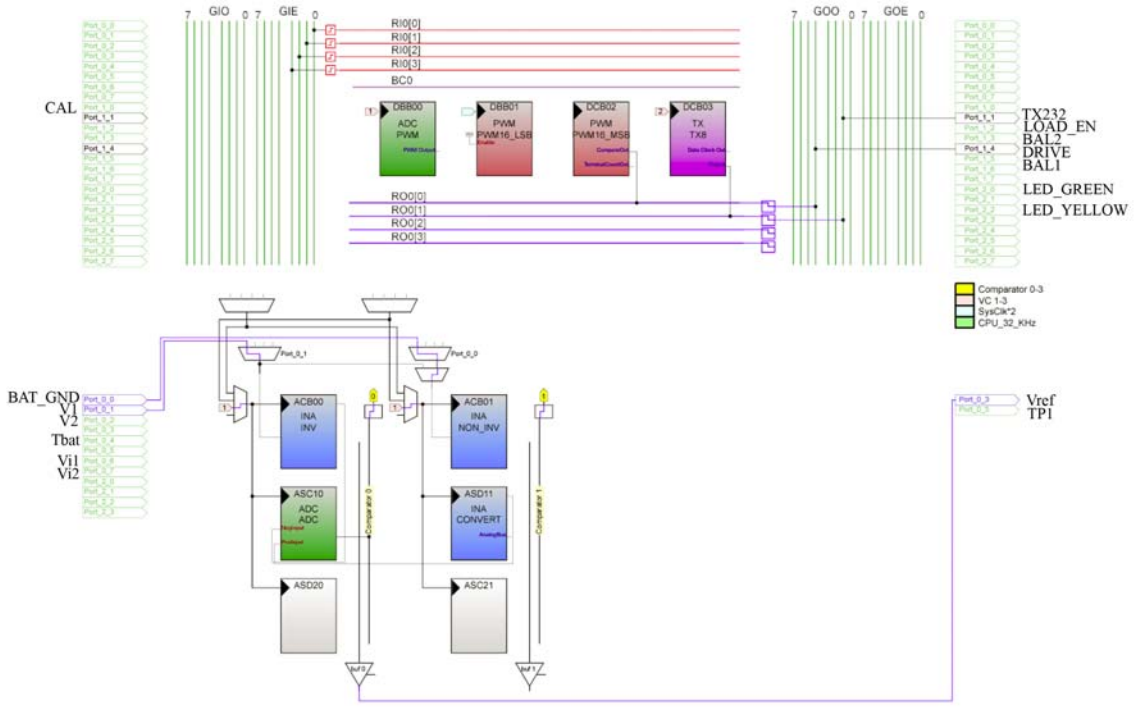


Figure 6. PSoC Internal User Module Configuration

Battery Measurement

To provide a correct implementation of the charge and cell-balancing algorithms, the charge current, battery voltage and temperature must be measured accurately.

These three parameters are measured as the voltage drops on corresponding resistors by using the instrumental amplifier INA. The measurement is implemented as a two-stage procedure to eliminate any voltage offset from the INA and ADC inputs. The INA inputs are shorted together in the first stage. This state is used to measure INA and ADC offset voltage. Then the real signal is measured. At this point the difference between the ADC codes corresponding to the first and second stages is directly proportional to the battery measurement parameter without the influence of the INA and ADC offset voltage.

To transform the battery current (voltage drop on the current-sense resistor) and battery voltage into levels suitable for PSoC signals, precise resistive dividers are used. To limit the current flow from the battery to the powered-down battery charger, divider resistors of large nominal resistance are employed.

To provide higher current measurement accuracy, a current-sense resistor was put in the pack current path close to the negative battery voltage. In this case, the voltage drop on the resistive divider (R15, R16, R20, and R21) is independent of the battery pack voltage level. This is not true if a current-sense resistor is placed close to the positive voltage. At the beginning of the charging process, the voltage bias on the current-sense resistor is measured and during subsequent processes it is subtracted from the measured values. In this way, the difference between resistor values in the resistive divider is partly compensated. The following equation represents the current measurement scheme:

$$\Delta n = n_{\max}\frac{V_{ADC}}{V_{ref}} = n_{\max}\frac{G_{ina}\beta_I I_{bat} R_{sense}}{V_{ref}} \quad \textbf{(16)}$$

The value Δn is the ADC code without the influence of the INA and ADC offset voltage and without the voltage bias on the current-sense resistor ($\Delta n = n_{meas} - n_{offset} - n_{bias}$). The value $n_{\max}$ is the maximum ADC code, which is equal to 2048 for the 12-bit incremental ADC in bipolar mode.

The value I_{bat} is the battery current, G_{ina} is INA gain (4), V_{ref} is the bandgap reference voltage (1.3V), and β_I is the resistive divider coefficient (0,833333):

$$\beta_I = \frac{1}{1+\frac{R_{20}}{R_{15}}} \quad \textbf{(17)}$$

The voltage measurement also is performed by the INA on the corresponding resistor. The resistive dividers (R7, R6), (R13, R12), and (R18, R19) transform cell voltage into signals suitable for the PSoC device. It is very important to use the high-precision resistors in the resistive divider to obtain a high-value common mode signal rejection. The recommended R6, R7, R12, R13, R18, and R19 tolerances are 0.1 percent. The following equation depicts the voltage measurement scheme.

$$\Delta n = n_{\max}\frac{V_{ADC}}{V_{ref}} = n_{\max}\frac{G_{ina}\beta_V V_{bat}}{V_{ref}} \quad \textbf{(18)}$$

The value Δn is the ADC code without influence of the INA and the ADC offset voltage $(\Delta n = n_{meas} - n_{offset})$. The value $n_{\max}$ is the maximum ADC code and is equal to 2048 for 12-bit incremental ADC in bipolar mode. The value V_{bat} is the battery voltage, G_{ina} is INA gain (1), V_{ref} is the bandgap reference voltage (1.3V), and β_V is the resistive divider coefficient (0.25):

$$\beta_V = \frac{1}{1+\frac{R_7}{R_6}} \quad \textbf{(19)}$$

To provide higher voltage measurement accuracy in decision-making charging voltages, the following calibration technique is used. All voltage thresholds are stored as calibrated ADC codes. During operation, the ADC code of the battery voltage is compared with these calibrated values. For this purpose we use an external precision 4.2V voltage source and calibration procedure after assembly. All voltage thresholds are tuned from this precision voltage:

$$n_{new} = n_{old} \times \frac{n_{4.2V\_new}}{n_{4.2V\_old}} \quad \textbf{(20)}$$

The value n_{new} is the new voltage threshold ADC code. The value n_{old} is the old voltage threshold ADC code that is calculated by using Equation (16). The value $n_{4.2V\_new}$ is the input ADC code during the calibration procedure. The value $n_{4.2V\_old}$ is the old voltage threshold ADC code for 4.2V, which is calculated by using Equation (16). In this way, the calibration is performed for all decision-making charging voltages simultaneously. All devices must be calibrated during the manufacturing process by using external reference.

For temperature measurement, a reference voltage resistive divider is employed based on a thermistor and a precision resistor (R6). Thermistor resistance is calculated according to the voltage drop on the precision resistor and the value of the reference voltage. To provide the necessary temperature measurement accuracy, the RefHI reference voltage is first set, and then AGND. After this, the second value of the resistor voltage drop is subtracted from the first. Bias voltages RefHi (2.6V) level in the first step and AGND (1.3V) in the next step are formed by using the continuous time user module TestMux. This technique allows compensation for both the ADC/INA offset error and the variation in the voltage drop on the current-sense resistor during the charging/discharging process. The following equations represent the temperature measurement scheme:

$$V_t^2 - V_t^1 = V_{AGND} \times \frac{R_{ref}}{R_{ref} + R_{term}} \quad \textbf{(21)}$$

$$n_t^2 - n_t^1 = n_{AGND} \times \frac{R_{term}}{R_{ref} + R_{term}} \quad \textbf{(22)}$$

The value V_t^1 is the voltage level on the temperature reference resistor during application of the V_{AGND} (1.3V) reference voltage, V_t^2 is the voltage level on the temperature reference resistor during application of V_{REFHI} (2.6V) reference voltage, R_{term} is the thermistor resistance, R_{ref} is the temperature reference resistance R24 (10K), and n_t^1 and n_t^2 are the ADC codes of V_t^1 and V_t^2, respectively. The value n_{AGND} is the ADC code of the AGND input level and is equal to 2048 for 12-bit incremental ADC in unipolar mode.

The battery charge/discharge algorithm only needs to check for temperatures that fall in allowed ranges: during charging (typical values are 0 to 45 degrees Celsius) and discharging (typical values are -20 to 60 degrees Celsius). During the charge phase we add a hysteresis for the lower and upper bounds in/out temperature. This prevents multiple triggering when the temperature is close to the preset range. If the temperature is outside the discharge range, the LOAD connector is turned off and the PSoC device goes into sleep mode. Therefore, a hysteresis for the discharge range is not needed. The temperature profile is shown in Figure 7.

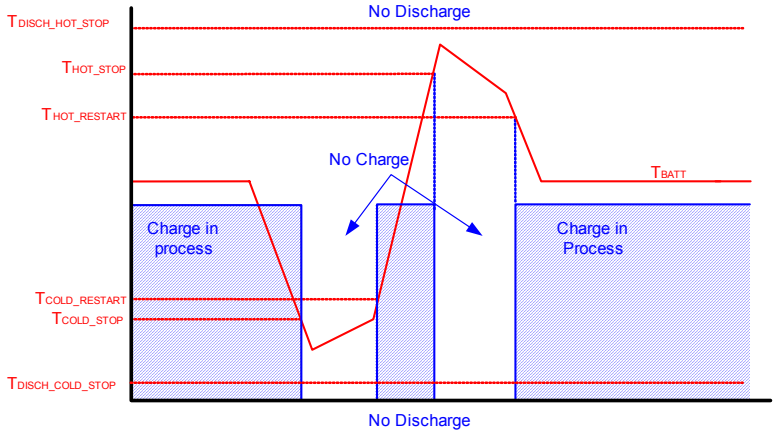


Figure 7. Temperature Profile

Two-Cell Battery Charger Firmware

The two-cell battery charger firmware is separated into several modules that serve distinct functions, such as performing measurements, regulating the battery charge process and timer functions, implementing the charge and cell-balancing algorithms, checking the charge termination conditions, storing calibration settings into the PSoC device Flash memory, and transmitting debugging data. Most of these modules are described in AN2107, AN2258, and AN2294. Therefore, in this section only the charge and cell-balancing algorithms will be described.

Two-Cell Battery Charger Algorithm

The two-cell battery charge algorithm was implemented in the charger firmware as a state machine. The following states are used:

- **Initialization** – Indicates charge process initialization.
- **Activation** – Depicts battery activation charging.
- **Rapid** – Depicts rapid battery charging.
- **Charge Complete** – Indicates that the battery pack is charged completely.
- **Wait For Temperature** – Used to depict the idle state when the battery pack temperature is outside the allowed temperature range.
- **Error** – Indicates that during the charge process an error has occurred. There are three error types: over-voltage, over-current and stage time-out exceptions.

- **Discharge** – Indicates that the battery pack discharge process and the storage device state are without external power supply.
- **Full Discharge** – Indicates that the battery pack is discharged completely and is not suitable for further use.

The two-cell battery charger state diagram is shown in Figure 8.

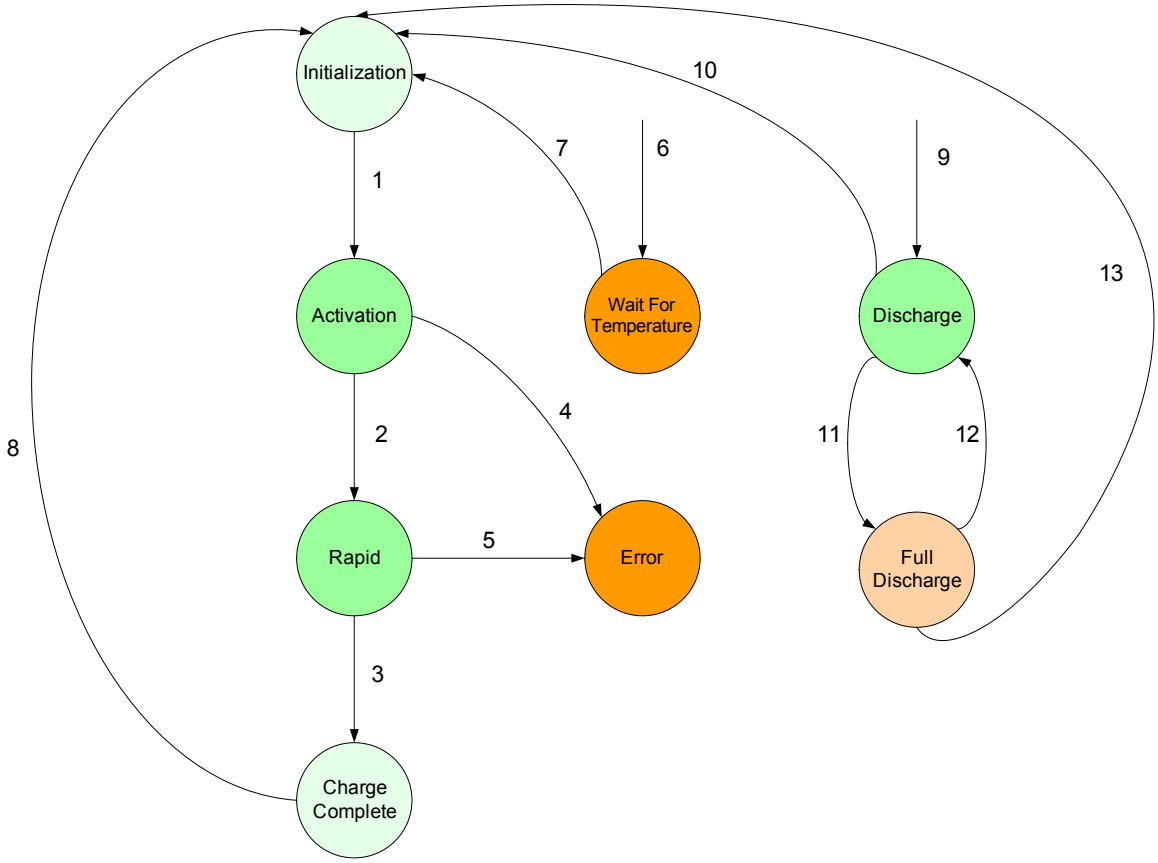


Figure 8. Two-Cell Battery Charger State Diagram

Initially the charger is in the **Initialization** state. After some device preparation, the charger goes to the **Activation** state (1). When the battery voltage reaches the rapid start voltage, the charger leaves the **Activation** state and switches to the **Rapid** state (2). If the charge current drops below a predefined charge-terminate level, the charger goes to the **Charge Complete** (3) state. The charger remains in the **Charge Complete** state and the charging process can be restarted if the voltage drops below some predefined level (8). The charging process can be terminated with an error if a total charge time-out or an operation charge time-out occurs, or if the battery voltage or charge current is higher than the charge termination voltage/current levels (4), (5).

The charger from all states jumps to the **Wait For Temperature** state when the battery temperature is outside the allowed temperature range. For the **Activation** and **Rapid** states, the allowed temperature range is the charge range. For other states, the allowed temperature range is the discharge range (6). In the case of the charge range, when temperatures fall into the defined range with some hysteresis value, the charger goes to the **Initialization** state (7).

Regardless of the state of the charger, it jumps to the **Discharge** state when the external power supply is switched off (9). If the external power supply is switched on, the charger goes to the **Initialization** state (10, 13). When the battery pack discharges completely (11), the charger switches to the **Full Discharge** state.

If the system load resistance decreases and the battery pack voltage level re-establishes to the predefined voltage level, then the charger returns to the **Discharge** state (12).

A two-cell battery charger firmware flowchart that corresponds to the state diagram is shown in Figure 9 and Figure 10. The invocation points of the cell-balancing procedures are also shown. The charge profile example is presented in Appendix A, Figure 13.

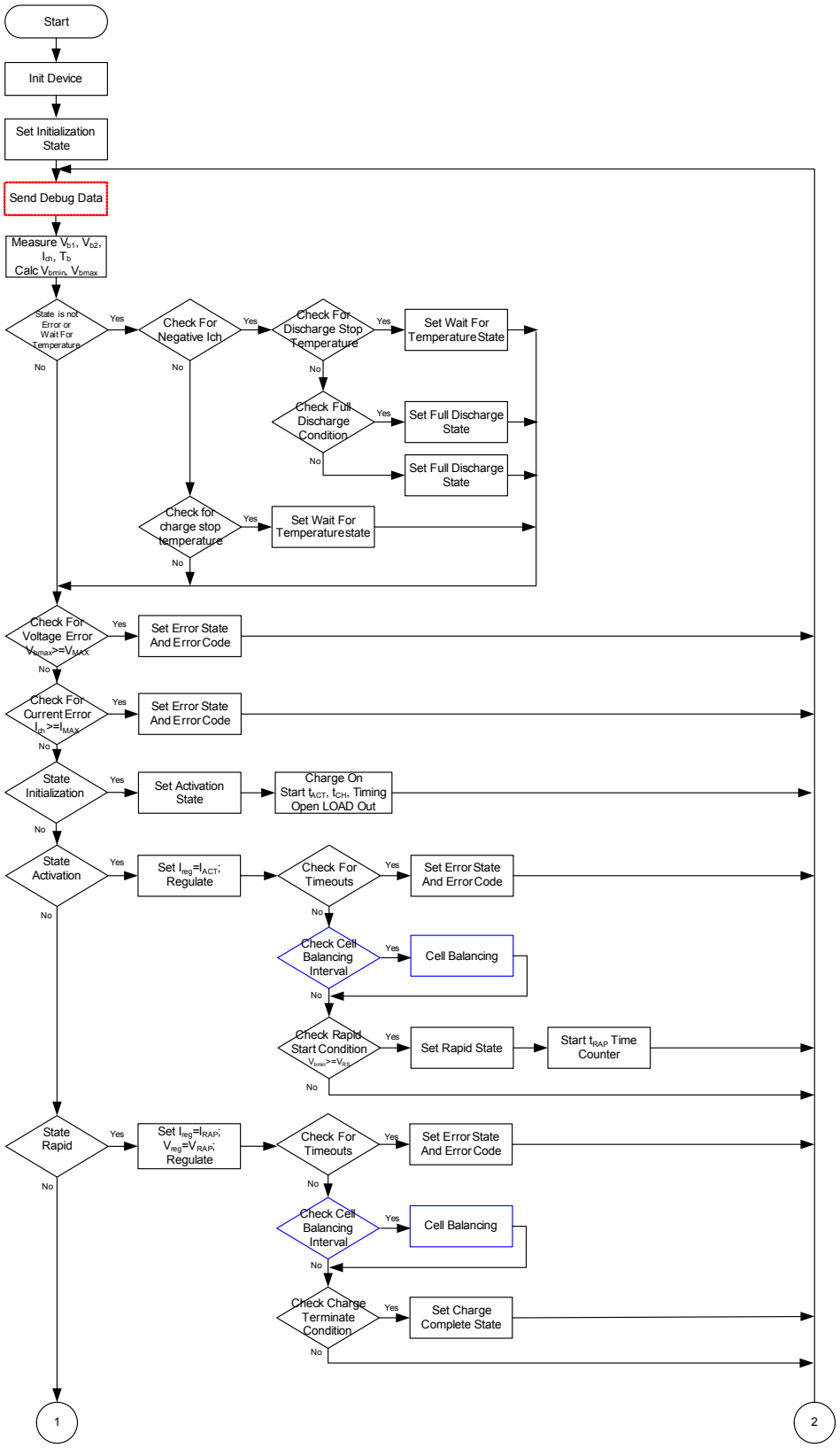


Figure 9. Two-Cell Battery Charger Firmware Flowchart Part 1

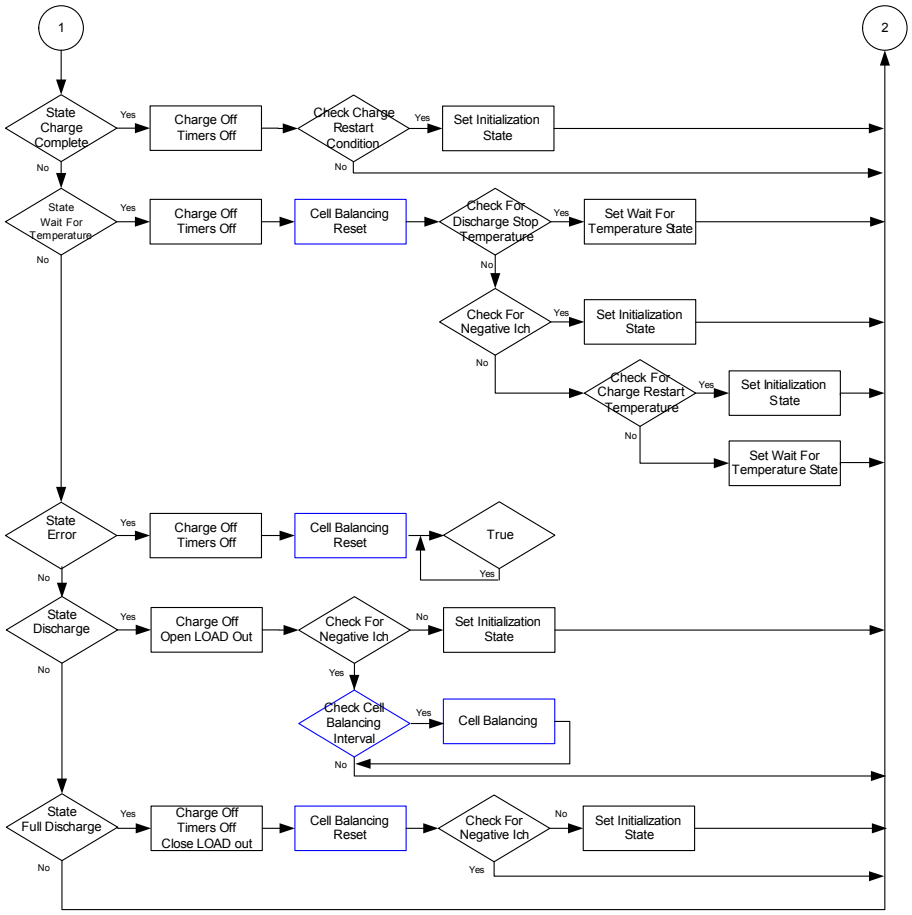


Figure 10. Two-Cell Battery Charger Firmware Flowchart Part 2

Cell-Balancing Algorithm

At first sight, the cell-balancing algorithm for a two-cell battery charger appears very simple. The criterion for the cell imbalance is the voltage difference between the cells. The cell with a greater voltage should be shunted. But this algorithm can lead to still more imbalance. During cell balancing only intrinsic cell voltage should be taken into account. The voltage portion contributed by the impedance of the cell leads to errors in cell balancing. In the deep discharge battery, where the internal resistance of the battery can be as high as several ohms, the I x R drop dominates the overall cell voltage. For this reason, cell balancing is not recommended when the battery pack is close to deep discharge. Cell balancing during this time can lead to greater imbalance than before cell balancing was conducted.

During the 1-C rate charge, the battery has reached approximately 50 percent of the charged state when its voltage has risen above 3.9 volts. If the charging current is less than 1C, this threshold can be reduced. At this charge state, the internal resistance drops below 0.2Ω and the distortion level is within acceptable limits. Therefore, some cell-balancing methods can be executed if the cell voltage is above the predefined VMID value (voltage of middle charged state) and the minimum cell-balance parameter consists of the voltage measure error value plus the internal impedance error value.

A better practice, which yields more accurate cell voltage measurements, is to perform the cell sampling operation after suspending or interrupting the charge current - the *pulse charge technique*. With this technique, the charge operation is temporarily interrupted to permit voltage measurement of the cells in the pack. Such suspension of charging eliminates the contribution of cell impedance to cell voltage measurements and yields more accurate indication of cell mismatches.

When the pulse charge technique is used, the minimum cell-balance parameter equals the voltage measure error value and, therefore, cell balancing can be executed at any time during the full charge cycle. In the present implementation, the pulse charge technique is used. As shown in Figure 11, the charge operation is interrupted before voltage measurement.

At the end of the charge process, the shunted current switching on the cells (to achieve cell balance) can result in a premature system shutdown. Therefore, during constant voltage mode of the rapid-charge stage, if the charge current stays below the minimum cell-balance parameter, the balancing process stops. Note in Figure 11 the “Check Out of the Minimum Cell Balancing Current” condition.

Cell balancing during the discharge phase also is executed if the maximum cell voltage is above the predefined VMID value. See in Figure 11 the “Check Out of the VMID Voltage” condition. The discharge VMID value can differ from the charge VMID value (described earlier in this section), and its value is dependent on the discharge rate. The minimum cell-balance parameter consists of the voltage measure error value plus the internal impedance error value.

The cell-balancing algorithm that is implemented here does not significantly lengthen the charge time. The charger monitors all of the cell voltages. Cell balancing is performed during both phases and it is realized in one common module. The cell-balancing algorithm is represented in Figure 11. The cell-balancing profile examples are shown in Appendix A, Figure 14 and Figure 15.

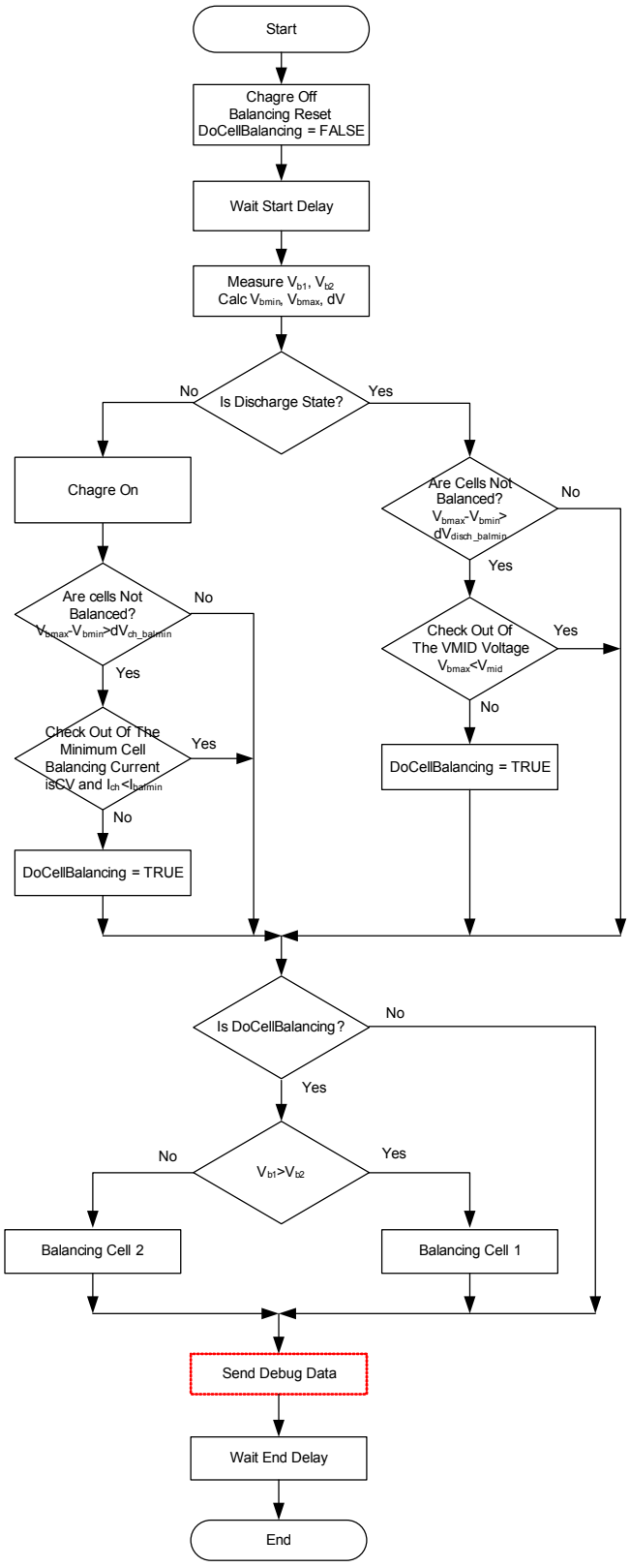


Figure 11. Cell-Balancing Algorithm

Two-Cell Battery Charger Parameters

All two-cell battery charger parameters are located in the header file *globdefs.h* in the project folder. *globdefs.h* contains the following parameters:

Table 2. Two-Cell Battery Charger Parameters

Parameter	Unit	Description
Charging Parameters		
Vrs	V	Rapid-Charge Stage Start Condition
Vrap	V	Full Charge Voltage (Constant Charge Voltage)
Vcrst	V	Recharge Voltage
Vbmax	V	Emergency Shutdown Voltage
Vfull_disch	V	Full Discharge Voltage
Iact	A	Activation Stage Charge Current
Irap	A	Rapid-Charge Stage Current
Ichmax	A	Emergency Shutdown Current
Irtn	A	Charge Termination Current
Timing Requirements		
T_{ACT}	second	Time Limit for Battery Activation Period
T_{RAPID}	second	Time Limit for Final Stage of Constant Charge Mode Voltage
T_{CHARGE}	second	Time Limit for Total Charge Period
T_{TERM}	second	Minimum Time for Charge Complete (when Ich ≤ Irtn)
Thermistor Measurement Requirements		
$R_{TERM\_CH\_COLD\_STOP}$	Ohms	Thermistor Resistance for Cold Stop Battery Charge
$R_{TERM\_CH\_COLD\_RESTART}$	Ohms	Thermistor Resistance for Cold Restart Battery Charge
$R_{TERM\_CH\_HOT\_STOP}$	Ohms	Thermistor Resistance for Hot Stop Battery Charge
$R_{TERM\_CH\_HOT\_RESTART}$	Ohms	Thermistor Resistance for Hot Restart Battery Charge
$R_{TERM\_DISCH\_COLD\_STOP}$	Ohms	Thermistor Resistance for Cold Stop Battery Discharge
$R_{TERM\_DISCH\_HOT\_STOP}$	Ohms	Thermistor Resistance for Hot Stop Battery Discharge
Schematic Parameters		
CURRENT_SENSE_R	Ohms	Current-Sense Resistor
TEMPERATURE_R_REF	Ohms	Thermistor Reference Resistor

Cell-Balancing Parameters

All cell-balancing parameters are located in the header file *globdefs.h* in the project folder. *globdefs.h* contains the following parameters:

Table 3. Cell-Balancing Parameters

Parameter	Unit	Description
Vmeas_err	V	Resistor Matrix Error for Measuring Cell Voltage
Vin_err	V	Internal Cell Impedance Error
Vch_bal_min	V	Minimum Cell Balance for Charge Phase
Vdisch_bal_min	V	Minimum Cell Balance for Discharge Phase
Vdisch_mid	V	Voltage of 50 Percent Charging Cell During Discharge Phase
Ibal_min	A	Minimum Charge Current Value When the Cell Balancing is Allowed (on CV Phase)
T_BAL_INTERVAL	second	Cell-Balancing Interval

Conclusion

A two-cell battery charger with cell-balancing technology has been described. Recommendations for cell-balancing circuit components are given. An effective cell-balancing algorithm for both charge and discharge phases is developed. The algorithm avoids problems that can arise in a battery pack with two cells in series. By altering several configuration parameters, the cell-balancing algorithm can easily be adapted for various applications and selected batteries. A method to perform cell balancing is proposed that uses charge/discharge phases that do not significantly lengthen charge times. This two-cell battery charger supports the pulse charge technique.

The two-cell battery charger algorithm and cell-balancing algorithm are implemented in the PSoC device firmware. The dedicated PC-based software is developed to perform real-time charging and cell-balancing process visualization and analysis via a graphical user interface. The proposed device can be used as a complete battery pack management system for laptop computers, and medical, industrial, and other applications. References have been made to AN2294 if users are interested in easily adding fuel gauge functionality to this project. The unique architecture of the PSoC device and the in-circuit and self-programming capabilities make these operations simple. The chosen CY8C24x23A PSoC device family further reduces total system cost.

The Photograph

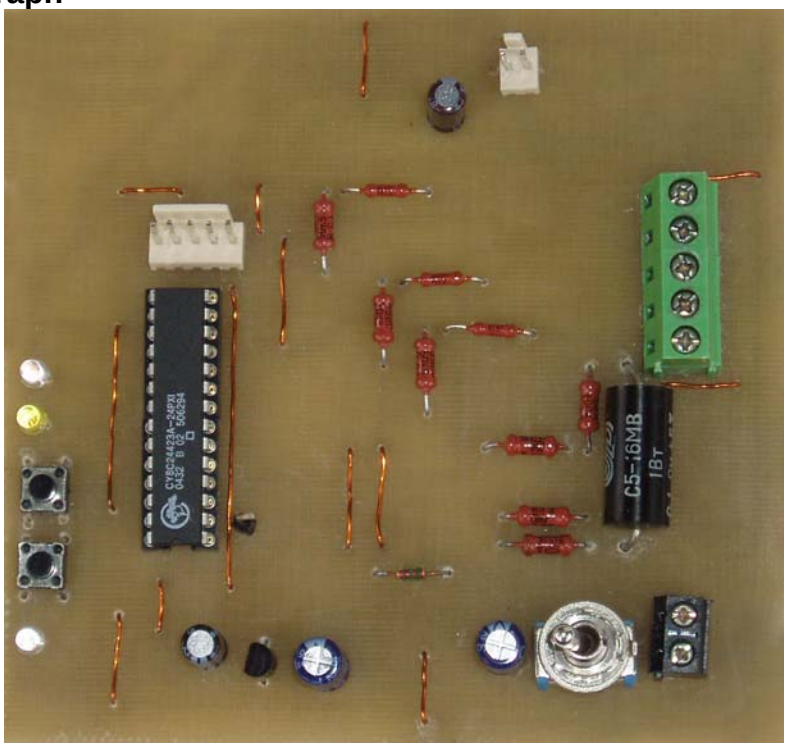


Figure 12. Two-Cell Battery Charger Photograph, Actual Size

Appendix A. Charge/Discharge and Cell-Balancing Profile Examples

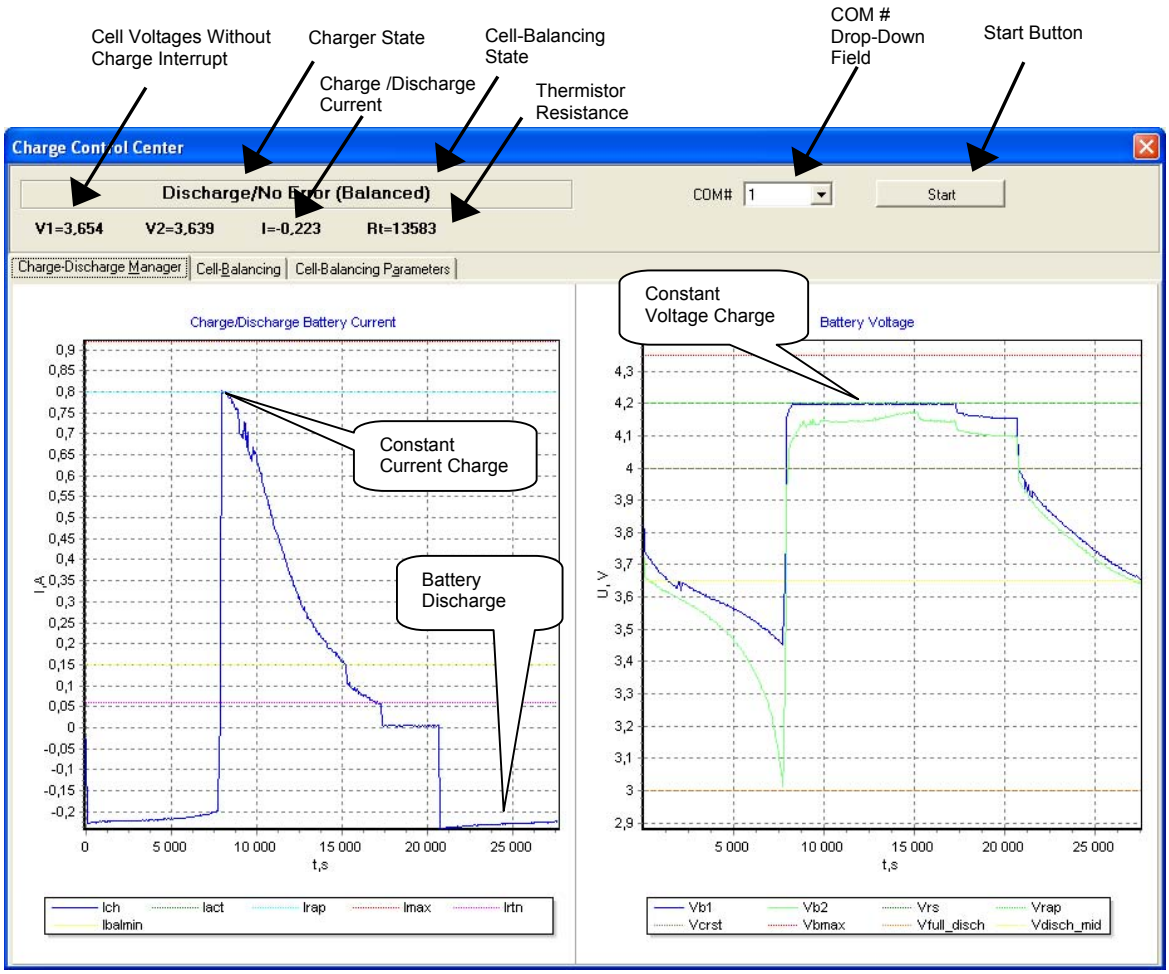


Figure 13. Charge/Discharge Manager Profile

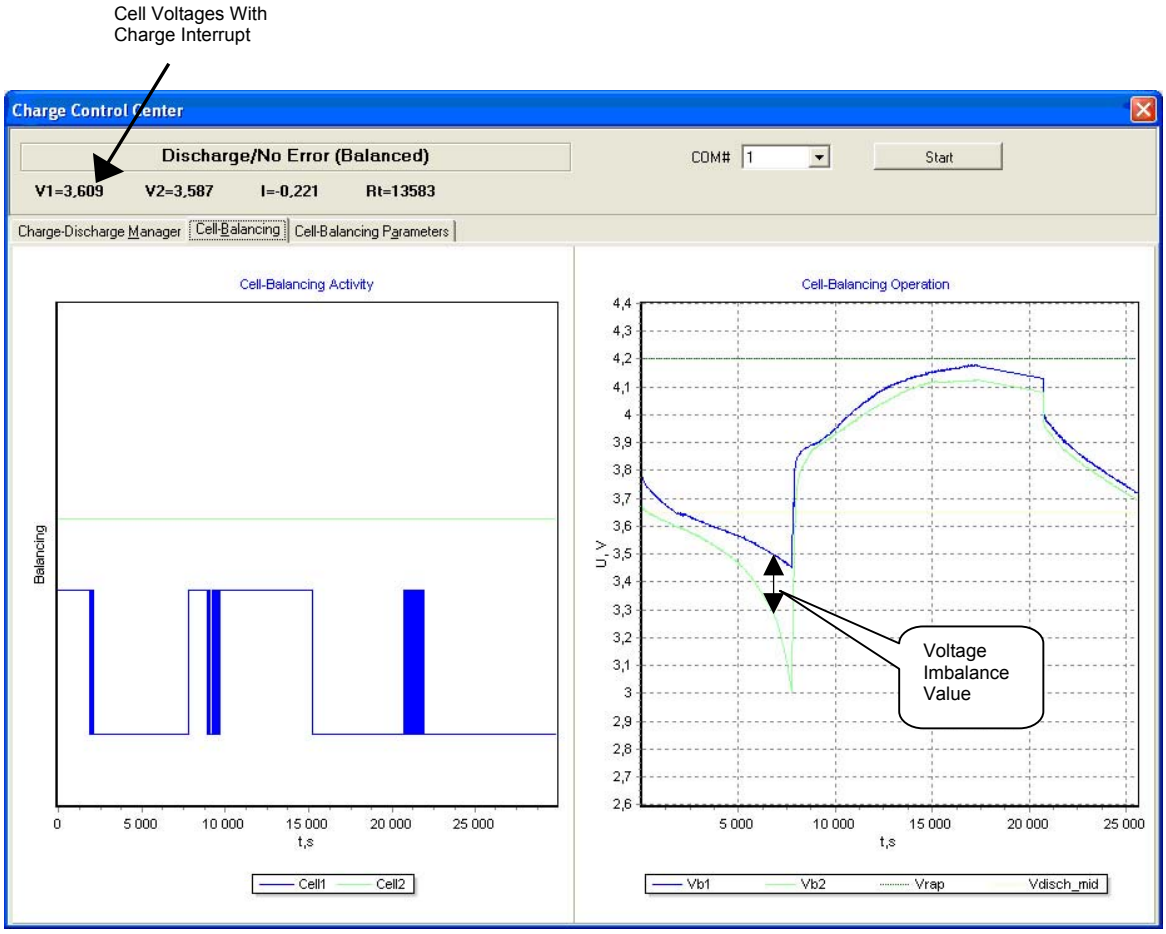


Figure 14. Cell-Balancing Activity Profile

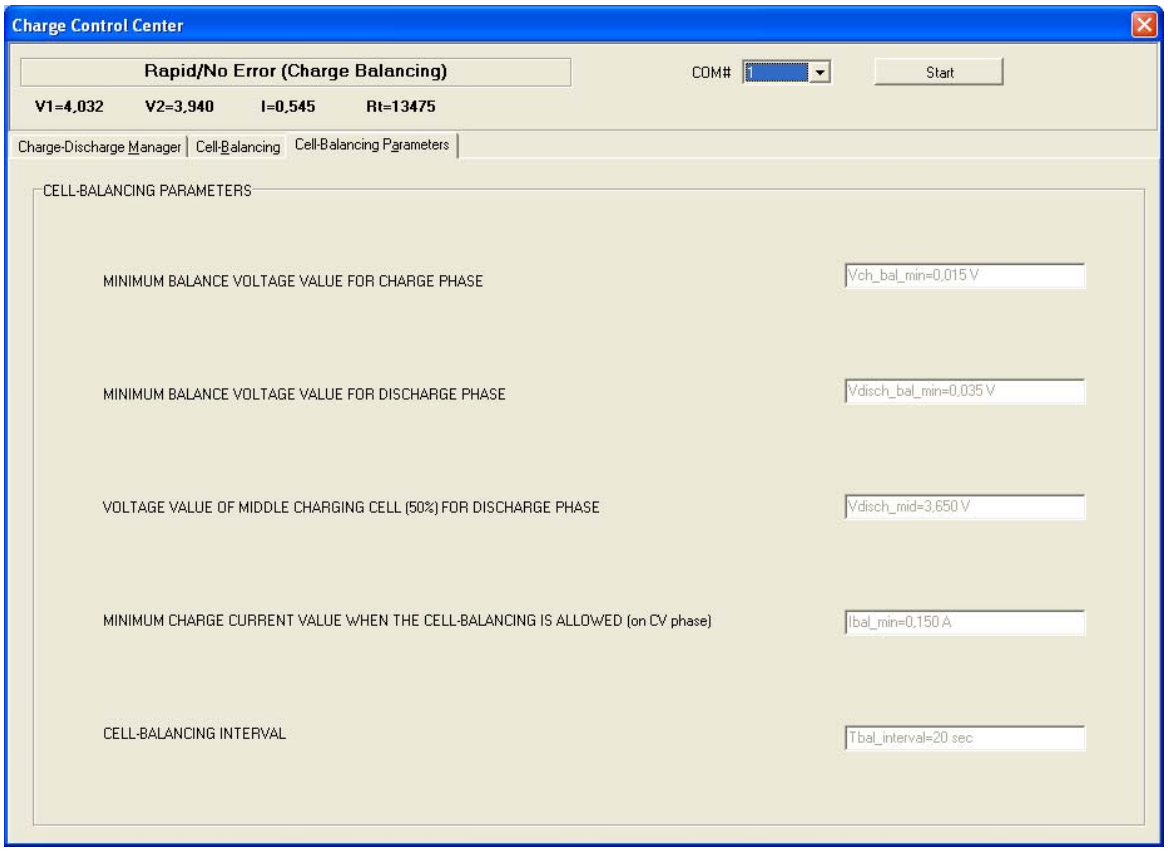


Figure 15. Cell-Balancing Parameter Profile Screen

About the Author

Name: Oleksandr Karpin
Title: Post-Graduate Student
Background: Oleksandr received a master's degree in computer engineering in 2001 from Lviv Polytechnic National University (Ukraine), and continues his studies there as a post-graduate student. His interests include embedded systems design and new technologies.
Contact: karpinoo@ukr.net

Cypress Semiconductor
2700 162nd Street SW, Building D
Lynnwood, WA 98087
Phone: 800.669.0557
Fax: 425.787.4641

http://www.cypress.com/