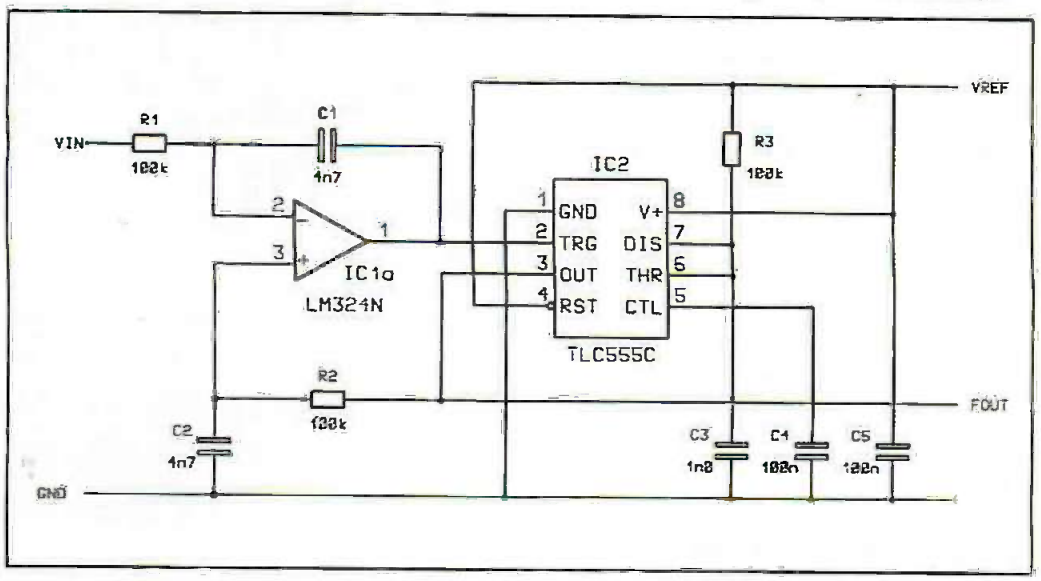
Voltage to Frequency CONVERTER

THIS CIRCUIT PRODUCES A STREAM OF CONSTANT WIDTH PULSES AT A RATE DIRECTLY PROPORTIONAL TO THE (INPUT VOLTAGE)/(REFERENCE VOLTAGE).

It differs from other similar circuits in operating from a single supply voltage yet having the input directly referenced to the negative (ground), and only one op-amp and a timer chip are required as active components. The basic operation is also similar to other VFCs - the output pulse rate is adjusted so that the averaged voltage of the pulse stream is equal to the input voltage. Usually, if not using bipolar supply rails, the input voltage would require some kind of level shifting, needing another op-amp at least. No level shifting is needed in this version.

The timer used here is a CMOS version of the ubiquitous 555 timer. The output of this chip switches from rail-to-rail, being CMOS, rather than to 1.5V below the positive supply as with the bipolar version. Since in this circuit the high level of the 555 output is also the VFC reference voltage, this is a distinct advantage. When the trigger pin is taken below 1/3 of the supply voltage, the output immediately goes high and the timing operation starts. The output pin is kept high after the normal time if the trigger pin is still low, which is a desirable feature in this circuit as it ensures that the circuit will always start up. It is possible to use other one-shot timers, as long as they have a negative going trigger and a positive output pulse; for instance, in a mainly digital circuit a spare half of a 74HC123 dual timer could be used. The one-shot using a couple of NAND gates might be another. To ensure start-up with a timer like the '123 requires a few components more, to force the output high as long as the trigger is low.

The op-amp must accept and operate with inputs near the negative supply level, and the output must be capable of going down to at least the trigger level for the timer. The LM324 is one such device. It can also work from 5V, which is handy. The schematic doesn't show the supply for the op-amp, which could well be the same as for the timer, but doesn't have to be. The timer works up to an absolute maximum of 18V, but 15V is the sensible limit. Both the 324 and the 555 will work at 5V, so it would be easy to use this in an otherwise digital circuit, and if there is a microcontroller available, two port pins could then be co-opted into taking on the timer function.



Operation:

The input voltage VIN must always have a DC path to ground. Assume VIN is lower than that on the filter capacitor C2: the op-amp output will rise steadily as the difference is integrated by C1. The timer trigger input will rise above the trigger point (VREF/3), releasing the timer and allowing its output to switch to GND once the delay time has elapsed (which it may already have done). The C2 voltage will then decay towards GND, eventually falling below VIN. At this point, the direction of the op-amp integrator output will change direction from rising to falling.

After some time, the integrator output will become lower than the VREF/3, and the 555 output will switch to its high level, which is VREF. This will cause the voltage on C2 to rise. When it becomes higher than the input voltage the integrator again changes direction, with the op-amp output falling once more, and the cycle repeats.

Why is the output rate proportional to the input voltage? The simple no-maths explanation is that with a fixed pulse width the average voltage of the stream is proportional to its frequency. The timer is connected as an oscillator, since there is positive feedback from the output to the trigger via the filter capacitor and the op-amp, which puts that timer-output derived sawtooth on the trigger input. If the pulse waveform average is higher than the input voltage, the integrator will tend to drift up away from the timer trigger level, and the timer will get triggered later, so reducing the rate. Conversely, if the rate is too low, the integrator will tend to fall below the trigger level, the timer will be triggered earlier, and the rate will rise. This is where the 555 trigger behaviour comes in handy – if there is an input voltage but no pulse stream, the integrator will eventually fall below the trigger level and the 555 output will be forced high, so the C2 voltage will rise to the VIN level. It will always start.

Value Selection

The waveform on the capacitor C2 is the normal charge/discharge curve for a C-R with a rectangular pulse train applied. It turns up at the op-amp output as a linear sawtooth,

though, as the action of the integrator adds a compensating curve if the two time constants associated with the op-amp are the same. That is, if C1*R1=C2*R2. The amplitude of the waveform at the op-amp output is the same as on capacitor C2, but it is shifted so that the lowest level reached is set at the trigger voltage for the 555, VREF/3. This shift may be up or down, depending on the input voltage level.

For linear VFC operation, the op-amp output must not reach its upper limit and saturate. This can be prevented by ensuring that the product of C2*R2 (and therefore also C1*R1) is larger than the value of the 555 output pulse width, limiting the maximum amplitude of the waveform on C2. There is a trade-off, as the higher the op-amp time-constants the smaller is the amplitude of the op-amp output signal, which has consequences in increased noise-induced pulse jitter, and the longer is the settling time after a change in VIN. Operating both chips from 5V, a ratio of around 4 will be safe, less than 3.3 may to lead to op-amp saturation. The higher the operating voltage, the closer the time-constants can become.

The frequency range of the VFC depends on the timer output pulse width, which is 1.1*C3*R3 seconds; this is the minimum period for the output cycle. If reached, the output would be permanently high, as this would actually be a 100 duty cycle, but the notional frequency would be 1/(1.1*C3*R3) = 0.909/(C3*R3)Hz. With the input voltage at VREF/2 there will be a 50 duty cycle output, the period will be 2.2*C3*R3, and so the frequency will be 1/(2.2*C3*R3) = 0.454/(C3*R3). For the values used here, mid point frequency will be 4545Hz. Minimum frequency (for a grounded input) is zero. The scale is linear, with the reachable upper limit depending on the maximum working common-mode voltage of the op-amp; that is 1.5V below the supply for the LM324. If this is lower than VREF, then this sets the maximum effective range of VIN. By adding another resistor from the inverting input to ground, the input voltage scaled as required, though of course it does not increase the reachable maximum output frequency. For instance, changing R1 to 200k and adding a 200k to ground will double the range of VIN without changing the time constants. It also ensures the requirement is also satisfied that a DC path is maintained for the inverting op-amp input to ground. The TLC555 is specified to work well beyond 1MHz, which will be out of range for the 324 op-amp, but up to 100kHz should be fine.