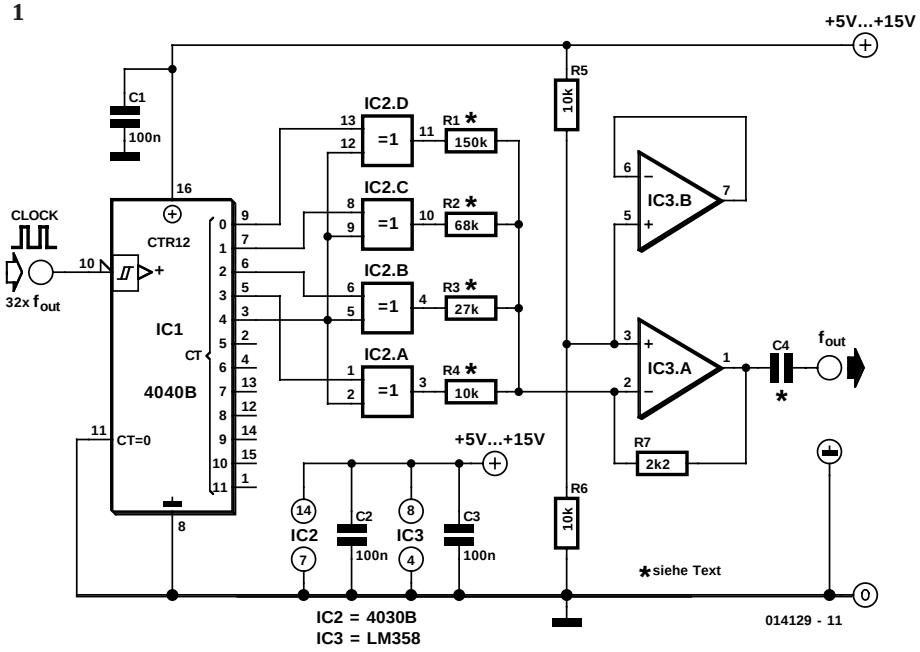
Wideband Waveform Generator 020

This circuit is designed to provide a wideband digital sine wave signal source. Its main feature is that because it synthesises the signal in 32 steps, no low-pass filter is required to suppress the odd harmonics.

A well-known method for synthesising a sine wave under control of an input frequency is to apply a low-pass filter to a square wave of the same frequency. Along with the fundamental, this includes odd harmonics. After filtering out these parts of the signal we are left with a clean sine wave at the desired frequency. Unfortunately, the corner frequency of the low-pass filter limits the usable range of frequencies.

1



The solution presented here in **Figure 1** avoids low-pass filtering by using more voltage levels than just 'high' and 'low'. Here there are 16 voltage levels which follow one after the other in a series of 32 samples. Outputs Q0-Q3 of counter IC1 control the voltage steps. Q4 inverts the polarity of the output in the second half of the period. This does not completely remove the odd harmonics — the signal still has steps in it — but they are severely attenuated.

Resistors R1-R4 together provide operational amplifier IC3 with 16 voltage levels. R5 and R6 hold the non-inverting input of IC3 (pin 3) at half the supply voltage. The operational amplifier therefore operates as an inverting amplifier with R7 as the feedback resistor. To obtain as symmetrical a signal as possible, a potentiometer is recommended for fine adjustment of this path.

This fine adjustment was be made before measuring the distortion: a THD + N figure of less than 10 % (over a bandwidth of 22 kHz) and less than 13 % (over a bandwidth of 500 kHz) was obtained with an input frequency of 32 kHz and an output frequency, therefore, of 1 kHz. The measured output signal is shown in **Figure 2**.

The shape of the output waveform (in this case a sine wave) is determined by the ratios between resistors R1 to R4. This allows plenty of scope for experiment! The clock frequency at the input to the counter should always be 32 times the desired output frequency.

The output of the operational amplifier has a DC offset of half the supply voltage. If this causes a problem in the circuit being driven, a coupling capacitor C4 must be fitted: the lower the operating frequency and the lower the load impedance, the greater the required value of capacitor.

The circuit operates from a supply of between +5 V and +15 V, and this determines the amplitude required of the input clock signal to drive counter IC1. The amplitude of the output signal can be set with resistor R7 and is independent of the output waveform. The current consumption of the waveform generator is about 3 mA.

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2