Multivibrators

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Multivibrators are used in computer hardware to go from a high level to a low level. With positive logic it would be binary 1 as high and zero as low, whereas just the opposite is true of negative logic. There are three types of multivibrators: the astable, monostable, and bistable. Although it is the bistable that is of most interest to computer hobbyists, I will touch briefly on the other two.

THE ASTABLE

The astable is made up of two stages using AC coupling and each stage being phase-inverted and positive feedback coupling. This causes continuing oscillation. When Tr1 is on Tr2 is off. This will cause the base voltage of the Tr2 to reach exponentially that of the supply voltage. The collector voltage in turn will start to drop and be coupled to the base of Tr1. Tr1 will now start to turn off and an apparent rise in collector voltage will occur. Simultaneously, the base current of Tr2 will increase, reducing its collector voltage. The switching of on and off states will be completed when Tr2 reaches saturation. When designing this type of circuit it is imperative that the base-emitter be protected with high-speed diodes, and the Vcbo has to twice that or better of the Vcc. This applies to when the collector is twice the plus Vcc in relation to the base that is reverse-based.

The astable multivibrator is useful where there is a need for successive repetitive pulses such as in PCM work.

THE MONOSTABLE

The monostable vibrator operates on both AC and DC coupling. This will allow it to rest, and then to be quasi-stable by an external pulse. When the vibrator is in the quasi-stable state, the circuit is usually turned on by the input's negative edge. If the positive half of the input happens to offset the quasi-stable state, it will cause a premature resetting of the circuit. This is usually overcome by adding a diode and a resistor to the base of Tr1. It can also be overcome by coupling a capacitor-resistor from base to emitter of Tr2. The values of R5 and R1 are approximately the same. If high speed application is involved a diode is put across R5. It is interesting to note that if pnp transistors are used rather than npn, as in the above circuits, and supply voltages and diodes are reversed, the waveforms will be just the opposite.

The monostable multivibrator is usually applicable to power supplies.

THE BISTABLE

The bistable multivibrator is the one that is of most interest to the computer hobbyist. It is used in central processing unit's register as the binary counter. It can be used in memory and is the heart of all frequency counters. The bistable multivibrator is essentially an astable type except that there are two DC couplings instead of the AC and DC. The circuit switches between two different stable states, the triggering being an external pulse. The heart of the bistable is the integrated circuit. There are exceptions, though, when an IC is not used. They are when input and output conditions are such that IC compatibility would be impossible, when there is low power dissipation, when low or high speed is necessary and also involving only a simple counter. When not using the IC scheme, we will be involved with transistor configurations.

It is the IC configuration involving the concept of logic about which we shall be most concerned. The basic rule that applies to bistables is that they must have a memory, which means when the external signal has been removed they will stay in the state of that signal. This is often referred to as a flip-flop condition.

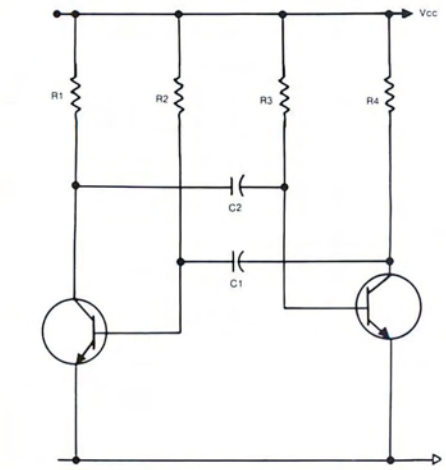
The bistable IC is classified according to its triggering level or threshold and also transient or edge triggering. The first consideration is concerned with the way the output changes when the input is at its threshold or triggering level. For example, if we were to go from a +5V input to a +15V there would obviously be a change in amplitude of the output waveform and perhaps a change in the shape of the waveform itself, which we shall discuss later. The second condition is when the clock within the IC itself changes state, often referred to as toggling.

The most often-discussed and perhaps simplest bistable or flip-flop is the R-S. It is two NOR or NAND gates that are coupled in a cross-like manner, often called latching. There are generally two inputs, the R (reset, often called C (clear), and the S (set) input. The output of the gates are called Q and $\overline{Q}$. This means that the output states are completely opposite. But when R and S are zero, then Q and $\overline{Q}$ will be one when using the NAND gate configuration. The truth table for both the NAND gate and NOR gate bistable is given in Figure 3. Figures 3 and 4 show the relationship of the R-S to the truth table. It will be noticed that the second and third lines of the table represent the reset and set input respectively. When there is a one on the set input and a zero on the reset, this will trigger output (Q) to zero, while ($\overline{Q}$) will be a one. From the table the reader will be able to discern that the direct opposite is true of line three for all conditions. The fourth line states that when there is a 1 on R of Gate 1, still using two NAND gates, and S on Gate 2 is a 1, and there is a zero on Q going to the other input of Gate 1, this ultimately has not altered the Q output from that of line three. This type of situation is truly that of a multivibrator. From the information given so far about the R-S truth table the reader will be able to make up different logic equations of his own. The complete R-S principle works on the idea of regeneration.

As I mentioned previously the subject of waveform would be discussed when working with an R-S configuration. The diagram in Figure 4 will show the type of action that is involved when a sinusoidal waveform, namely AC is applied to the input, there will be a square wave output that has a rise and fall time of approximately 10 to 15 nanoseconds. The triggering voltage of most standard gates has to be approximately one volt, which means that it is not in range of the threshold level, thus accomplishing triggering.

THE R-S-T FLIP-FLOP

The next member in the family of bistables is the R-S-T flip-flop. The T in this case denotes toggle or triggering terminal. It is this type that belongs to the edge-triggered classification. It will change condition or state up-going



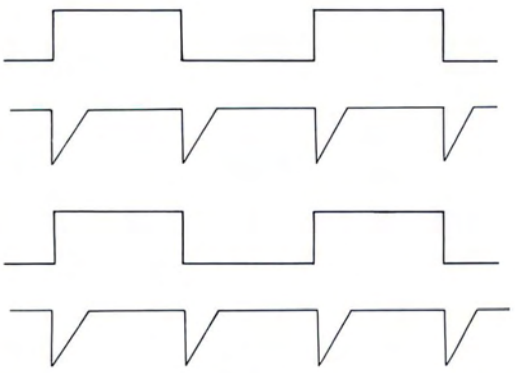
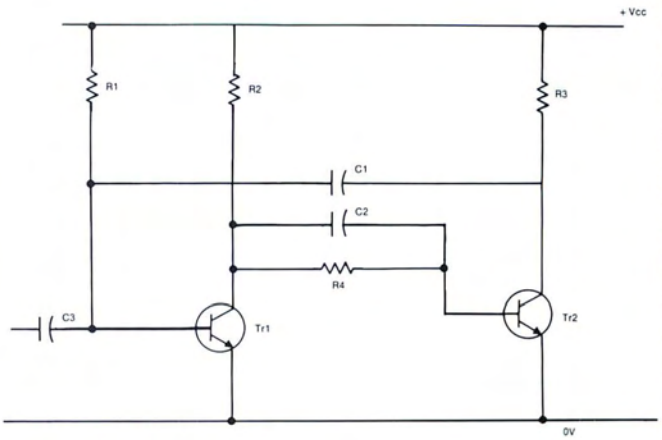


Figure 1. It is seen with the astable vibrator, as shown in the waveforms, that when Tr1 is turning off the collector voltage increases which in turn increases Tr2's base current. When Tr2 has reached saturation, then both Tr1 and Tr2 will turn off. The voltage on the base of Tr1 will then rise according to C1 and R1's time constant.



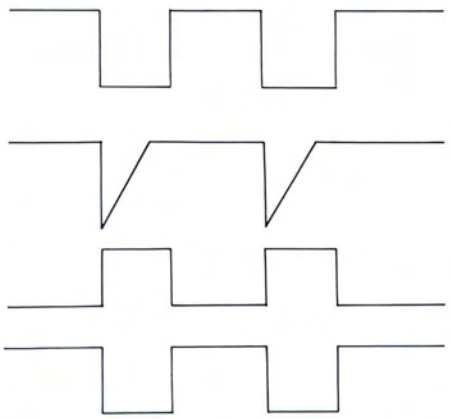
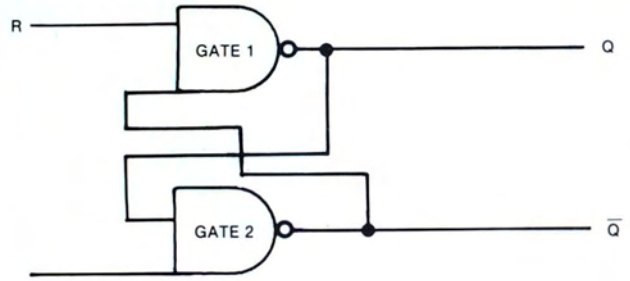


Figure 2. The input is coupled to Tr1 by C3. When the downgoing negative edge of the input reaches Tr1, then its collector voltage will rise which in turn will cause the base voltage of Tr2 to increase. After Tr2 has reached saturation it will turn off; therefore the collector voltage of Tr2 will drop, in turn turning off Tr1. It will be noted that C2 reduces Tr2 turnoff time.



R	S	Q	$\overline{Q}$
0	0	1	0
1	0	0	1
0	1	1	0
1	1	1	0

Figure 3. The truth table follow the rules for any logic circuit bistable multivibrator. In this case we are using the NAND gate configuration.

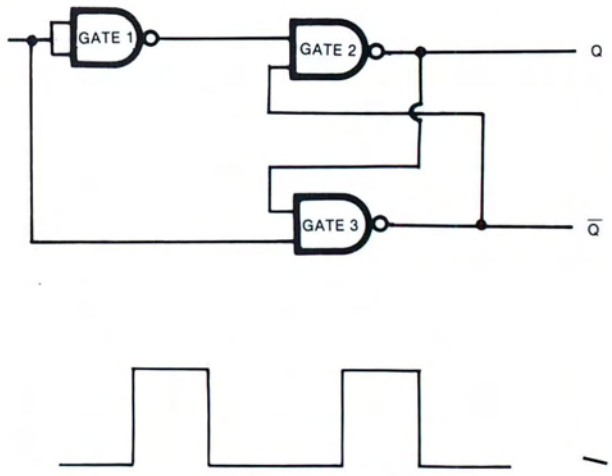


Figure 4. The inverter circuit is used as the follower when we want to change the input waveform into a different output wave.

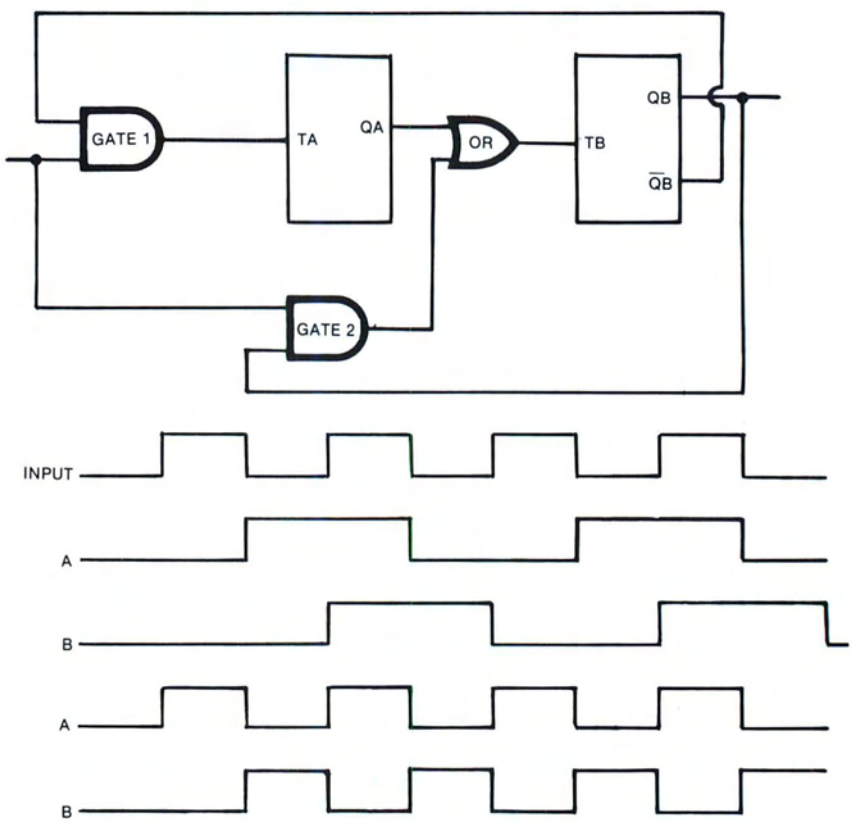


Figure 5. The OR gate is added to be able to count or divide by three by using an input and three outputs. Note that on QA and QB there is only one pulse with QB one clock cycle ahead of QA, and that on TA and TB there are two pulses with TB ahead of TA. This timing sequence enables the counter to set and reset.

or down-going change of the input which is the T terminal. This is shown in Figure 5. When an R-S-T is purchased, the user can apply it as an R-S-T flip-flop or if he wishes use it just as an R-S simply by not connecting the T into the circuit.

The R-S-T is particularly useful as a frequency counter. This can be accomplished by a down signal on T which causes the output at Q to change, hence alternating between different inputs at T brings about a change on Q's output. This type of action produces an output that has half the number of pulses in a given alloted time period. The output at Q is always a square wave provided that T's pulses are of the same time factor. This is shown in Figure 6.

The flip-flops when connected in series will divide by a power of two, four, eight, sixteen, etc., depending on how many there are in series. When using such an arrangement as a frequency counter, the answer will be based on the number of flip-flops used and will often be a number that is twice the number of flip-flops. For example, with two flip-flops in series the answer would be four, with eight flip-flops the quotient is sixteen, etc. When the count is completed it will automatically start the cycle over again.

The counter first begins counting by making sure that the Q outputs are all set to zero. For the rest of the discussion on the R-S-T flip-flop, we shall be working with the four-stage counter. After the counter has been set to zero, a certain number of pulses are applied to the input, this input is usually denoted by 2^n, the n denoting the number of flip-flops in series. The example in Figure 7 shows more clearly how a four-stage works.

It is often advantageous to use an AND gate when working with an R-S-T combination. This will enhance the dividing frequency of the counter itself. The idea is to allow the counter to divide to the "last count."[1] It will

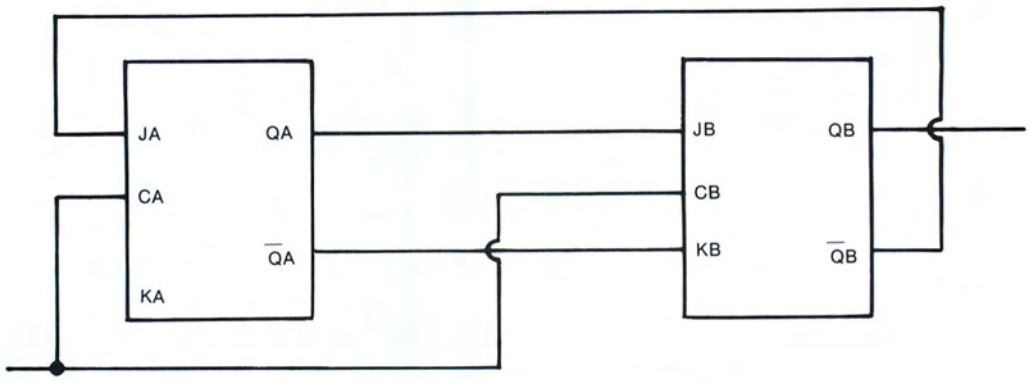


Figure 6. The J-K flip-flop follows almost the same principle in dividing as the R-S-T in that there is an input and two outputs.

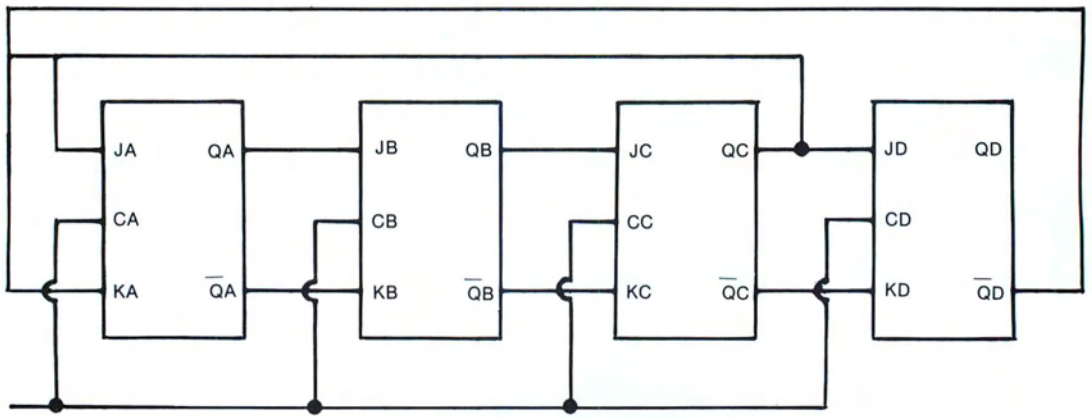


Figure 7. This counter divides by seven because there is one output from the final stage going back to the J input of the first stage, which resets the count, and also because of two inputs going to each succeeding stage.

also enhance the ability of the counter to handle the odd digits as well as the even ones. When using an AND gate, if the flip-flop is set to zero, then this will automatically start the counting sequence. This is done with one input of the AND input being connected to Q_B's output of the R-S-T which is set to 1 at the start. The first input that is high on the AND gates will not cause the R-S-T's to change state, but when it goes to zero, the flip-flop at (A) will toggle to one. The second flip-flop does not change its state because the input at T_B has not fallen. The input then goes back to high, which does not affect the change of either flip-flop, but when the input goes to zero, flip-flop (A) will change to a zero at the Q_A output and the second flip-flop will toggle, and the output at Q_B goes to one and Gate 1, which is tied to the output of $\overline{Q}_B$, will become inhibited. At this point the second gate will be enabled. When the input rises and falls again it will go to the second AND gate, whose output is tied to the input of an OR gate that is connected to Q_A, its state still remaining at zero. Flip-flop B will also toggle to zero, and the count starts all over.

The R-S-T counter is a serial counter because each stage has to wait for the pulse from the preceding flip-flop.

The next flip-flop is the J-K device. This is a synchronous flip-flop because of the fact that the clock terminal which corresponds to the toggle of the R-S-T has its output synchronized to the J and K input signal. The R-S-T is asynchronous because the output is not in correlation with its input.

The operation of the J-K goes according to its truth table.

The terminals J and K are the inputs but do not necessarily affect Q's output. They do determine, however,-what happens at Q on the downgoing or upgoing pulse at the clock terminal. This a synchronized output because it changed with the changes on the clock terminal.

The J and K terminals are either OR or AND gates. When using the OR gate, a 1 that is applied to one of the multiple inputs will cause it to trigger so as to have an output at Q. However, if an AND gate with multiple inputs is used all the J's or K's must have a 1.

Sometimes in logic design it will be necessary to tie the J and K inputs together and apply a trigger signal at that junction. This will also act as a clock terminal.

As I had said previously the J-K operates on the principle of the truth table. When Q_A and Q_B are both zero at the first count and a pulse arrives on the J-K terminals, then on the first flip-flop Q_A will toggle to a one and on the second flip-flop, Q_B will remain at zero. At the next input pulse Q_A will toggle again but this time Q_B will have a one on its terminal. When the third pulse arrives Q_A will still be zero and Q_B will be zero. This will start the count over again. These pulses are all "down-going pulses." If a square wave is used at the input, then the output waves at Q_A and Q_B will be the same rectangular waveform as on the "down-going pulse" except that there is no phase relationship between the high and low cycle.

The last flip-flop to be considered is the shift register. the flip-flops are connected together as stages or a staged flip-flop. Each flip-flop has an input and four outputs, in addition to a clock and reset terminal.

The often used application of a shift register is the conversion of "serial data" into "parallel data." This principle applies especially to calculators. For example, when multiplying 10 x 2, it will be fed into the logic circuitry one at a time by the user. The answer 20 is read by the LED's coming on all at the same time or in parallel.

REFERENCES

1. Streater, Jack W., *How to Use Integrated Circuit Logic Elements,* 1969.
2. Ward, Brice, *Solid-state Circuits Guidebook,* 1974.