

Moving to Altium Designer from PADS Logic[®] and PADS Layout[®]

Summary

This application note highlights the key conceptual differences you need to be aware of when moving from PADS[®] to Altium Designer. It identifies equivalent functionality, where to find it, and how to get started in this powerful and flexible electronic product development environment. You've made the switch to Altium Designer – a single, unified application that incorporates all the technologies and capabilities necessary for complete electronic product development – and now you're keen to get on with the design process.

This application note gives you a jump start on the basics of designing in Altium Designer, and maps out the key differences you need to understand when moving from the PADS[®] environment to Altium Designer. It also shows how easy it is to transfer your PADS Layout[®] designs and libraries into Altium Designer.

Transferring Your PADS Logic and Layout Designs

Translating complete PADS Logic and Layout designs, including PCB, Schematic files and library files can all be handled by Altium Designer's **Import Wizard** (Figure 1).

The **Import Wizard** streamlines the design translation by analyzing the PADS design files and offering defaults and suggested settings for project structure, layer mapping, PCB footprint naming, and so on.

Import Wizard				
Select Type of Files to Import				
Select the type of files you wish to import from the list	below.			
File Types	Description			
99SE DDB Files	99SE DDB (*.DDB)			
CircuitMaker 2000 Schematics and Libraries Files	CircuitMaker Schematics (*.CKT), CircuitMaker User Libraries (*.LIB), CircuitMaker			
Orcad Designs and Libraries Files	Orcad Designs (*.DSN), Orcad PCB (*.MAX), Orcad Design Libraries (*.OLB), Orca			
Orcad CIS Configuration Files and Libraries	Orcad CIS Config File (*.DBC), Orcad Library Files (*.OLB, *.LLB)			
PADS ASUI Design And Library Files	PADS ASUITPUB (*ASU), PADS ASUITPUB Library (*.D), PADS ASUITLogic (*.1% Dread Designe (*.DSNI), Dread Design Librariae (*.DLP), PADS ASUITLOGIC (*.ASU)			
P-CAD Des PADS Import Wizard				
Importing PADS Designs Choose the PADS design files to im	port.			
Add PADS designs to the list below for processing. PADS PCB files will be imported as Altium Designer PCB documents, P will be imported as Altium Designer schematic documents, and both be grouped into Altium Designer PCB projects.				
PADS Design Files				
🕼 C:\PADS Projects\padsnet.asc	🕼 C:\PADS Projects\padsnet.asc			
🙀 C:\PADS Projects\Layout_Eval_I	Routed.asc			
C:\PADS Projects\Samples\PGn	etlist.asc			

Figure 1: Import Wizard - PADS ASCII Design and Library files.

The **Import Wizard** only translates PADS ASCII versions 5.2 onwards and does not read PADS binary files. If you only have binary PADS files you will need to export these binary files into ASCII format from your PADS application, preferably in the ASCII 2005.2 format.

The PADS designs imported by the **Import Wizard** are captured as documents in individual PCB Projects which are created automatically after the translation in Altium Designer.

Errors in the translation are reported in a log file with the filename of the imported design with a LOG extension as shown in the **Reporting Options** page of the **PADS Import Wizard** as in Figure 2.



Figure 2: Import Wizard - Reporting Options to control the reports manager.

We will go through the import process in three sections; Importing PADS logic designs, Importing PADS Layout files and Importing PADS Library files below. We will cover the mechanics of each import process in detail.

Getting Started – Transferring Your PADS Logic Designs

Translating complete PADS Logic designs which are Schematic files can be handled by Altium Designer's **Import Wizard**. The Import Wizard streamlines the design translation by analyzing your files automatically. One Altium Designer schematic document is generated for each PADS Logic sheet within a Logic file by the Import Wizard. Each translated Logic file will be grouped into automatically created Altium Designer PCB project with an *.PrjPCB file extension.

Files in the Import Wizard translate as follows:

• PADS ASCII Schematic Logic sheets within a Logic file with an *. TXT extension translate to Altium Designer Schematic files with an *. SchDoc file extension.

Importing Which PADS ASCII Logic Files?

The Import Wizard supports Pads Logic versions 2005.0 and 2005.2 as well as the older Pads PowerLogic version 5.2. It is best to export Logic files that have the version 2005.2 as they contain the most data. These files have to be in ASCII format. The file extension used by the Pads ASCII format is \star .txt.

For the import of PADS Logic files, there are no specific settings in the **Import Wizard** in Altium Designer.

Ensure that when the Logic ASCII files are exported from the PADS application; enable all Logic data sections in the ASCII Output dialog in PADS application as shown in Figure 3.

All the data for translation needs to be in the ASCII file, which is why Decals, Part Types and Parts must all be enabled otherwise no components will be imported. Thus the Decals section need to be enabled for Part Types section and the Part Types section needs to be enabled for Parts section as well.

In some cases, you can skip some of the above settings such as Text and Lines which are usually used for the border and title blocks. You can use Altium Designer's Schematic border and title blocks instead.

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Figure 3: Exporting a PADS Logic file with the following sections enabled in the PADS application.

The Schematic designs normally do not require any libraries, and in fact doesn't use them. Currently the **Plot Params** section and the **Rules** section within a PADS file are ignored when files are being imported into Altium Designer.

Using the Import Wizard for PADS Logic Files

The Import Wizard can be launched from the Altium Designer File menu. Click on this menu command to invoke the wizard. Right-click pop-up menus are available for further control over the translation process through each page of the wizard.

Make sure you firstly export your PADS Logic files as ASCII files in the 2005.2 version. Incompatible or incorrect file formats are not imported and an error file with a LOG extension will be generated.

Once the PADS Logic files have been added in the Import Wizard's PADS Design Files list within the Importing PADS Designs page, you can toggle the options to control the Reports manager, review the output project structure and then specify the output directory to import the files in Altium Designer. Each PCB project is created for each PADS Logic schematic file in Altium Designer.

Getting Started – Transferring Your PADS Layout Designs

Translating complete PADS Layout designs which are PCB files can all be handled by Altium Designer's Import Wizard. The Import Wizard removes much of the headache normally found with design translation by analyzing your files and offering many defaults and suggested settings for project structure, layer mapping, PCB footprint naming, and so on. Complete flexibility is found in all pages of the Wizard, giving you as little or as much control as you would like over the file translation settings, before committing to the actual translation process.

Importing Which PADS Layout Files

There are different PCB file formats that can be exported from the PADS Layout package version 2005 and they are;

- PADS Layout V2005.2
- PADS Layout V2005.0 ٠
- PADS PowerPCB V5.0, V4.0, V3.5, V3.0 etc

The Units list (Figure 4) has two settings, Basic and Current units. The Basic setting causes the ASCII file to be in the database units. The Current setting exports units based on the design setting, which can be mils, mm, or inches.

The Expand Attributes section has two settings; Parts and Nets. Checking either of

these setting causes higher level attributes to be propagated into and exported with either the Parts or Nets or both depending on what is checked.

The Sections part of the dialog has a list of PADS objects that can be in an ASCII file. A PADS PCB ASCII file is divided into sections as outlined below which is taken directly from the PADS Help.

Item	Exported information
PCB Parameters	Global design information, such as units and colors
Reuse	Elements in, and the definition of, a physical design reuse
Text	Text
Lines	Two-dimensional lines
Clusters	Clusters and unions
Vias	Vias and dangling vias, jumpers, and pad stacks
Decals	Footprints
Packages	Electrical information
Parts	Component instances



Figure 4: PADS Layout ASCII File Export format

Item	Exported information
Jumpers	Jumpers If you plan to export to the PowerPCB V1.1 ASCII format, you cannot output complete jumper information. This is because PADS Layout considers jumper pins as vias and jumpers are exported as vias when you select the Vias check box.
Connections	Unrouted pin pairs
Routes	Traces, including route loops
Teardrops	Must export routes if you want to export teardrops. If you plan to export to the PowerPCB V1.1 ASCII format, you cannot output teardrops.
Miscellaneous	Information not included in other items
Rules	Clearance, routing, and high-speed rules
CAM	Information related to plot file configurations generated using CAM
Pour	Copper pours
Assembly Options	Assembly variants
Test Points	Test points and the test side (top, bottom, or both)
Attributes	Attribute Dictionary and all individual attributes and value assignments in the design. Status of attributes (read-only, system, ECO-registered, or hidden).
	Attributes are exported to the extent possible for formats previous to V3.0. Previous versions do not support all of the default attributes. Values through the attribute hierarchy are not exported.

Using the Import Wizard for PADS Layout Files

The **Import Wizard** can be launched from the Altium Designer **File** menu. Click on this menu command to invoke the wizard. Right-click pop-up menus are available for further control over the translation process through each page of the wizard. These translated files will be grouped into an automatically created Altium Designer PCB project (*.PrjPCB).

Files in the **Import Wizard** translate as follows:

 PADS ASCII PCB Layout (*.ASC) files translate to Altium Designer PCB files (*.PcbDoc).

Layer Mapping for PADS PCB ASCII Files

All used PADS PCB layers must be mapped to an Altium Designer layer prior to import when using the **Import Wizard**. There are additional options provided to control the automatic creation of design rules, missing vias and keep-out conversions as well.

It should be noted about how the layers are mapped on import for PCB designs. Layer Mapping is simply a mapping between the names of the PADS PCB layers and Altium Designer PCB layers. You can change as many mappings as you want as only suggested default mappings are given. This mapping is used by the **Import Wizard** to build the layer mapping for each PCB that can then be individually customized. The rationale here



Figure 5: Use the Layer Mapping Options from the Edit Mapping button in the Import Wizard to associate PADS PCB layers to Altium Designer layers.

is that should you wish to import ten PCB designs and you want to map the layer *Assembly 1* to *Mechanical Layer 1*, you would not have to customize each of the ten PCB designs in order to get the right layer mapping. The customized layer mappings are stored in a .INI file.

The advantage to importing in this manner is that batch management of layer mapping can save a lot of time when importing multiple designs. In this instance, the default layer mapping will be saved to your **Preferences**. The disadvantage to using this is that Default Layer Mapping is not always intelligent with differing structures in designs, and so some manual changes may be needed afterwards. You'll need to decide what is best for your situation.

PADS Import Wizard	? 🛛
Default Options Set the default options common to both the PCB and PCB library import processes.	
General Detride Pad Inner Value With Largest Found	

Figure 6: Turning the Override Pad Inner Value option on means that imported pads will have their sizes on the midlayers set to the largest size found.

Make sure you firstly export your PADS Layout files as ASCII files in the 2005.2 version. Incompatible or incorrect file formats are not imported and errors are stored in a text file with a LOG file extension.

Once the PADS Layout files have been added in the **Import Wizard**'s PADS Design Files list within the **Importing PADS Designs** page, you can toggle the options to control the Reports manager, review the output project structure and then specify the output directory to import the files in Altium Designer. Each PCB project is created for each PADS Layout PCB file in Altium Designer.

Getting Started – Transferring Your PADS Library Files

Translating complete PADS library files can all be handled by Altium Designer's **Import Wizard**. The **Import Wizard** removes much of the headache normally found with design translation by analyzing your files and offering many defaults and suggested settings.

Complete flexibility is found in all pages of the wizard, giving you as little or as much control as you would like over the file translation settings, before committing to the actual translation process. Each translated library file will be imported into an automatically created Altium Designer PCB project (*.PrjPCB).

The PADS application (Logic and Layout) both support four library types; (Decal, Part, Lines and CAE Decal files) however the **Import Wizard** can only translate three library types – Decal library, Part library and CAE Decal library only.

Importing which PADS PCB Library Files

The PADS package exports a decal library with footprint definitions in ASCII format using the file extension *.d. The conversion is very straightforward with the **Import Wizard** in Altium Designer; a PADS decal file is translated into an Altium Designer library document of PCB footprints. It is highly recommended to import the 2005.2 version PCB decal files (ASCII format).

Importing Which PADS Schematic Library Files

The PADS Logic package exports the Schematic symbols as CAE decals in ASCII format with the file extension *.c. This file only contains the definitions of the Schematic symbols, such as the graphics and pin orientation. The CAE files alone cannot be used to translate into Altium Designer Schematic components. A Schematic library component in Altium Designer is the "combination" of the PADS Logic symbol and component information such as gates and pin designator. The PADS package exports the specific component information into a file called "Part Library". It is an ASCII format file with the extension *.p.

You have to supply the Part Library (*,p) and CAE Decal (*,c) files in order to translate into an Altium Designer Schematic library. The CAE decal (*,c) files are used as a lookup for CAE (or symbol) definitions. The user can supply as many *,c and *,p files and add them in the **Import Wizard**, which will try to look up the gate name (CAE name) for the part reference.

The best way to smoothen the **Import Wizard** in Altium Designer process is to supply the set of CAE files (*.c) that have the CAE definitions that the parts (*.p) reference. For example, you can export the common libraries into the common.c file and add them into the **Import Wizard**.

Using the Import Wizard for PADS Library Files

The **Import Wizard** (can be launched from the Altium Designer **File** menu. Click on this menu command to invoke the wizard. Right-mouse click command menus are available for further control over the translation process through each page of the wizard.



Figure 7: PAD ASCII libraries with PCB decals (*.d), CAE decals (*.c) and Parts (*.p).

Files in the Import Wizard translate as follows:

- PADS ASCII Library PCB decal files (*.d) as Altium Designer PCB library files with a *. PCBLIB file extension.
- PADS ASCII Library CAE decal files (*.c) and PADS ASCII Library Part Type files (*.p) as Altium Designer library files with a *.SCHLIB extension.

Layer Mapping for PADS ASCII Library Files

All used PADS PCB layers must be mapped to an Altium Designer layer prior to import when using the **Import Wizard**. There are additional options provided to control the automatic creation of design rules, missing vias and keep-out conversions as well.

It should be noted about how the layers are mapped on import for PCB designs. Layer Mapping is simply a mapping between the names of the PADS PCB layers and Altium Designer PCB layers. You can change as many mappings as you want as only suggested default mappings are given. This mapping is used by the **Import Wizard** to build the layer mapping for each PCB that can then be individually customized. The rationale here is that should you wish to import ten PCB designs and you want to map the layer *Assembly 1* to *Mechanical Layer 1*, you would not have to customize each of the ten PCB designs in order to get the right layer mapping. The customized layer mappings are stored in a .INI file.



Figure 8: Use the Layer Mapping Options from the Edit Mapping button in the Import Wizard to associate PADS PCB layers to Altium Designer layers.

The advantage to importing in this manner is that batch management of layer mapping can save a lot of time when importing multiple designs. In this instance, the default layer mapping will be saved to your **Preferences**. The disadvantage to using this is that Default Layer Mapping is not always intelligent with differing structures in designs, and so some manual changes may be needed afterwards. You'll need to decide what is best for your situation.

Once the PADS library files have been added in the **Import Wizard** PADS Design Files list within the **Importing PADS Designs** page, you can toggle the options to control the Reports manager, review the output project structure and then specify the output directory to import the files in Altium Designer. Each PCB project is created for each PADS library file in Altium Designer. Remember a set of *.p and its corresponding *.c files is treated as a translated single library file in Altium Designer.

PADS Import Wizard	? 🔀
Default Options Set the default options common to both the PCB and PCB library import processes.	
General Options Image: Constraint of the second	

Figure 9: Turning the Override Pad Inner Value option on means that imported pads will have their sizes on the midlayers set to the largest size found

The Altium Designer Environment

The Altium Designer environment offers a complete electronic product development environment for all areas of design – from schematic capture to the generation of PCB output, as well as complete FPGA design, development and on-chip debugging.

The environment is fully customizable, allowing you to set up the workspace to suit the way you work. Consistent selection and editing paradigms across the different editors allow you to easily switch between various designs tasks all within the Altium Designer environment.

User Interface Elements

Perhaps the single biggest difference that you will notice when you start working in Altium Designer is that there is only one application used to create and edit all design files, regardless of the type of file – schematics, PCB, library, text, and so on. No longer will you have to switch between different applications when you want to move from viewing the schematic to the PCB. All the files (referred to as documents which are described further below) open in the same executable, each appearing on a separate document tab within Altium Designer.



Figure 10. As you move from one type of document to another from the Projects panel, the menus and toolbars automatically switch, giving you the right editing environment for that document.

Altium Designer has full support for multiple monitors too. If you have multiple monitors on your PC you can easily drag a document out of Altium Designer and drop it on the second monitor, greatly enhancing your design productivity.

To get you started let's review some of the basic terminology that you'll need to know as you work in Altium Designer.

Working with Documents

In PADS Layout all design work begins on the workspace, the logical working area of the PCB design. Each design is saved to a single design file (*. PCB file). In PADS Logic, all design work begins on the sheet, the logical working area of the schematic design. There can be multiple schematic sheets within a single PADS schematic design file (.SCH file).

In Altium Designer, the logical design area begins with a document, and for each document there is a file stored on the hard drive. This means that for each Altium Designer schematic sheet there is a file. This is an important conceptual difference to remember.

There can also be multiple design documents of varying types, depending on the nature of the design you are working on in Altium Designer. Getting started, most PADS users will be interested in the schematic and PCB document types as these are the files that their designs will be translated to (Figure 11).

Where's all my stuff? Accessing Your Project Documents

All design documents and generated output files, including your translated PADS design files, are stored as individual files on your hard disk. Your design documents can be accessed by opening the project first and then opening the individual documents or any individual document can be opened directly, using the **File » Open** menu command.

Workspace Panels

Workspace panels are a basic form of the Altium Designer user interface and replace the use of panes and explorer windows from PADS Layout. Whether specific to a particular document editor or used on a more global, system-wide level, they present information and controls that aid your productivity and allow you to design more efficiently.

Accessing Panels

When Altium Designer is first started, a number of panels will already be open. Some panels, including the **Files** and **Projects** panels, will appear grouped and docked to the left side of the application window. Others, including the **Libraries** panel will be in pop-out mode and appear as buttons on the right-hand border of the application window.

Many elements of the environment will appear intuitive to PADS users, helping as you to start exploring the system. For example, the **Projects** panel will appear similar to the PADS **Project Explorer**; except that since it is not limited to schematic design data it can include the PCB, all libraries, output files, as well as other project documents, such as Word or Excel files.

You will also notice that your translated files will be grouped somewhat



Figure 11: Basic file operations: new PCB and schematic document types can be easily created via the File » New menu, or by right-clicking on the project in the Projects panel.

differently than you are used to seeing. Whether you need to open a specific document such as a schematic, or need information or control to design on a more global, system-wide level, it can all be done using the **Projects** panel.



Figure 12. At the bottom of the Altium Designer window are a number of buttons that provide quick access to the available workspace panels, in context with the document editor that you are using.

As you open and make active the documents within various editors you will notice that the resources and available panels will

change dynamically; the menus, available panels, and toolbars will quickly change to match the document type you are currently focused on for editing. You'll want to familiarize yourself with how to access these panels, manage, group, and control your display modes to get the most out of the productivity features that are provided here. Press **F1** when the cursor is over a panel for more information on that panel.

Projects Panel

Altium Designer, like PADS, also features project management capabilities but there are conceptual differences you'll need to get firm in your mind first. The Altium Designer approach to managing your project is that *all* design documents (schematic, PCB, libraries, etc.) are linked to the project file, both for management and access to certain design features such as design verification, comparison, and synchronization.

The Altium Designer presentation through the **Projects** panel provides high visibility and a complete view of everything you need in your project, not just the schematic part of it. The project file, which is what you are viewing in the **Projects** panel, contains links to all your documents in your design, as well as any other project-level definitions. The essential concepts of project-based design are discussed later in the *Project-based design* section.

Refer to the document, *Altium Designer Panels Reference*, for a comprehensive reference about all the workspace panels that can be accessed from within the Altium Designer environment. Their function,



Figure 13: The Projects panel is your view into your project. Right-click in the Projects panel to access all project-related commands.

content and use, as well as many specific tips and notes for using them as part of your design process are fully explained.

Project-based Design

Now that we've covered some of the basics of the Altium Designer environment, it is time to talk about designing. The starting point for every design created in Altium Designer is a project file.

It's a simple and important concept – an Altium Designer project is a set of design documents whose output defines a single implementation. For example, the schematics and PCB in a PCB project output the fileset required to manufacture a single printed circuit board, while the schematics (and HDL) in an FPGA project output the fileset required to program a single FPGA. The project file brings together all of the design documents that make up the project.

Altium Designer supports a number of different types of projects, including: PCB, FPGA, Embedded Projects, Core Projects, Integrated Libraries, and Script Projects.

Project File Role

The project file stores all project-relevant settings, including a link to each document in the project, and all project-relevant settings. Each document in the project is stored as a separate file, which is linked to the project via a relative reference for files on the same logical drive, or an absolute reference for files on a different logical drive. Outputs generated from the project are also referenced in the project file.

The exact set of project options stored will depend on the project type. It will include those options configured in the *Options for Project* dialog, such as:

- Compiler error check settings
- Design synchronization settings
- Design compiling settings
- Location of output files
- Multi-channel annotation settings
- Output settings such as reports, print Gerber, etc.

From the Knowledge Center in Help, links for videos and understanding project management features of Altium Designer can be found in the Documentation Library » The Altium Designer Environment » Project Management.

Projects Panel Role

The **Projects** panel is one of the more commonly-used panels in day to day work. It allows you to make changes to your project options, add to and remove documents from the project, change the display options of projects, change the order of documents within a project, or even how you would like to display information in the **Projects** panel.

All of your translated design files will appear in the **Projects** panel, organized into their respective projects that were automatically created for them. The environment also supports multiple projects being open at the same time. These can be unrelated projects, or related.

Refer to the application note *Project Essentials* for all the basics of using project files effectively: creating, adding and removing files from a project; setting project options, as well as understanding the various project types.

Compilation – a Cornerstone of Altium Designer

Compilation is a cornerstone concept of the Altium Designer environment, and a fundamental difference from PADS. Compilation is a process that allows you to harness many powerful design features and can be done with your translated PADS Layout and PADS Logic files, or even just a net list. Compilation can also be done on other types of documents such as library documents (described later in this application note).

When you select **Project** » **Compile Project** the compilation process works out the structural relationships between the source schematic documents in the project, then determines the net-level connectivity within each sheet, and finally the connectivity between the sheets. All this component and connective intelligence from your schematics design is written into an internal data structure that can then be used for many post-compilation activities, such as comparing and showing differences between schematics, parameter managing, parametric navigation of your design, cross probing back and forth between the schematics and PCB, and much more.

Where are my nets and components from my design?

You're going to notice that connectivity is not as explicit in your design as it was before, but rather has to be extracted from the design using the compilation process. This is available through the right-click menu in the **Projects** panel, or using the **Project** » **Compile Project** menu command.

Once the design is compiled the sheet-level hierarchy, as well as all the components, nets and buses are displayed in the **Navigator** panel. From here you can easily locate any component, bus, net or pin throughout the entire design. And if you hold the **ALT** key as you click on an object in the **Navigator** panel it is highlighted on the PCB as well as the schematic – no longer will you need to inspect net lists to review design connectivity.

Verifying Your Design – Expanded Error Checking

Another benefit that results from compiling a project in Altium Designer is built-in error reporting. This is completely configurable for your needs and can be done before your project is compiled. Right-click the project file and select **Project Options** from the pop-up menu, or access the command from the **Project** menu.

C	ptions for PCB Project Powerboard Benchmark.PrjPCB		?×
<	Error Reporting Connection Matrix Class Generation Comparator ECO Generation Options Multi-Channel Default Prints	Search Paths Parameters	
	Violation Type Description	△ Report Mode	^
	Violations Associated with Documents		
	Conflicting Constraints	🚞 Error	
	Duplicate sheet numbers	🗀 Warning	
	Duplicate Sheet Symbol Names	🚞 Error	
	Missing child HDL entity for sheet symbol	🚞 Error	
	Missing child sheet for sheet symbol	🚞 Error	
	Missing Configuration Target	🚞 Error	
	Missing sub-Project sheet for component	🔁 Warning	
	Multiple Configuration Targets	🚞 Fatal Error	
	Multiple Top-Level Documents	Error	
	Port not linked to parent sheet symbol	Error	
	Sheet Entry not linked to child sheet	Error	
	Unique Identifiers Errors	Warning	
	Violations Associated with Hamesses		
	Lontlicting Harness Definition	Fatal Error	
	Harness Lonnector Lype Syntax Error	Warning	_
	Missing Harness Type on Harness	E Fatal Error	=
	Multiple Harness Types on Harness	🛄 Warning	
	UNKNOWN Harness Type	Fatal Error	
	Adding bidden with yets		
	Adding haden next to sheet	warning	
	Auding refins from inducement of ref	Warning	
	Build Point of Berger	Error	
	Dis Operational Pair Net Connection Polarity Inversed	Warning	
	Differential Pair Net Uneconnected To Differential Pair Pin	Error	
	Differential Pair Unproperly Connected to Device		
	Dunlinate Nets		
		Constanting and the second sec	×
	Set To Installation Defaults	OK Canc	el

Figure 14. The Error Reporting tab in Project Options dialog.

You may wish to get a better picture of the entire development cycle and how it unfolds from an engineer's perspective by reading *An Overview of Electronic Product Development in Altium Designer*.

Immediate Access to Help

For further information about the Favorites panel as well as many other topics in Altium Designer, open the **Knowledge Center** panel (via the **Help** button on Status line). When the **Knowledge Center** panel is open it will auto-load help on the object, command, or menu entry currently under the cursor if you pause, or you can press **F1** to load the topic immediately.

Projects

Workspace1.DsnWrk

File View O Structure Editor

Source Documents

CPU_Design.SchDoc

🗆 🗾 cpu design.PrjPCB

cpu design.PrjPCB

🗆 🛄 Libraries

🕀 🥅 Generated .

Design Capture Using PADS Logic

Project Hierarchy

For any project involving multi-sheet design, there are two choices that need to be made – defining the structural relationship between the schematic sheets (flat or hierarchical), and determining the method of electrical connectivity between the circuitry on those sheets. Display of the project hierarchy is in Altium Designer's **Projects** panel.

Sheet Structure in PADS Logic

Like Altium Designer, PADS Logic supports flat and simple hierarchical designs. Both use a block-like symbol to define sheet-to-sheet structure in a hierarchical design, called a *Sheet Symbol* in Altium Designer, and a *Hierarchical Block* in Logic. In both, the symbol references the lower level schematic. In Altium Designer this is simply another schematic sheet.

Typically a flat Logic design is one schematic (folder), with the design being drawn on as many pages as required in that schematic (folder). For a hierarchical design, the hierarchical block symbol (or part with an attached schematic sheet or model) is the mechanism used to partition the major functional regions of a design.

For a simple hierarchy, each hierarchical block, or part with an attached schematic folder represents a unique design module.

Sheet Structure in Altium Designer's Projects Panel



📕 CPU_Power_Supply.SchDoc 🖹

🗆 🚞 Schematic Library Documents

😤 CPU Design_Library.SchLib

Workspace

Project

• 🛃 🌒

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In Altium Designer, hierarchical designs can likewise be viewed and navigated also as a tree structure through the **Projects** panels. Once the project has been compiled at least once, the **Projects** panel will show the hierarchical structure. In a hierarchical design you can think of the first sheet as the parent and those represented by sheet symbols as children (note that child sheets can have their own children too). With that idea in mind, the hierarchy tree makes it easy to navigate and get the overall picture of your design, the hierarchy of the example CPU Design shown in Figure 15 as it appears in Altium Designer.

A multi-sheet design project in Altium Designer can also be arranged as a hierarchical structure of logical blocks, where each block can be either a schematic sheet or a HDL file (VHDL or Verilog). At the head, or top, of this tree structure is a single master schematic sheet, more commonly referred to as the project's top or parent sheet.

The structure of the sheets is formed through the use of a special symbol called a sheet symbol. Each of the source documents that make up the design are represented on the parent sheet by a sheet symbol. The Filename property of each sheet symbol references the schematic sub-sheet that it graphically represents. In turn, a schematic sub-sheet can also contain further sheet symbols referencing lower schematic sheets or HDL files. In this way you can define a structural hierarchy of source documents that can be as simple or complex as your needs require.

Defining Net Connectivity

In PADS Logic, net connectivity is made using off-page symbols, hierarchical symbols and globals. Nets between schematic pages within a single schematic folder are connected through the off-page symbols while the hierarchical symbols connect the nets between the schematic folders. Globals are used to connect power/ground nets throughout the design.

Altium Designer uses a similar set of net identifiers to create net connectivity. Within a schematic sheet you can use *Wires* and *Net Labels*. Between schematic sheets, nets in a flat design are typically connected using *Ports*, but *Off-Sheet Connectors* are also available. Nets in a hierarchical design are connected from a *Port* on the lower sheet to a *Sheet Entry*

From the Knowledge Center in Help, links for understanding in more detail how Design Capture and connectivity works in Altium Designer can be found in the Documentation Library » Design Capture » Multi-Sheet and Multi-Channel Designs.

of the same name, in the sheet symbol that represents the lower sheet. Power/ground nets are connected using Power Ports.

Configuring for Design Connectivity

Altium Designer supports different types of design connectivity, and this must be set to suit the structure of the design. The type of sheet-to-sheet connectivity is referred to as the *Net Identifier Scope*. It is set in the **Options** page of the *Options for Project* dialog (Figure 16), and saved with the project.

In the Net Identifier Scope list you can select from the following connectivity options:

- Automatic (Based on project contents)
- Flat (Only ports global)
- Hierarchical (Sheet entry <-> port connections)
- Global (Net labels and ports global)

The **Import Wizard** handles connectivity automatically through the translation process and will give you the **Automatic (Based on project contents)** configuration by default. This option is simply an instruction to Altium Designer's design compiler to determine which of the other three options are best suited for the connectivity in your design.

Hierarchical blocks are mapped as sheet symbols, and they will translate to sheet symbols in Altium Designer. In Automatic mode, the design compiler then looks at the sheet symbols on the top sheet. If there are sheet entries (hierarchical pins) in them, it will assume vertical connectivity, and internally use the Hierarchical option. If there are no sheet symbols on the top sheet, or if there are sheet symbols but they do not include any sheet entries, it will assume horizontal connectivity for which there are two ways that Altium Designer supports this: Flat and Global. In order to determine which of these two options to use, the design compiler looks for ports or off-sheet connectors on the subsheets. If there are any it uses the Flat option, if there are no ports it uses the Global option.

Options for PCB Project CPU Design.PrjPcb	· · · · · · · · · · · · · · · · · · ·
Error Reporting Connection Matrix Class Generation Cor	nparator ECO Generation Options Multi-Channel Default Prints Search Paths Parameters
Output Path: C:\Program Files\Altium Designer\Designs Output Options Image: Compile Image:	ICPU Design\Out CPU Design\Out
Netlist Options Allow Ports to Name Nets Allow Sheet Entries to Name Nets Append Sheet Numbers to Local Nets Higher Level Names Take Priority Power Port Names Take Priority	Net Identifier Scope Automatic (Based on project contents) Allow Pin-Swapping Using These Methods Adding / Removing Net-Labels Changing Schematic Pins
Set To Installation <u>D</u> efaults	OK Cancel

Figure 16. From Project » Project Options, Options tab, you can set the Net Identifier scope.

Remember that you can easily go back and change this configuration after the translation process through the *Project Options* dialog from the **Project** menu. The **Import Wizard** also allows PADS users to determine how they want their junctions to import, and also log any errors or warnings that you can check later after importing.

Defining net connectivity, net identifiers, scoping and how it all relates to multi-sheet design is a must read for PADS users and is fully explained in *Connectivity and Multi-Sheet Design*.

Design Synchronization

Design synchronization is fully integrated in Altium Designer without the need for passing a net list. Synchronization in Altium Designer is also bi-directional, allowing you to make annotation changes and component property updates in both directions between your schematic and PCB, in a single operation.

Again, an important and fundamental premise of Altium Designer is that the setup of the design's connectivity is driven from the schematic through to the PCB. This is also similar to PADS. If you are making connectivity changes in the opposite direction (from PCB to Schematic), a report is generated and these updates can then be performed on the schematic.

The synchronization feature is used when you first transfer from the schematic to the new blank board, or when you make design changes that need to be passed over.

For more information on design transfer and design synchronization, read the article *Finding Differences and Synchronizing Designs*.

As well as being able to detect electrical differences, such as changed designators, component values or net connectivity, Altium Designer also include a physical difference engine, which can find schematic and PCB layout changes – ideal for examining changes between different revisions of a board.

Complex Hierarchy

Complex hierarchy is the general term used throughout the industry to describe the process of using multiple instances of the same sheet in a schematic hierarchy. This important concept is supported by Altium Designer.

Multi-channel Design

Traditionally, a design that included complex hierarchy had to go through a process of 'flattening' or 'expanding' the hierarchy at some point, to uniquely instantiate every component and net. Altium Designer does not need to do this, so this multiple-instantiation capability is referred to as multi-channel design instead of complex hierarchy.

Like complex hierarchy, multi-channel design is the ability to reference a child sheet multiple times. It can be done by placing multiple sheet symbols, each referencing the same sub-sheet, or it can be done by placing a single sheet-symbol and using the Repeat statement to generate an array of sub-sheets. This is built on the complex hierarchy architecture of multiple instances, but in this case the parent object is expanded by the design compiler at the time of compilation (discussed below).

Multi-channel design also supports multiple levels. For example, a 32-channel design could be structured over two levels, having 4-banks of 8-channels, to create the final 32-channels. Additionally you can wire signals to either all of the channels or use a bus where one member of the bus goes to each channel. Altium Designer is the only electronic design platform to offer this concept.



There are several example multi-channel designs that come with Altium Designer that you may wish to look at. These include the *Multi-Channel Mixer, Peak Detector* and *PortSwitcher,* all three designs can be found in the *\Examples\Reference Designs* folder of your Altium Designer installation. Once you have opened one of the examples you should compile it, and then look for the tabs at the bottom of each schematic sheet.

For more information on multi-channel designs, refer to the article Multi-Channel Design Concepts.

Parametric Multi-channel Design

Support for multi-channel design – designs where the same section of circuitry is repeated – is an outstanding strength of Altium Designer. The ability to be able to make each channel different by passing parameters to it from the parent sheet symbol is also supported, and is referred to as parametric hierarchy.

Using parametric hierarchy you can parametrically define the component value, supporting the situation where a component does not have the same value in each channel. Parametric components are defined by declaring their value as a parameter of the sheet symbol above, and then referencing that parameter on the target component.

A tutorial that shows how to create a multi-channel design in the Schematic Editor, including the use of sub-sheets, sheet symbols, and the **Repeat** command may be found in *Creating a Multi-channel Design*.

The Schematic Symbol Is the Part...

As an expert PADS Layout user, you'll know that *parts* form the basic building blocks of design in PADS Layout. Parts are defined as having a part type, a logic family, number of pins, number of gates, and signal pins. The term *component* is only used when the part becomes placed as a physical object in the PCB layout design.

In PADS Layout (PCB), a part can represent one or more physical components. Parts in PCB designs usually correspond to physical objects: gates, chips, connectors, objects that come in packages of one of more parts. Multiple-part packages are physical objects that are comprised of one or more parts.

From the Knowledge Center in Help, links and videos for understanding the essentials of component, model, and library concepts in Altium Designer can be found in the Documentation Library » Library and Component Management. In PADS Logic, a part is a logical entity that is described graphically by a symbol, pins and various properties. As parts are placed in a schematic design, Capture maintains the identity of the part for back annotation, net listing, bills of materials, and so forth. At the very minimum, a part requires a part name, a part reference prefix, and a name of a PCB footprint.

These two definitions that use the same term depending on the context of design may initially cause some confusion in the new environment which uses the term *component*. But it is not unlike how things work in Altium Designer except that the schematic symbol is effectively the part for all phases of design, and not just the PCB Layout portion of it.

In Altium Designer, the logical symbol is assumed to be the essential starting point of a component. It can be initially defined at minimum as a name in a schematic library to which pins and any graphical symbols or alternative display options needed for implementation may be added. This flexibility allows a component to be represented in different ways during the design and capture process. This may not only be as a logical symbol on the schematic, but also be a footprint on the PCB or even as a SPICE definition for simulation.

Altium Designer Components



Figure 17: Altium Designer symbols can have multiple footprints and symbol models.

For a tutorial that steps you through all the basics of creating components, read Creating Library Components.

The fundamentals of how components are defined, their properties, and basic relationships between components, models and library concepts are explained further in *Component, Model, and Library Concepts*.

Design Rules

Designs today may have specific requirements for individual nets, components, as well as such issues as crosstalk, reflections, and net lengths. It's not possible to satisfy all the requirements of PCB designs by considering only clearances between tracks, pads, and vias. These requirements lead to a couple major conceptual distinctions in how design rules are integrated and defined in Altium Designer as compared to how you understood them coming from PADS Layout.

All design rules in Altium Designer, whether they are for layout, testing, or fabrication, are integrated and accessed from a single dialog – the PCB Rules and Constraint Editor. This is unlike PADS Layout where design rules are accessed from separate locations in the product.

Additionally, rules are not pre-defined but user-defined, and consequently very powerful. All default rules are based on a scope (described later) that applies to the whole board, with the exception of Fanout Control rules. With a well-defined set of design rules, you can complete boards of the toughest requirements.

Design Rule Categories

True to the unified nature of Altium Designer, which incorporates all phases of electronic design, design rules are accessed from a single dialog – the PCB Rules and Constraint Editor. There are 10 rule categories that cover all respective aspects of design verification.

PADS Layout Rule Category	Altium Designer Rule Category	Comments	
Clearance	Placement	Room Definitions, Component Clearances, Component Orientations. Permitted Layers, Nets to Ignore, and Component Height.	
Routing	Routing	Differential pairs routing can be checked from within the PCB Editor. Widths, topologies, priority, layers, corners, via styles and fanout control.	
High Speed	High Speed	Matched Net Lengths, Length and parallel segments. All rules easily checked between layout and the schematic without importing.	
*	Electrical	Integrated into Altium Designer's PCB Editor.	
Fabrication	Manufacturing	Verified within the PCB Editor environment using the CAM Editor. Minimum Annular Ring, Acute Angle, Hole Size, and Layer Pairs.	
*	SMT	SMD To Corner, SMD To Plane, and SMD Neck-Down.	
*	Plane	Power Plane Connect Style, Power Plane Clearance and Polygon Connect Style.	
*	Mask	Solder and Paste Mask Expansion	
Test Point	Test Point	Styles and usages	
*	Signal Integrity	In addition to standard set of design rules for DRC, signal integrity analysis is integrated directly into the PCB Editor (Tools » Signal Integrity).	

Table 1. A table of the more commonly-used PADS Layout design rules terms and their closest respective Altium Designer equivalents (* indicates that this rule is not checked as a part of the core design rules in PADS Layout).

Creating and Editing Design Rules

All categories of design rules can be created, edited and managed from a single location in Altium Designer. With the PCB as the active document, select **Design » Rules** from the main menu to open the *PCB Rules and Constraint Editor* dialog (Figure 18).

NPCB Rules and Constraints Editor [mil]								? 🗙
Design Bules	Name (D.:	En	Turce	Catagory	Cases	Attributes	
Electrical	P Esperit BCA	1		Fanaut Cantral	Reuting		Stule Auto	Direction
	Fariout_BCA	I E		Fariout Control	Deuting	ISDCIA	Style - Auto	Direction -
	Fanout_Derault	0		Fanout Control	Routing	All	Style - Auto	Direction -
The Short Circuit	Fanout_LLL	2		Fanout Control	Routing	ISLUU	Style - Auto	Direction -
	STANDUT_Small	4		Fanout Control	Routing	[CompPinCount < 5]	Style - Auto	Direction -
Bouting	Solic Fanout_SOIC	3		Fanout Control	Routing	IsSOIC	Style - Auto	Direction -
± strought	Net_Via_Style_1	1	~	Routing Via Style	Routing	InNet('GND') Or	Pref Size = 22	2mil Pref I
E S Bouting Topology	Set_Width_1	1	✓	Width	Routing	InNet('GND') Or	Pref Width = !	50mil Mir
E - Bouting Prioritu	🚟 RoutingCorners	1	✓	Routing Corners	Routing	All	Style - 45 Deg	gree Min
Bouting Lauers	🚟 RoutingLayers	1	✓	Routing Layers	Routing	All	TopLayer - Er	nabled Mid
E Bouting Corpers	端 RoutingPriority	1	✓	Routing Priority	Routing	All	Priority = 0	
E Sa Bouting Via Style	a RoutingTopology	1	✓	Routing Topology	Routing	All	Topology - Sł	nortest
	a RoutingVias	2	~	Routing Via Style	Routing	All	Pref Size = 50	Jmil Pref I
THE SMT	aa Width	2	~	Width	Routing	All	Pref Width = 1	10mil Mir
 Solder Mask Expansion Paste Mask Expansion Plane Testpoint Manufacturing Minimum Annular Ring Acute Angle Hole Size High Speed Parallel Segment Length Matched Net Lengths Daisy Chain Stub Length Vias Under SMD Maximum Via Count Placement Macinel Integrity 	<							
<u>R</u> ule Wizard						OK Can		Apply

Figure 18. The PCB Rules and Constraint Editor dialog, where all design rules can be managed.

Using Design Rules Checking (DRC)

Like PADS Layout, Altium Designer features both batch and online DRC. Options for enabling and using these two modes are fairly intuitive for PADS Layout users and work in a similar fashion. However, both the logical and physical integrity of your design (in comparison to PADS Layout where DRC is limited to layout design rules) can be verified. Checks can be made against any or all enabled design rules and can be made online as you are working. They can also be defined as a batch check, with results reported immediately in the **Messages** panel as well as a generated report.

Batch DRC

Batch DRC allows you to manually run a design check at any time during the board layout process, similar to PADS Layout. Configuring for this is done through the *Design Rule Checker* dialog, accessed through **Tools » Design Rule Checker** in the PCB Editor. When setting up your batch DRC, additional options can be defined by clicking on the **Report Options** folder, in the folder-tree pane of the *Design Rule Checker* dialog. These options include the generation of the DRC report.

After the check has completed, all violations will appear in the Messages panel.

Design Rule Checker	? 🔀
Protect Options Image: Protect Check Image: Protect Check	DRC Report Options Create Report File Create Violations Sub-Net Details Internal Plane Warnings Verify Shorting Copper Report Drilled SMT Pads Report Multilayer Pads with 0 size Hole Stop when 500 violations found NOTE: To generate Report File you must save your PCB document first. To speed the process of rule checking enable only the rules that are required for the task being performed. Note: Options are only enabled when corresponding rules have been defined. On-line DRC tests for design rule violations as you work. Include a Design Rule in the Design-Rules dialog to be able to test for a particular rule type.
Run Design Rule Check	Close

Figure 19. After setting up all your options, a batch DRC is initiated by clicking the Run Design Rule Check button.

In the folder-tree pane on the left side of the dialog, each of the design rules categories whose rule types can be checked are listed under the **Rules To Check** folder. Click on the root folder (**Rules To Check**) to list all checkable design rule types, across all categories, in the main editing window of the dialog (Figure 19).

Online DRC

Like PADS Layout, Online DRC is turned on as an option in the **PCB Editor** - **General** page of the *Preferences* dialog **Tools** » **Preferences** (Figure 20). When enabled, Online DRC runs in the background as you work flagging and automatically preventing design rule violations.

Preferences			? 🛛				
System	PCB Editor – General						
	Editing Options	Autopan Options					
Transparency	Online DRC	Style	Adaptive 🖌				
Design Insight	Snap To Center 📃 Smart Component Snap	Speed	1200				
Projects Panel	Double Click Runs Inspector	 Pixels/Sec 	O Mils/Sec				
File Types	Remove Duplicates						
- A New Document Defaults	Confirm Global Edit	Space Navigator	Options				
Installed Libraries	Protect Locked Objects	Disable Rol	II				
	Confirm Selection Memory Clear	Polygon Repour					
🗄 🚞 Version Control	Click Clears Selection						
Embedded System	Shift Click To Select Primitives	Repour	Never				
	Smart Track Ends	Threshold	5000				
Board Insight Display	Other	Eile Format Chan	ge Report				
Board Insight Lens	Undo/Redo 30	Disable op	ening the report from older versions				
Interactive Routing	Rotation Step 90.000	Disable op	ening the report from newer versions				
mag irue iype Fonts							

Figure 20. Online DRC is an option that has to be turned on in the Preferences dialog.

You can also conveniently enable or disable Online and Batch checking for each rule you wish to check in the *Design Rule Checker* dialog (Figure 21).

Design Rule Checker			?	X
Design Rule Checker	Rule Clearance Parallel Segment Vidth Length Matched Net Lengths Daisy Chain Stub Length Routing Via Style Short-Circuit Un-Routed Net Vias Under SMD Maximum Via Count Minimum Annular Ring Acute Angle Room Definition SMD To Corner Component Clearance	Category Electrical High Speed High Speed High Speed High Speed High Speed Online DRC - Used C Online DRC - All On High Speed Online DRC - All Off Batch DRC - All On Batch DRC - All On Batch DRC - All Off High Speed Manufacturing Placement SMT Placement		
	Component Unentations	Placement Signal Integrity Signal Integrity		
	Mr. Overshoot - Rising Edge	Signal Integrity		~
<u>R</u> un Design Rule Check			Close	

Figure 21. Use the options available from the right-click pop-up menu to quickly enable/disable checks of all rule types, or to enable checks of all used rule types only.

The application of Design Rules and a comprehensive reference for setting up design rules in a PCB design can be found in the *Design Rules Reference*.

Scoping

A new concept in Altium Designer's PCB Editor, rules scope – the extent of a rule's application – replaces the Rules Hierarchy from PADS Layout. A scope is effectively a query that you build to define all the member objects that are governed by that rule, giving you full control.

For the sake of a baseline comparison, let's review the Rules Hierarchy of PADS Layout. These rules rely on a pre-defined list format where higher numbers on the list have precedence over those that are lower:

- Default
- Class
- Net
- Group
- Pin Pair
- Decal/Component

In the PADS Layout rules schema, Default rules are considered level 1 and are the lowest while Decal and Component rules represent the highest. Conditional layer rules can be applied for an additional level of precedence. For example, a Default with a conditional layer rule would be higher in the precedence hierarchy than a simple Default rule.

In Altium Designer, scoping allows you to decide exactly what a rule's precedence will be and how it will be applied to target objects through a query. You can even define multiple rules of the same type, but each targeting different objects. Queries are easily accessed for any rule (Figure 22). **Advanced (Query)** options are also available to help you write your own, more complex queries.

It may arise that a design object is covered by more than one rule with the same scope. In this instance, a *contention* exists. All contentions are resolved by the priority setting. The system simply goes through the rules from highest to lowest priority and picks the first one who's scope expression (s) matches the object(s) being checked.

PCB Rules and Constraints Editor [mil]	
Manufacturing High Speed High Speed Seatallel Segment Length Matched Net Lengths Sigu Chain Stub Length Vias Under SMD Maximum Via Count Placement Room Definition Room Definition SRAM Free 1	Name DiffPair_MatchedLengths Comment Unique ID TRDYJPXN Where the First object matches
U_ELASH U_Bypass_Board U_Bypass_3V3 U_Bypass_2V5 U_Bypass_IV2 U_SRAM_Free U_SDRAM U_UMemory_CommonBus U_SPARTAN3 U_SPARTAN3 U_UPSU U_LEDS Component Clearance Component Clearance	Constraints Tolerance 1000mil Style 90 Degrees Amplitude 200mil
<u>R</u> ule Wizard <u>P</u> rioriti	es OK Cancel Apply

Figure 22. Double-clicking on any rule while in the PCB Rules and Constraint Editor dialog will bring up the specific query for that rule in the right pane.

All default design rules have a scope (Full Query) of ALL, meaning that they apply to the whole board.

In addition to scoping, there is also a user-defined priority setting (described below and seen in Figure 23). The combination of rule scoping and priority is very powerful and gives an unprecedented level of control that allows you to precisely target the design rules for your board.

If you do not want to use a design rule, but may want to use it in the future, rather than delete it, you can disable it. Toggle the corresponding Enable option for the rule in the relevant list.

Rules Priority

As you create a new rule in Altium Designer, it is automatically given a **Priority** setting. This setting defines the order in which multiple rules of the same type are applied when, for example, performing a DRC. Each new rule you add for the same rule type will be given the highest priority setting, i.e. 1. You can then change the priority order that exists for rules of the same type using the *Edit Rule Priorities* dialog which is accessed from the **Priorities** button in the *PCB Rules and Constraint Editor* dialog.

PCB Rules and Constraints Editor	r [mil]						? 🛛
	Name 🔼	Priority	Enabled	Туре	Category 🤇	Scope	Attributes
Room Definition	FPGA_U1_Manual	2	<u> </u>	Room Definition	Placement	InComponentPlass('F	PC Region (BR) = (14
	U_FPGA_U1_Auto	3	✓	Room Definition	Placement	InComponentClass("L	J_F Region (BR) = (15
FPGA_U1_Manual	U_WC_Boot	4	✓	Room Definition	Placement	InComponentClass("L	J_∖ Region (BR) = (14
U_FPGA_U1_Auto	U_WC_KB	5	~	Room Definition	Placement	InComponentClass("L	J_∖ Region (BR) = (50
U_WC_Boot	U_WC_LCD	6	✓	Room Definition	Placement	InComponentClass("L	J_∖ Region (BR) = (10
	U_WC_MODEM	1	 Image: A set of the set of the	Room Definition	Placement	InComponentClass("L	J_V Region (BR) = (50
	U_WC_PWR	7	✓	Room Definition	Placement	InComponentClass("L	J_V Region (BR) = (30
	U_WC_RS232	8	~	Room Definition	Placement	InComponentClass("L	J_V Region (BR) = (35
	U_WC_SENS	9	~	Room Definition	Placement	InComponentClass("L	J_V Region (BR) = (32
	U_WC_SRAM	10	~	Room Definition	Placement	InComponentClass("L	J_V Region (BR) = (17
	U WC VGA	11	 Image: A start of the start of	Room Definition	Placement	InComponentClass("L	J \ Region (BR) = (20
Component Orientations							
Permitted Lavers							
Nets to lanore							
Height	<						>
<u>R</u> ule Wizard	Priorities					DK Cancel	Apply

Figure 23. When you select on a root folder of category or type, you can see the Priority and Scope for each of the defined rules.

Initially the *Edit Rule Priorities* dialog will list all rule instances for that rule type that is currently selected in the *PCB Rules and Constraint Editor* dialog. Defined rules are listed in order of current priority – from 1 (highest) downwards.

E	dit Rule	e Priorit	ies	?	×
	<u>R</u> ule Type	e: Room	Definition		~
	Priority 1	Enabled	Name U WC MODEM	Scope Attributes InComponentClass('U Region (BR) = (50mil, 1050mil), (1525mil, 4050mil) Style - 1	Ke
	2 3		FPGA_U1_Manual U_FPGA_U1_Auto	InComponentClass('FF Region (BR) = (1450mil, 625mil), (2900mil, 1325mil) Style InComponentClass('U, Region (BR) = (1580mil, 1160mil), (2860mil, 2540mil) Style	- K 9 - I
	4 5		U_WC_Boot U_WC_KB	InComponentClass('U, Region (BR) = (1450mil, 25mil), (2850mil, 1025mil) Style - I InComponentClass('U, Region (BR) = (50mil, 3450mil), (3250mil, 4455mil) Style - I	Ke Ke
	6 7	✓ ✓	U_WC_LCD U_WC_PWR	InComponentClass('U, Region (BR) = (100mil, 3550mil), (4100mil, 6525mil) Style InComponentClass('U, Region (BR) = (3085mil, -200mil), (4125mil, 3850mil) Style	• K • K
	9 10	~	U_WC_RS232 U_WC_SENS	InComponentClass('U, Region (BR) = (350mil, 6100mil), (2025mil, 7625mil) Style - InComponentClass('U, Region (BR) = (325mil, -25mil), (1425mil, 1125mil) Style - K	·Κ (eε
	11	<	U_WC_VGA	InComponentClass(U, Region (BR) = (1750mil, 2550mil), (2550mil, 5550mil) Style	9-1 9-1
<	Increas	se Priority	Decrease Priority		

Figure 24. Select a rule entry and use the Increase Priority and Decrease Priority buttons to move rules up or down in priority order.

The PCB Editor allows you to easily export and import rule sets, enabling you to store and retrieve your favorite design rule configurations for the job at hand (discussed later).

Signal Integrity

Previously in PADS Layout, you were able to perform some signal integrity verification using the standard design rules checking system. Altium Designer offers in addition to the standard set of design rules for DRC, Signal Integrity analysis integrated directly into the PCB Editor (**Tools » Signal Integrity**). This includes pre-layout and post-layout Signal Integrity analysis capabilities that you can perform from either the Schematic or the PCB Editors, evaluate net screening results against predefined tests, perform reflection and crosstalk analysis on selected nets, and display waveforms.

Running Signal Integrity from a PCB project

When running a Signal Integrity analysis from a PCB document, the PCB must be part of a project along with the related schematics. Note that you could also run Signal Integrity from any of the schematic documents in the project and will have the same effect as running it from the PCB. This will allow both reflection and crosstalk analysis to be performed.

You can have some of the schematic components in the PCB but any that have been placed must be linked with Component Links. This can be checked by selecting **Project » Component Links**. Note also that any unrouted nets will use the Manhattan length between pins to calculate a track length estimate for analysis purposes.



A tutorial that covers the setting up of design parameters like design rules, and Signal Integrity models, starting up Signal Integrity from the SCH and PCB Editors, and configuring your tests further can be found in the tutorial *Performing Signal Integrity Analyses*.

PCB Layout and Design

With increasing component densities and faster signal speeds and transitions, successful board layouts today rely on design systems that unify the design definition with the physical layout and routing. Altium Designer offers such a PCB system, and like PADS Layout, includes a number of familiar features to help you place and route your board.

But unlike the PADS Layout environment, these capabilities are available in a less constrained way – smoothing your design process by peeling away design complexity and allowing you to navigate and manipulate your design easier. For example, you can place objects at anytime and start a route anywhere without ever having to switch modes. Many design and drafting commands that you are used to from PADS Layout are centralized from a single menu allowing you to focus completely on the job at hand. The PCB Editor environment of Altium Designer features innovative panels and dialogs efficiently designed for selection and editing of objects in large, dense designs.

PCB Editor Environment

When the PCB Editor is active (i.e. a PCB document (*.PcbDoc) is open and active) the main application window will contain:

- A main design window in which you can start designing, capable of display in both 2D and 3D
- Menus and toolbars that are specific to the PCB Editor
- Workspace panels that are both global and editor-specific.



Figure 25. Any object placement, routing, or graphical editing is carried out on the PCB document, which appears as a tab in the main design window.

Placing Design Objects

Design commands in PADS Layout are limited primarily to actions performed on design objects with respect to placement and routing. Many of the equivalent placement and routing commands in Altium Designer that you'll be interested in are located in the **Place** menu of the PCB Editor. They are not, however, context-sensitive for a particular mode as they are in PADS Layout. But whether you are placing arcs, circles, pads, via, components, polygon pours, or are interactively routing, it can all be done from this menu.

By comparison, the **Design** menu in Altium Designer has a different conceptual context and contains command more relevant to the actual design or design process as a whole. Design synchronization, rules, the Layer Stack Manager, Netlist, and Board Options are a few examples of the available commands.

Editing Design Objects

Design objects in Altium Designer must be selected first to be edited and there are a number of ways of doing this depending on your need. The Windows standard mouse-click shortcuts can be used – a familiar approach for PADS Layout users. This includes placing the cursor over and object and left-clicking to select one object. Holding the left-mouse button down and dragging a selection rectangle will select all the objects within an area. In addition to these standard selection methods, there is a new specialized dialog and panel designed specifically for selecting and editing multiple objects.

Find Similar Objects Dialog

To select many objects, including those spread out over a dense design, you can use the *Find Similar Objects* dialog (Figure 26). Right-click on one of the objects being edited and select **Find Similar Objects** from the right-click pop-up menu. Only documents which are open in the project are affected by any changes you make in this dialog.

Find Similar Objects		? 🛛
Kind		¥
Object Kind	Fill	Same 💌
Object Specific		Any
Layer	Bottom Layer	Same Different N
Net	No Net	Any K
Keepout		Any
Graphical		¥
X1	3755.907mil	Any
Y1	7157.479mil	Any
X2	3952.757mil	Any
Y2	7251.967mil	Any
Locked	✓	Any
Rotation	0.000	Any
Selected	✓	Any
✓ Zoom Matching ✓ S	Delect Matched V Clear Existing	
		Cancel

Figure 26: You can instruct to match target objects based on object attributes.

PCB Inspector Panel

Unlike anything you may have seen in PADS Layout, the **PCB Inspector** panel (Figure 27) displays the properties of whatever you have selected. This could be one object or many objects. The **PCB Inspector** panel enables you to navigate and edit the properties of one or more design objects in the active document. Used in conjunction with appropriate filtering, this panel can be used to make changes to multiple objects of the same kind from one convenient location.

The **PCB Inspector** panel has some handy qualities for everyday use. Unlike PADS Layout where you must open dialogs to edit, this panel can be visible all the time - much more efficient if you are making many reviews in your design. It can also display the common properties of *different* objects and let you edit them.

The panel is basically divided into two main regions:

- Filtering controls to define which objects are displayed in the panel (display scope).
- Sections of attributes for objects falling under the defined display scope.

PCB Ins	pector		▼ ×
Include	all types o	of objects	1
Ob	ject Kind	Fill	^
🗆 Obje	ct Specif	ic	
La	yer	MidLayer1	
Ne	et i	<>	
Ke	epout		
🗆 Grap	hical		
×1		<>	
Y1		<>	
×2		<>	
Y2		<>	
Lo	cked	✓	
Ro	tation	180.000	
		_	~

Figure 27. When you type a value into the PCB Inspector and press ENTER, the value of that property is changed for all selected objects. Selected objects can be of the same or differing type. Common properties that have the same value will show that value, otherwise the value will display <...>.

Various techniques for applying edits globally to multiple objects in your design in discussed in Editing Multiple Objects.

A comprehensive reference for placing and editing the various objects used to layout your PCB design is found in *PCB Editor and Object Reference*.

Setting Up the Workspace

A tutorial that covers all the basics of PCB design transfer, including the topics mentioned and much more can be found in *Getting Started with PCB Design*.

Getting your workspace set up after transferring your design is relatively straightforward. However, you should be aware that environment settings offer substantially more control compared to PADS Layout and have some differences in naming.

Environment settings which are global to all PCB documents in any editor are called *Preferences* while those that pertain to an individual PCB document are called *Board Options*. They are located in different menu locations. In PADS Layout, the *Options* dialog (which contains both global and some design level settings) is located under the **Tools** menu. In Altium Designer, the *Preferences* dialog is accesses from the **Tools** or **DXP** menus. Remember that these are only global settings. Document-specific settings and anything relevant to the design itself are located under the **Design** menu.

These settings are likely to be more comprehensive than you've seen before as they incorporate all document editors and all phases of electronic design. Having everything in one location and accessible in a tree-like navigation structure allows you to quickly and efficiently set system-wide preferences and gives you greater control over your working environment.

PCB Preferences – Global Settings

Altium Designer centralizes the setting of environment options across all document editors within a single context-sensitive and comprehensive dialog – the *Preferences* dialog (Figure 28). Accessible from **Tools » Preferences** [shortcut: **T**, **P**] like the *Options* dialog in PADS Layout, it features a tree-like navigation structure.

Some examples of system preferences that may be found here include those that assist in positioning components easier such as Online DRC, Snap to Center, and Selection preferences.

General	PCB Editor – 0	General				
Altium Web Update	Editing Options	<u>Autopan Optio</u>	ins			
Transparency		Stula	Adaptive	~		
Navigation		Jen	Loop			
	Shap To Center Smart Compone	ent Snap Speed	1200			
Projects Panel	Double Click Runs Inspector	 Pixels/S 	ec 🔷 Mils/Sec			
File Types	Remove Duplicates					
- Paulo Document Defaults		Space Navigab	or Ontions			
- 🚰 File Locking	Confirm Global Edit					
Participation Installed Libraries	Protect Locked Objects	Disable I	Roll			
Schematic	Confirm Selection Memory Clear					
I FPGA	Cish Classe Colorities	Polygon Repor	Jr			
Embedded System		Repour	Never	~		
PCB Editor	Shift Click To Select Primitives					
	Smart Track Ends	Threshold	5000			
- 🕮 Display						
- 🕮 Board Insight Display	Other	Eile Format Ch	ange Report			
Board Insight Modes		Disable.				
Board Insight Lens	Undo/Redo 30		opening the report from on	uer versions		
Interactive Routing	Rotation Step 90.000	Disable	opening the report from ne	ewer versions		
Mouse Wheel Configuration	Cursor Type Small 90	V	10 - 10 -			
Befaults		Paste from oth	ter applications			
SPCB Legacy 3D	Comp Drag none	Preferred F	ormat Metafile	*		
Reports	Metric Display Precision					
Berger Colors						
Models	Digits	Internal planes	5			
Text Editors		🗹 Enable i	Enable Multithreaded Plane Rebuilding			
CAM Editor	To edit this value please close all PCB	Enable this	Enable this option if your computer has multi core			
Production Manager	documents and PCB library documents. Chapging it requires restart of Altium	CPU, Rebui	lding split planes larger tha	n 4 square		
	Designer.	inches (~25 cores allowi	sq. cm) will utilize addition on process to finish faster	al CPU		
Wave			ing process to minist rester.			

Figure 28: Unlike PADS Layout which features a single tab in Options for global settings, changing any Preferences will affect all PCB documents you work on.

PCB Board Options – Document Settings

All options for the placement grid, measurement units, sheet position, and designator display are found in the *Board Options* dialog (Figure 29).

<u>M</u> easu	rement Unit	<u>E</u> lectrical	Grid	Sheet Position
Unit Snap (X Y Compo X	Imperial arid 5mil 5mil 5mil 1000 10		trical Grid a 10mil ap On All Layers ap To Board Outline id Lines 25mil	X 1000mil Y 1000mil Width 10000mil Height 8000mil
Y Design	25mil ator Display	Grid 2	1000mil	Lock Sheet Primitiv
Disp	lay Logical Designal	ors		
— Disp	lay Physical Design	ators		

Figure 29: For multi-channel designs, you can select between logical and physical designator display in the Board Options dialog.

With a PCB document active in the main design window (for this and all of the following context-sensitive dialogs), select **Design » Board Options** [shortcut: **D**, **O**] from the main menu to open the *Board Options* dialog.

Importing Your Design Rules

Like PADS Layout, Altium Designer also allows you to transfer your favorite design rules from another board. Design rules can be exported from, and imported to, the *PCB Rules and Constraints Editor* dialog (Figure 30).

🔊 РСВ	Rules and Constraints Edito	or [mil]						? 🗙
i i	Nam Dula	Name 🖉	Priority	Enabled	Туре	Category	Scope	Attributes
		🔪 🕕 ComponentClearand	:1	✓	Component Clearance	Placement	All - All	Clearance = 10mil
/		FPGA_U1_Manual	2	✓	Room Definition	Placement	InComponentClass('FPG	Region (BR) = (14
	Report	Height	1	✓	Height	Placement	All	Pref Height = 500
		U_FPGA_U1_Auto	3	✓	Room Definition	Placement	InComponentClass("U_F	Region (BR) = (15
	Export Rules	U_WC_Boot	4	✓	Room Definition	Placement	InComponentClass("U_\	Region (BR) = (14
	Import Rules	U_WC_KB	5	✓	Room Definition	Placement	InComponentClass("U_\	Region (BR) = (50
		U_WC_LCD	6	 Image: A set of the set of the	Room Definition	Placement	InComponentClass("U_\	Region (BR) = (10
		U_WC_MODEM	1	✓	Room Definition	Placement	InComponentClass("U_\	Region (BR) = (50
	II WE SENS	U_WC_PWR	7	✓	Room Definition	Placement	InComponentClass("U_\	Region (BR) = (30
		U_WC_RS232	8	✓	Room Definition	Placement	InComponentClass('U_\	Region (BR) = (35
		U_WC_SENS	9	✓	Room Definition	Placement	InComponentClass("U_\	Region (BR) = (32
	Component Clearance	U_WC_SRAM	10	~	Room Definition	Placement	InComponentClass("U_\	Region (BR) = (17
	Component Orientations	U_WC_VGA	11	✓	Room Definition	Placement	InComponentClass('U_\	Region (BR) = (20
	Permitted Layers							
	Nets to Ignore							
	🗄 🧻 Height 🛛 💌	<						>
	<u>B</u> ule Wizard	Priorities					OK Cancel	Apply

From the Knowledge Center in Help, links for videos on PCB Design and Layer Control in the PCB Editor can be found in the Documentation Library » Board Layout » Videos.

Figure 30. To import, select Import Rules from the pop-up menu. The Choose Design Rule Type dialog will open.

View Configurations (Layers and Colors)

View configurations are settings that control many PCB workspace display options for both 2D and 3D environments, and apply to the PCB and PCB Library Editors. The view configuration last used when saving any PCB document is also saved with the file. This enables it to be viewed on another instance of Altium Designer using its associated view configuration. View configurations can also be saved locally and be used and applied at any time to any PCB document. Any PCB files that you open which do not have an associated view configuration are displayed using a system default one.

Note: The *View Configurations* dialog provides access to 2D color settings for layers and other system-based color settings – these are *system settings*, that is, they will apply to all PCB documents and are not part of a view configuration. Color profiles for the 2D workspace can also be created and saved, similarly to view configurations, and can be applied at any time.

Select **Design** » **Board Layers & Colors** [shortcut: **L**] from the main menu to open the *View Configurations* dialog (Figure 35). This dialog enables you to define, edit, load and save view configurations. It has settings to control which layers to display, how to display common objects such as polygons, pads, tracks, strings etc, displaying net names and reference markers, transparent layers and single layer mode display, 3D surface opacity and colors and 3D body display.

You can apply view configurations using the *View Configurations* dialog or by selecting them directly from the drop-down list on the **PCB Standard** toolbar.



You can quickly navigate between the layers of your design by selecting the layer tabs at the bottom of the main design window. Helpful shortcut keys from the numeric keypad include the '+' and '-' for cycling through all visible layers, and the '*' to cycle through visible signal layers.

Layer Stack Manager

Layers are easily managed using the *Layer Stack Manager* dialog (Figure 31). Select **Design » Layer Stack Manager** [shortcut: **D**, **K**] from the main menu to open it. You can associate nets to planes, change the number of layers, define layer and substrate thickness and reassign electrical layer data in this dialog.

Although a different look and feel from the PADS Layout *Layers Setup* dialog, the *Layer Stack Manager* dialog offers much of the same functionality but in a more visual 3D format.



Figure 31: The Layer Stack Manager dialog shows a cross-section of the board as you design. Layers may be added or redefined in this dialog.

Two functional areas that you are accustomed to finding in the PADS Layout *Layers Setup* dialog are found in other places in Altium Designer that are more related to the specific area – enabling specific electric layers and defining the primary routing direction for layers.

For further information on setting up your board, refer to the tutorial Preparing the Board for Design Transfer

Enabling Specific Layers

Enabling or disabling layers for routing is treated as a rule in Altium Designer instead of an option for a layer. It is easily found in the *PCB Rules and Constraint Editor* dialog (Figure 32) under **Design » Rules**.

PCB Rules and Constraints Editor	[mil]	X
	Name RoutingLayers Comment Unique ID EFATYGVB Where the First object matches Image: Comment Full Query All Net Image: Comment Image: Comment All Net Class Image: Clayer Query Helper All Net and Layer Query Builder Image: Constraints Image: Constraints Constraints Image: Clayer Allow Routing Image: Clayer MidLayer1 Image: Clayer Image: Clayer Image: Clayer MidLayer4 Image: Clayer Image: Clayer Image: Clayer	
<u>R</u> ule Wizard	Priorities OK Cancel Apply	

Figure 32. Selecting the Routing rules from the PCB Rules and Constraint Editor dialog will allow you to set a constraint for enabling or disabling layers for routing.

Defining Layer Routing Direction

Routing direction for each enabled signal layer in the design is defined as part of the Situs Autorouter setup. A little more configuration is required to do this than you may have done in the past. First you must first ensure that there is a **Routing** Layers rule with a Query of AII (Figure 32). All enabled signal layers (as defined in the *Layer Stack Manager* dialog) will be

listed. Layer directions can then be defined in the *Layers Directions* dialog which is accessed by **Auto Route » Setup » Edit** Layer Direction (Figure 33).

Situs Routing Strategies		? 🗙
Routing Setup Report		
		<u>^</u>
Errors and Warnings - O	Errors 0 Warnings 1 Hint	
Hint: no <u>default SMDNeckD</u>	own rule exists.	
Report Contents		
Routing Widths		
Routing Via Styles		
Electrical Clearances		
Laver Directions	Layer Directions 🛛 🖓 🔛	
Drill Pairs	Layer Current Setting Actual Direction	
Net Topologies	Top Layer Horizontal Top Layer	
Net Layers	MidLayer1 Not Used A Disabled	
SMD Neckdown Rules	MidLayer4 Horizontal Disabled	×
Edit Layer Directions	Bottom Layer Any K Vertical	we Benort As
	2 O''Clock	
Routing Strategy	4 O''Clock 📉	
Available Bouting Strategies		
Name		
Cleanup		
Default 2 Layer Board		
Default 2 Layer With Edge Connecto		ectors
Default Multi Layer Board		
General Urthogonal		uia minimization
VIA MISEI	Strategy for fouring manager boards with aggressiv	e via minimization
Add Bemove	Edit Duplicate Lock All Pre-routes	
	Bip-up Violations After	Routing
		-
		K Cancel

Figure 33: Defining the primary routing direction for layers to suit the flow of connection lines. Situs uses topological mapping to define routing paths, so it is not constrained to route horizontally or vertically.

Should you wish to exclude a particular net (or class of nets) from being routed by the autorouter, simply define a Routing Layer rule targeting that net or net class and, in the Constraints region for that rule, ensure that the **Allow Routing** option for each enabled signal layer is disabled.



Situs Topological Router brings a new approach to autorouting. While it is straightforward to set up and run, there are certain points you should be aware of to produce optimal routing of your board. *Situs Autorouting Essentials* discusses these in more detail.

Interactive Routing

Like PADS Layout, Altium Designer also has specific modes for interactive routing. But unlike PADS Layout, modes for interactive routing are not dependent on licensing options, all are available in the PCB Editor and are not restricted to a mode.

The PCB Editor in Altium Designer is a connectivity-aware design environment. At all stages of routing your design, the software monitors and manages net list connectivity. Because the connectivity analyzer automatically monitors the completion status of the net you are routing,

From the Knowledge Center in Help, links for videos on Interactive and Differential Pair Routing can be found in the Documentation Library » Board Layout » PCB Routing.

you can route without regard to the arrangement of the from-tos. Once you complete a connection, the entire net is reanalyzed and connection lines are added and reoptimized as necessary.

The PCB Editor also features a sophisticated "look-ahead" feature that operates as you place tracks. The track segment that is connected to the cursor is called a *look-ahead* segment and is shown in outline/draft mode as you move the cursor. The segment between this look-ahead segment and the last-placed segment is the current track that you are placing (shown in final mode). Interactive routing modes are available in the **Place** and right-click menus.

Standard Interactive Routing Mode

Standard Interactive Routing can be started from **Place** » **Interactive Routing** and allows you to place down track segments to define a routing path. Similar to the basic Route Command in PADS Layout, it also monitors where you click and applies all applicable design rules and updates the connectivity as soon as you finish a route. Interactive routing shortcuts are shown in Table 3 at the end of this document.

You must have a signal layer active before you can begin routing. Display the layer that you would like to start on by enabling the **Show** checkbox for the layer in the *View Configurations* dialog [shortcut: L]. Once you are displaying the signal layer, the tab for it will display in the main design window. Click on the Layer tab at the bottom of the workspace to make it the current (active) layer, ready to route on.

Via On Layer Change

Press the * key on the numeric keypad to change to another signal layer while routing. A via will automatically be inserted, the properties of the via are determined by the applicable **Routing Via Style** design rule.



Line 45 End:Walkaround Obstacles [Width From: Rule Preferred] [Via-Size From: Rule Preferred]

Figure 34. Configure the interactive routing options in the Preferences dialog, or use the SHIFT + R shortcut and monitor the current mode on the Status bar.

Setting Up the Routing Layers

Routing layers, also referred to as signal layers, are set up in the *Layer Stack Manager* dialog (**Design » Layer Stack Manager**). Use the dialog controls to add layers and set their location in the layer stack.

The display of all layers, and the addition of mechanical layers, is controlled through the *View Configurations* dialog (**Design » Board Layers & Colors**).

Hale

View Configurations		K
Select PCB View Configuration	Board Layers And Colors Show / Hide View Options	1
Name Kind 2D 2D simple Altum 3D Blue 3D Altum 3D Brown 3D Altum 3D Dk Green 3D Altum 3D Lt Green 3D Altum 3D Fiel 3D Ben Purple Haze 3D Sample 1 3D	Signal Layers (S) Color Show Internal Planes (Color Show Mechanical Layers(M) Color Show Enable Single Linked To Layer BottomLayer (B) Image: Single Image: Single	
Path C:\Program Files\Altium Designer 6\Templates\2D .config_2dsimple	Only show layers in layer stack Only show planes in layer stack Only show enabled mechanical Layers All On All Off Used On All On All Off Used On	
Explore Folder Description Enter description of new view configuration	Mask Layers (A) Color Show Other Layers (D) Color Show System Colors (Y) Color Show Top Paste ✓ Drill Guide ✓ Connections and From Tos ✓ Bottom Paste ✓ Keep-Dut Layer ✓ DRC Error Markers ✓ ✓ Top Solder ✓ Drill Drawing ✓ Selections ✓ ✓ Bottom Solder ✓ Multi-Layer ✓ Visible Grid 1 ✓ ✓ All On All On All On All On All On All Of ✓ Yisible Grid 2 ✓ Via Holes ✓ ✓ Yisible Grid 2 ✓ ✓	
Actions Create new view configuration Save view configuration Save As view configuration Load view configuration Rename view configuration	Board Area Color Board Area Color Sitiscreen Laye Color Sheet Area Color Sheet Area Color Bottom Overlay (R) ✓ Workspace Start Color Alt On Alt On	
Remove view configuration 2D Color Profiles Layer Pairs	All Layers On All Layers Off Used Layers On Selected Layers On Selected Layers Off Clear All Layers OK Cancel Apply]

Figure 35. The display of all layers is controlled in the View Configurations dialog.

Interactive Routing Mode

Interactive Routing is a more intelligent interactive routing mode, working in a more intuitive way while attempting to completely route the chosen connection along the shortest path, comparable to the Dynamic Route Editor of PADS Layout. It can use horizontal, vertical, and diagonal segments while automatically walking around obstacles along the path. Interactive Routing can automatically complete the entire connection if both the start and end nodes are on the same layer, while maintaining any applicable design rules.

Select **Place** » **Interactive Routing** from the menus to start routing, or select the command from the right-click menu.



Figure 36. A set of connections being Smart Routed, each requiring just a single click to completely route that connection. Press the \sim key (tilde) to display the Interactive Routing shortcuts menu during routing.

Since Altium Designer's routing tool is interactive, you control the behavior using the cursor and the built-in shortcuts. It has a basic mode of operation where it will

	neip	F1	
	Edit Trace Properties	Tab	
	Suspend	Esc	
	Commit	Enter	
	Undo Commit	BkSp	
	Autocomplete Segments To Targ	et (Ctrl+Click)	
	Look Ahead Mode	1	
	Toggle Elbow Side	Space	
	Cycle Corner Style	Shift+Space	
	Toggle Routing Mode	Shift+R	
	Choose Favorite Width	Shift+W	
	Choose Favorite Via Size	Shift+V	
	Cycle Track-Width Source	3	
	Cycle Via-Size Source	4	
	Next Layer	Num +	
	Next Layer	Num *	
	Previous Layer	Num -	
	Switch Layer For Current Trace	L	
	Add Fanout Via and Suspend	1	
	Add Via (No Layer Change)	2	
	Next Routing Target	7	
	Swap To Opposite Route Point	9	
	Hug Mode	Shift+H	
	Add Accordions	Shift+A	
	Toggle Length Gauge	Shift+G	
-			

E1

attempt to route up to the current cursor location as you move the mouse around the workspace, without clicking to commit track segments.

Reaching the target end point, a click on the pad will complete the route.

Also available while interactive routing is auto-complete where it will attempt to seek out a path from the connection start point to the end point and attempt to route it. Use the shortcut, **CTRL+Click** on a pad or connection line to auto complete it or press the shortcut while in the middle of routing a connection, and the entire connection is routed! Interactive Routing shortcuts are shown in Table 3.

Routing a Differential Pair

Differential pairs are routed as a pair – that is, you route two nets simultaneously. To route a differential pair, select **Place** » **Differential Pair Routing** from the menus. You will be prompted to select one of the nets in the pair, click on either to start routing. Figure 39 shows a differential pair being routed. To make the connection lines for the pair easier to see, click on the pair in the **Differential Pairs Editor** (**PCB** panel). This will mask all other nets in the design.

Differential pairs are routed using Altium Designer's Smart Interactive Routing mode, which is described earlier in this document. Standard routing shortcuts remain, such as pressing the * key on the numeric keypad to switch to the next routing layer. During differential pair routing, the Smart Interactive Routing shortcuts are also available, as shown in Table 4.

But before you can route, differential pairs must be first defined.

Defining Differential Pairs on the Schematic

Differential pairs are defined on the schematic by placing a differential pair directive (**Place** » **Directive**) on each of the nets in the pair. The net pair must be named with net label suffixes of _N and _P. Placing a differential pair directive on each pair net applies a parameter to the net, which has a parameter Name of DifferentialPair and a Value of True.

Differential pair definitions are transferred to the PCB during design synchronization.

된		AA10			
Š		AA9			
ž	VIRAPAD 19	_AB10	V_RX1_N		Т
A	RXINPAD 19	AB9	V_RX1_P		
Ĕ	RAPPAD 19	~Y9	Loup		Т
-	GNDA19	AB8	V_TX1_P	<i>*</i>	
	TXPPAD19	AB7	V TX1 N	- 	Т
	TXNPAD19	AA7			╈
	VTIXPAD19	AA8			╈
	AVCCAUXTX19			- 1	+

Figure 37. Place directives on the schematic to define differential pairs.

Defining Differential Pairs on the PCB

Differential pairs should be defined on the schematic, however, differential pair objects can be defined in the PCB Editor.

To create a differential pair object, select **Differential Pairs Editor** mode in the **PCB** panel and click the **Add** button. From the resulting *Differential Pair* dialog (Figure 38), select existing nets for both the positive and negative nets, give the pair a name and click **OK**.



Figure 38: Create a pair on the PCB using the Differential Pair dialog.

You can also create a differential pair objects using net names conforming to a naming convention with a common prefix, followed by a consistent positive/negative suffix, for example, TX0_P and TX0_N. To do this, click the **Create From Nets** button in the **PCB** editor panel to open the *Create Differential Pairs From Nets* dialog. Use the filters at the top of the dialog to show net pairs, based on existing net names.



Figure 39: Both nets in the differential pair are routed simultaneously.

Viewing and Managing the Pairs

Differential pair definitions are viewed and managed in the PCB panel, set to Differential Pairs Editor.

Using the Differential Pair Wizard to Define the Rules

Click the **Rule Wizard** button in the **Differential Pairs Editor** (**PCB** panel) to walk you through the process of setting the required design rules. Note that the scope used for the created rules will depend on what was selected when the **Rule Wizard** button was clicked – if one pair was selected the rules will target the nets in that pair, but if a differential pair class was selected then the rules will target the nets and all pairs in that class.

Optimizing and Controlling Net and Differential Pair Lengths

Tuning and matching route lengths is a standard technique for maintaining data integrity in a high-speed digital system, and an essential ingredient of differential pair routing. **Interactive Length Tuning** and **Interactive Diff Pair Length Tuning** features (launched from the **Tools** menu) allow a dynamic means of optimizing and controlling net or differential pair lengths by allowing variable amplitude wave patterns to be inserted according to the available space, rules, and obstacles in your design. Length tuning properties can be based on design rules, properties of the net, or values you enter into a dialog (press **TAB** to open the dialog whilst interactively length tuning).

Once you have launched the command, click on the routed net or differential pair and move the mouse along it to add tuning segments. The interactive length tuning cursor provides you with information during the tuning process including before and current track lengths as well as a graphical representation to gauge how close you are to the ideal lengths. The yellow cursor bars indicate the possible minimum and maximum lengths. The green bar indicates the target length, as determined from the applicable Matched Length and Max Length design rules, or the settings in the *Interactive Length Tuning* dialog (Figure 40). The sliding indicator shows how close you are to achieving a match.

The interactive length tuning tools can be configured for:

- **Target Length** can be specified either according to design rules, another net, or manually. The **Clip to target length** checkbox will precisely clip mitered wave patterns to the target length.
- **Pattern** wave styles are mitered with lines, mitered with arcs, and rounded. You have control over amplitude, gap and dynamic amplitude increments. It is possible to have more than one pattern on a net.

While interactively length tuning you can vary any aspect of the length tuning parameters. Press the \sim key (tilde) during length tuning to display the available shortcuts, or refer to Table 5 at the end of this document.



Figure 40. Current length as well as valid length range is displayed dynamically using the gauge bar. Pressing TAB while routing will bring up the Interactive Length Tuning dialog where you can make changes as needed.

Project Outputs

A plot type, drill, silk screen, or routing, configured together with an associated output device setup is called the *CAM document* in PADS Layout. This is not unlike Altium Designer which also uses the same document concept but documents that are specific to output are called *OutJob files* instead.

In PADS Layout, output configurations are saved within the . PCB file so that each file will have its own documents list. You use the **Import** and **Export** functions to move this documents list, including the aperture list, drill feed and speed table between .PCB files. This is an important difference with Altium Designer which creates and stores them as separate files.

The **OutputJob Editor** allows you to define and manage Output Job Configuration files (*.OutJob). An Output Job file allows you to define all your design output configurations – assembly, fabrication, reports, net lists, etc. – exactly as required but all in a single and portable document. Through its portable nature, an Output Job file can be defined once and used in multiple and differing projects, allowing you to use your favorite configurations quickly and easily without the need to set the individual output again and again.

OutputJob Editor

You can create a new file of this type for any active project by using either the **File** » **New** » **Output Job File** (Figure 41) command or right-clicking on a project in the **Projects** panel and choosing **Add New to Project** » **Output Job File** from the pop-up menu that appears.

Default Fabrication Outputs.OutJob								
						1		
	Outp	uts						
Name A	Data Source	Supports	Output Description	Variant	Enabled		Publi	ish To PDF
🖃 🕞 Assembly Outputs							Adobe	(F9)
[Add New Assembly Output]								
🖃 🕞 Documentation Outputs								
🛃 Composite PCB Print	4 Port Serial Interfa	PCB	PCB Prints				Output M	ledia
[Add New Documentation Output]	pul							
🖃 🕞 Fabrication Outputs							Print	
🛃 Composite Drill Drawing	4 Port Serial Interfa	PCB	Composite Drill Drawing	9	· •			
🛃 Drill Drawing/Guides	4 Port Serial Interfa	PCB	Drill Drawing/Guides				POF	
📑 Final Artwork Prints	4 Port Serial Interfa	PCB	Final Artwork Prints				Publish	To PDF
🕮 Gerber Files	4 Port Serial Interfa	PCB	Gerber Files				Adobe	
NC Drill Files	4 Port Serial Interfa	PCB	NC Drill Files					
Power-Plane Prints	4 Port Serial Interfa	PCB	Power-Plane Prints		· •	-//	General	e Files
🛃 Solder/Paste Mask Prints	4 Port Serial Interfa	PCB	Solder/Paste Mask Pri	n	· •			
IIII Test Point Report	4 Port Serial Interfa	PCB	Test Point Report					
[Add New Fabrication Output]							[Add Ne ⊡ Modium	w Uutput
Crist Outputs							Medium	1
[Add New Netlist Output]								
E Report Outputs								
Bill of Materials	Project (Default)	Project	Bill of Materials	[No Variat				
[Add New Report Output]								

Figure 41. Fabrication output job file for the Multi-Channel Mixer project.

The Output Job file is divided into a number of categories that reflect the function of the output. These include Assembly, Documentation, Fabrication, Netlist, and Report Outputs. You'll want to familiarize yourself with how to configure for the output options that you require. It's worth mentioning how some basic functions such as generating output and auto-loading in the CAM Editor can be done in Altium Designer.

A comprehensive technical reference for setting up and configuring your output jobs through the OutputJobs Editor may be found in the *OutputJob Editor Reference*. You can also open this by pressing **F1** when the cursor is over an open OutputJob.

Generating Output

There are a number of steps involved in generating output. The first step is decide on your Output Medium (choose from File Generation, Publish to PDF or printing), the second step is to link up your outputs to your Output Medium and then lastly, generate your output relevant commands from the **Tools** menu or the button at the top of the Output Media column.

Auto-loading fabrication output into the CAM Editor

When generating Gerber, ODB++, NC Drill or IPC-356-D output, you can specify that one or more of these types of output to be automatically imported into a new CAM Editor document (*.CAM). This is performed using the *Output Job Options* dialog (Figure 42), accessed from the OutputJob Editor's **Tools** menu.

Enable the corresponding options for the outputs you wish to auto-load upon generation. Although you can enable one output type, e.g. Gerber, and run just the associated output generator, typically you would enable NC Drill, IPC-356-D and either Gerber or ODB++ and then run the associated output generators.

Output Job Options	? 🛛
CAMtastic auto-load options -	NC Drill Output IPC-356-D Output utoloaded into a new CAMtastic generation is performed.
Reset auto-load options af	ter generation
	OK Cancel

Figure 42: Configuring CAM Editor auto-load options.

Once these options are defined they will persist. This means that the next time you run the output generators, the resulting output would be loaded into another new CAM document. If you wish to be able to update just the existing CAM document, enable the **Reset auto-load options after generation** option. This results in the clearance (disabling) of all auto-load options after the initial generation. You can then gain access to the CAM Editor's **Rescan** and **Reload** commands (from the **CAM** panel), which perform time-stamp comparison of generated and existing (imported) files and loading of data into existing layers respectively.

Documenting with Smart PDF

Smart PDF is a built-in PDF generation wizard that quickly generates a PDF of a single schematic sheet, drawings of the PCB, or all the schematics and PCB in a project, complete with clickable bookmarks to each component, net and pin in your design.



Figure 43: Use Smart PDF to generate live, bookmarked PDFs of your designs, ideal for design reviews and product documentation.

The Altium Designer Smart PDF wizard (Figure 43) is launched from the **File** menu, and will guide you through the steps required to export a design to PDF.

Library and Component Management

Altium Designer supports working directly from the source symbol or model libraries, an ideal approach when the schematic and PCB are designed by separate organizations. There are also *integrated* libraries, a concept that will be new for PADS Layout users. All libraries may be viewed and managed at any time from the **Projects** and **Library** panels.

Altium Designer Libraries

An integrated library in Altium Designer is one where the source symbol, footprint, and all other information (e.g. SPICE and other model files) are compiled into a single file. During compilation checks are made to see how relationships are defined, to validate the relationship between the models and the symbols and to bundle them into a single integrated library. This file can not be directly edited after compilation, offering portability and security.

All of Altium Designer's 70,000+ components are supplied in integrated libraries, from which the source libraries can be extracted at any time if required.

PADS Object	Altium Designer Object	Comments
Decal	Footprint	Graphical representation of the shape defined for the component to mount onto the PCB. This is 2-dimensional representation only, and can be quite different from the actual component itself
Part	Part/Component	The term Part is used only as part of the design capture (schematic) process in Altium Designer. Once <i>placed</i> as a footprint into a PCB file, it is given a designator and value (comment) and becomes a component.
Lines	Lines	Primitive object used for graphical information.
CAE Decal	Schematic symbol	The graphical representation of a schematic part, such as a NOR gate.

Table 2. A table of the more commonly-used PADS Library terms and their closest respective Altium Designer equivalents.

Library Types

There are four types of libraries used in the Altium Designer environment: model, schematic, integrated and database.

Model

These libraries contain the models for each component representation as per their design domain and are each stored in their respective "model containers", called model libraries. In some domains, there will be typically one model per file and they are referred to as model files (*.mdl, *.ckt). In other design domains, models are usually grouped into library files according to how the user has grouped them such as PCB footprints grouped into package-type libraries (*.PcbLib).

Schematic

These libraries contain source schematic components and their model interface definitions (*.SchLib).

Integrated

From the Knowledge Center in Help, links for videos on Library Editing and component models as well as other articles on components in Altium Designer can be found in the Documentation Library » Library and Component Management.

An integrated library (*.IntLib) is a compiled file, that includes schematic libraries along with all models referenced in the symbols' model interface definitions; which could include footprint model libraries simulation model files and 3D model libraries. This is unlike PADS library fi

footprint model libraries, simulation model files and 3D model libraries. This is unlike PADS library files where different part information is stored in different types of files.

Database

Database libraries provide similar functionality to the OrCAD Capture CIS. When you place from an installed database library (*.DBLib) all data in the component comes from the referenced database.

Where are my libraries? Some Basics on Library Management

You'll be able to view your source schematic and PCB library files immediately after translation through the **Projects** panel. Your translated PADS libraries are automatically grouped into one PCB project.

Libraries are installed (added) to the Altium Designer environment, making their components available in all open projects. Display the **Libraries** panel, from there you can install and remove libraries. Libraries can also be linked to any project, and you can also define project search paths, useful for referencing simulation models.

Refer to the article *Enhanced Library Management Using Integrated Libraries* for a further discussion on using Integrated Libraries.

A Brief Note on Database Linking

Appreciating the fact that many designers like to link from the components in their electronic design software to their company database, Altium Designer has strong support for linking and transferring database data through the design process and into the Bill of Materials.

Two techniques are supported, one where the Altium Designer library symbol holds all model references and also includes links into an external database, the second where the database holds all model references and other company information. While database connections in Altium Designer are set up for MS Access databases (*.mdb files) by default, any ODBC-compliant database can be accessed, offering the same flexibility you previously had with OrCAD.

To learn more about linking from Altium Designer components to an external database, refer to the application note *Linking Existing Components to Your Company Database*.

For information on placing components directly from a company component database, read the application note *Using Components Directly from Your Company Database*.

Interactive Routing Shortcuts

~ (tilde)	Display list of shortcuts
CTRL + Click	Auto-complete segments to target
BACKSPACE	Remove last segment
ESC	Terminate current trace
SHIFT + A	Add accordion sections (interactive length tuning)
SHIFT + C	Toggle auto-complete
SHIFT + G	Toggle length tuning gauge
SHIFT + H	Toggle Hug mode
SHIFT + O	Toggle visible routing area
SHIFT + P	Toggle Push mode
SHIFT + Q	Toggle glossing
SHIFT + R	Toggle routing mode
SHIFT + S	Switch layer for current trace
SHIFT + V	Select favorite via size
SHIFT + W	Open Choose Favorite Width dialog.
, (comma)	Decrease arc setback
SHIFT + . (comma)	Decrease arc setback 10x
. (full stop / period)	Increase arc setback
SHIFT + . (full stop / period)	Increase arc setback 10x
ENTER	Place Segment
+ (plus)	Next Layer (numeric keypad)
- (minus)	Previous Layer (numeric keypad)
* (multiply)	Next Signal Layer (numeric keypad)
SPACEBAR	Cycle corner direction
SHIFT + SPACEBAR	Cycle corner styles (if restrict to 90/45° is not enabled)
ТАВ	Edit trace properties
1	Toggle Look-ahead Mode – Switches between 1 and 2 segment placement mode
2	Add via, no layer change
SHIFT + 2	Add fanout via, tool immediately waits for next fanout to route and via to place
3	Cycle track width source
4	Cycle via size source
6	Force walk-around (with key pressed)
7	Switch leader trace or switch routing target in single trace mode

8	Toggle dynamic routing mode
9	Switches to opposite routing point

Table 3. Interactive Routing shortcut keys.

Interactive Differential Pair Routing Shortcuts

~ (tilde)	Display list of shortcuts
CTRL + Click	Commit auto complete segments (if applicable)
BACKSPACE	Remove last segment
SHIFT + BACKSPACE	Remove last cluster of segments
ESC	Terminate current trace
SHIFT + R	Toggle routing mode
SHIFT + W	Open Choose Favorite Width dialog.
ENTER	Place segment
+ (plus)	Next layer
- (minus)	Previous layer
* (multiply)	Next signal layer
SPACEBAR	Toggle corner direction
SHIFT + SPACEBAR	Cycle corner styles (if restrict to 90/45° is not enabled)
ТАВ	Edit trace properties
3	Cycle track width source
4	Cycle via size source
5	Toggle Auto-complete
6	Change via mode
7	Switch leader trace (diff pair) or switch routing target

Table 4. Interactive Differential Pair Routing shortcut keys.

Interactive Length Tuning Shortcuts

~ (tilde)	Display list of shortcuts
ТАВ	Edit tuning pattern settings
BACKSPACE	Remove last segment
SPACEBAR	Next tuning pattern
SHIFT + SPACEBAR	Previous tuning pattern
SHIFT + R	Toggle Routing Mode
, (comma)	Decrease pattern amplitude by one increment

Increase pattern amplitude by one increment
Decrease miter or radius
Increase miter or radius
Decrease pattern gap by increment
Increase pattern gap by increment
Toggle amplitude direction

Table 5. Interactive Length Tuning shortcut keys.

For Further Reference

Below are references to other articles and tutorials in the Altium Designer Documentation Library that talk more about the conceptual information as well as walking you through specific tasks. Remember, you can also browse through the Help contents, and use **F1** and **What's This** at any time in a dialog for more details.

For more FPGA project options, refer to the tutorial, Getting Started with FPGA Design.

An article that looks at some of the feature highlights of Altium Designer's CAM Editor, including ODB++ import and export, advanced panelization and direct export into Altium Designer's PCB Editor may be found in *CAM Editor Feature Highlights*.

For an overview of Altium Designer's FPGA design, development and debugging capabilities, read *An Introduction to Embedded Intelligence*.

For getting started with embedded software, refer to Getting Started with Embedded Software.

Revision History

Date	Version No.	Revision
10-Jan-2007	1.0	New document release
02-Jul-2007	1.1	Content reviewed and updated
9-Nov-2007	1.2	Added interactive length tuning and changes to diff pair routing for 6.8
7-Jan-2008	1.3	Updated view configurations info, added dialog units toggle images.
11-Feb-2008	1.4	Component body references changed to 3D body.
15-May-2008	1.5	Converted to A4 and reference to 'FPGA Designer's Quickstart Guide' replaced with reference to 'An Introduction to Embedded Intelligence'.
21-Jul-2008	1.6	Updated the sections on Interactive Routing and also the Output Job Editor
8-Sep-2008	1.7	Updated for Summer 08.
16-Mar-2011	-	Updated template.

Software, hardware, documentation and related materials:

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