HOW SMALL PCB DESIGN TEAMS CAN SOLVE HIGH-SPEED DESIGN CHALLENGES WITH DESIGN RULE CHECKING

MENTOR GRAPHICS

WHITEPAPER

HIGH SPEED DESIGN

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INTRODUCTION

Coping with SI (signal integrity) and EMI (electromagnetic interfaces) related issues is a daily challenge for PCB design engineers and small teams. To identify and resolve layout challenges during the PCB design process, many engineers rely on sophisticated rule-based checking. By using design rule checks (DRCs), you can avoid end-product problems such as emissions testing failures or signal-integrity-related failures.

This paper reviews the common causes of SI/EMC challenges and shows how they can be easily identified using eight advanced design rules, saving you time and costs.

ELECTROMAGNETIC INTERFERENCE

Electromagnetic interference, or EMI, is a disturbance that could degrade the performance of an electrical circuit, thus preventing it from functioning correctly or not functioning at all. EMI on PCBs is caused by unintended radiation from circuit elements, such as traces, vias, and connectors. High-speed PCB designs are more vulnerable to EMI problems if not designed to properly suppress unwanted radiation.

COMMON CAUSES OF EMI IN PCBs

Here are a few causes of EMI problems and how they can be avoided in PCB designs.

INTERRUPTED RETURN PATH

An interrupted return path is very common, and can be an unintentional source of EMI issues (Figure 1).

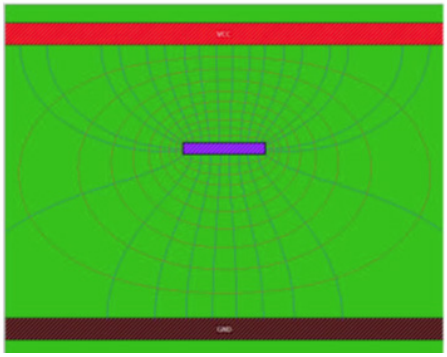

Figure 1: Interrupted return path

At high frequencies, a signal traveling along a trace traverses electromagnetic fields that are coupled through the trace into the nearest plane (also known as reference planes). These can act as current return paths and form a closed current path. If this closed current path is interrupted or broken, radiation occurs, causing EMI issues.

Typical examples of interrupted return-path cases include nets crossing gaps, a net near a plane edge, and reference plane changes.

NET CROSSING A GAP

Also known as trace-crossing or signal-crossing splits, a net crossing a gap occurs when a trace return path, e.g. on its reference planes, is a split that causes an interruption in the return path (Figure 2). The split could be a "hole" on a single plane, or a gap between two power islands.

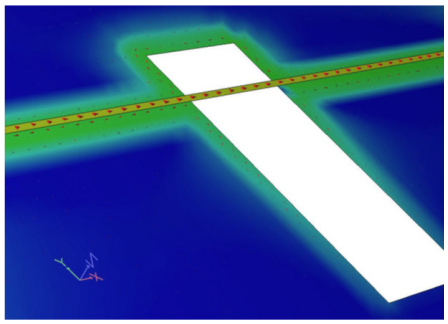

Figure 2: A net crossing a gap.

Ideally, all high-speed signals should be referenced to solid ground planes. But if a split happens, a stitching capacitor should be used to form an AC path through the gap.

NET NEAR A PLANE EDGE

If a high-speed signal trace is routed near its reference plane's edge, the electromagnetic field will wrap around the edge and radiate some energy.

Common instances of this radiation occurring are when a trace is routed too close to the edge of a board (Figure 3), and when a trace is routed too close to a large void on the reference plane (Figure 4).

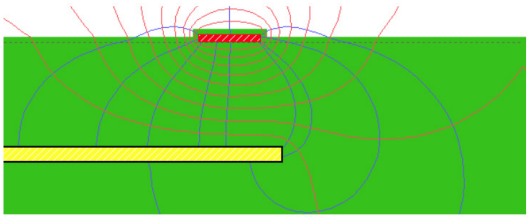

Figure 3: A trace routed too close to the edge of the board can produce EMI.

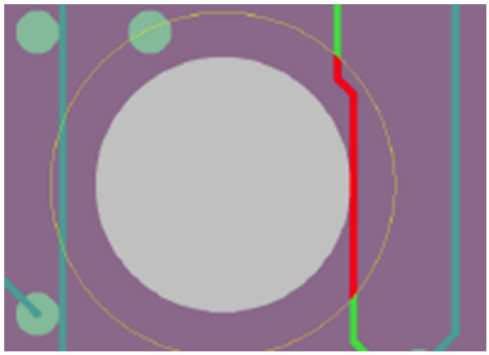

Figure 4: A trace routed near a large void on the reference plane can produce unwanted EMI.

REFERENCE PLANE CHANGE

When a signal is routed from one layer to another layer through a via, it can result in the signal's return path changing, making the closed current path even more complicated. In Figure 5, the current flowing on the traces of different layers couples (or references) to different planes. The return current on these reference planes needs to be continuous as well; otherwise, the whole current loop is interrupted or broken, producing EMI issues.

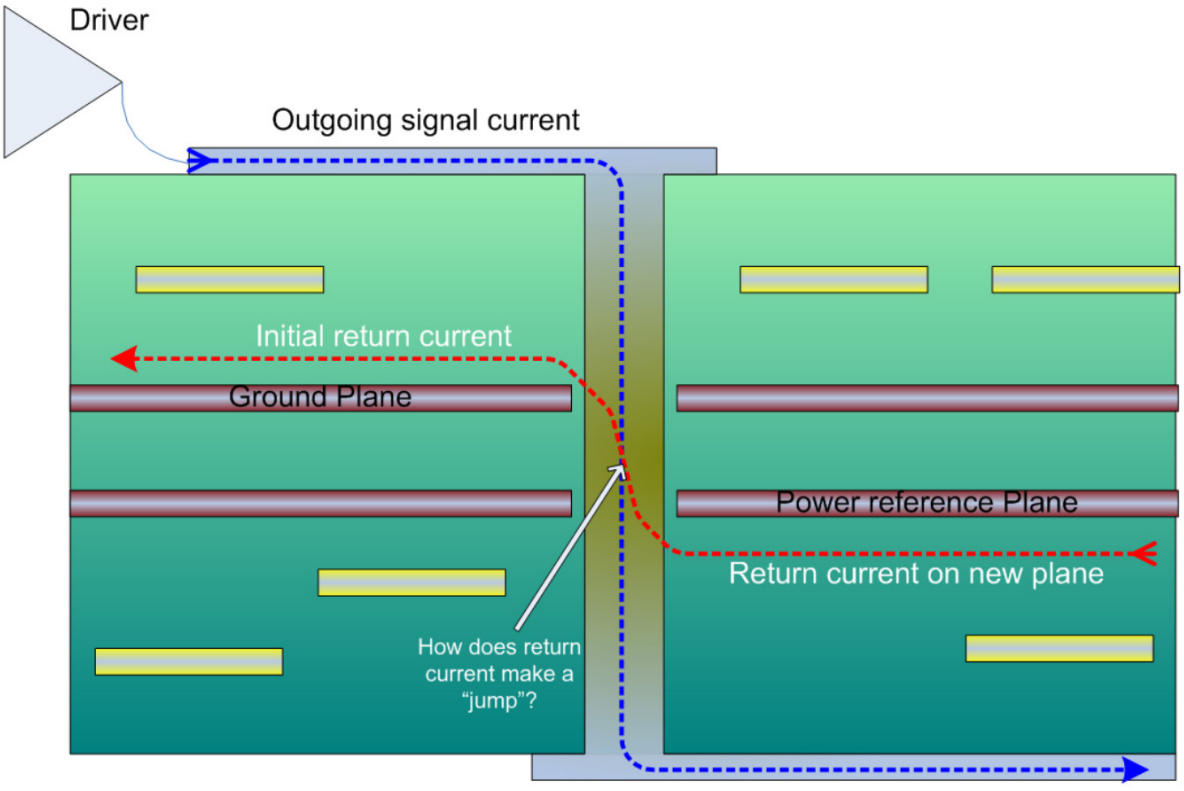

Figure 5: Unintended current flow, and unintended EMI, can result from a signal path that changes reference planes.

To ensure a closed current path, you must provide a continuous path for the return current:

- If the reference plane changes from power to ground, one or more stitching capacitors is required
- If the reference plane changes between grounds (or same-voltage planes), one or more stitching vias is required

ISOLATED METAL AREAS

Isolated metal areas are usually unwanted and, when left in a PCB design, they commonly act as unintentional sources, causing EMI issues.

VIA STUB

A via stub is a via, or a portion of a via, that has had its pad removed and is not connected to any layer, thus keeping it from being in series with a signal flow (Figure 6). However, if the via stub is drilled and plated during the manufacturing process, an isolated metal area is formed. In a high-speed design, a long via stub can act as an antenna and emit energy.

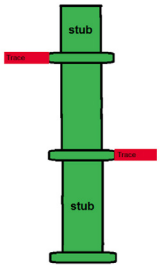

Figure 6: A via stub.

METAL ISLAND

A metal island is an isolated, floating metal area on a board that can act like an antenna and radiate energy, causing EMI issues. The metal island should be properly connected with vias at both ends, as shown in Figure 7, to avoid radiation.

Figure 7: A metal island needs vias at both ends.

COMMON CAUSES OF SIGNAL INTEGRITY ISSUES IN PCBS

Here are a few causes of SI problems and how they can be avoided in PCB designs.

CROSS-TALK COUPLING

Signals that are routed close to each other will couple energy on edge transitions. Dense boards unavoidably have areas where signals are routed with minimum trace-to-trace spacing. The longer the traces are routed next to each other, the greater the magnitude of coupling. Increasing the spacing between these tightly coupled traces during the layout clean-up phase will minimize the amount of cross-talk (Figure 8).

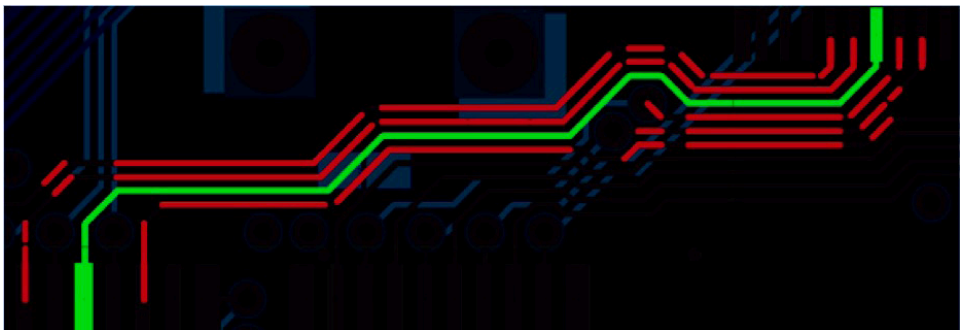

Figure 8: Densely routed traces can lead to cross-talk.

DIFFERENTIAL IMPEDANCE

Differential pairs maintain their characteristic impedance only if the trace-to-trace spacing is maintained along the route. Sometimes during layout, either due to break-out rules or inadvertently, the trace-to-trace spacing between differential pairs can change. If this occurs, the impedance of the differential pair will change instantly at the point of variation, causing unwanted signal reflections. Additionally, differential pairs with mismatched lengths will introduce skew at the receiver and can make the signals susceptible to unwanted EMI (Figure 9).

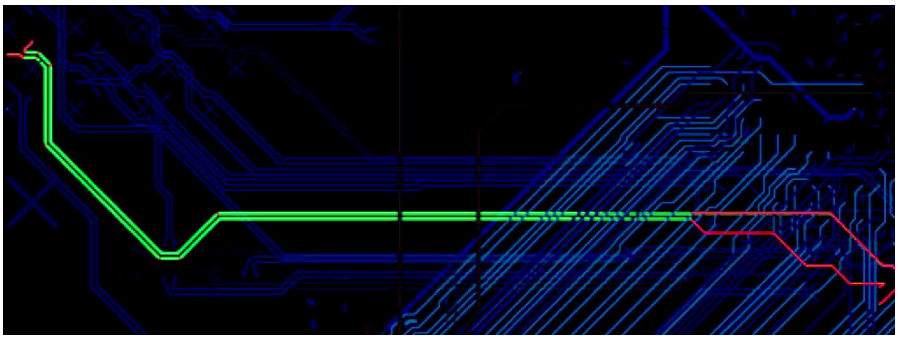

Figure 9: A differential pair that does not maintain trace-to-trace spacing along its route.

IMPEDANCE (SINGLE-ENDED)

By nature, every trace in a PCB design has a characteristic impedance (Zo). By controlling the width of the trace, the thickness, and its spacing between a plane layer or layers, the trace can be engineered to maintain a specific impedance value. The predominant approaches used to create controlled-impedance traces are microstrip (Figure 10) and stripline (Figure 11). If any of the key parameters (e.g., trace thickness, width, or spacing) to plane layer(s) varies along the route, the impedance will change. This can result in unwanted reflections and other SI effects.

$$Z_o \approx \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{0.8W + T}\right]$$

(Valid when 0.1<W/H<2.0 and 1< ε_r <15)

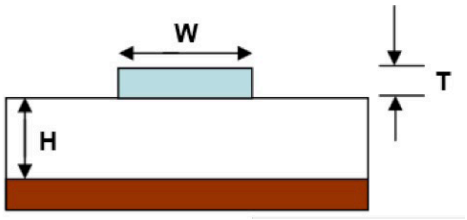

Figure 10: In a microstrip trace configuration, the key parameters are trace width, thickness, and spacing to plane layer.

$$Z_{o_{stripline}} \approx \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4H}{0.67\pi(T + 0.8W)}\right]$$

(Valid when W/H<0.35 and T/H<0.25)

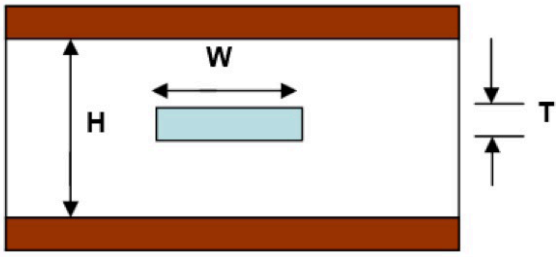

Figure 11: In a microstrip trace configuration, the key parameters are trace width, thickness, and spacing to plane layer.

LONG STUBS

In a PCB layout, a single net often connects multiple ICs. For example, an address bit on a memory interface can originate from the controller and connect to many different memory devices. The sections of copper that branch from the main trace and connect to the load are called stubs. If the stub is too long, it can cause unwanted signal reflections.

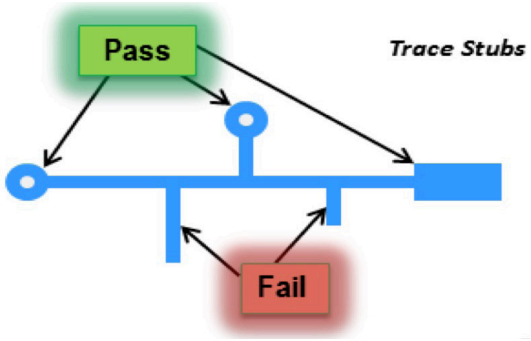

Figure 12: Examples of stubs that can be too long and cause SI issues.

MANY VIAS

Often, a trace will need to switch layers in order to complete a route successfully. Each time the trace transitions to a different layer, the signal travels through a via. Vias can degrade a signal or cause unwanted reflections because they impose an impedance discontinuity and can attenuate the signal. Fast edge rates, along with a large number of vias on a trace, can result in large SI- and EMI-related concerns.

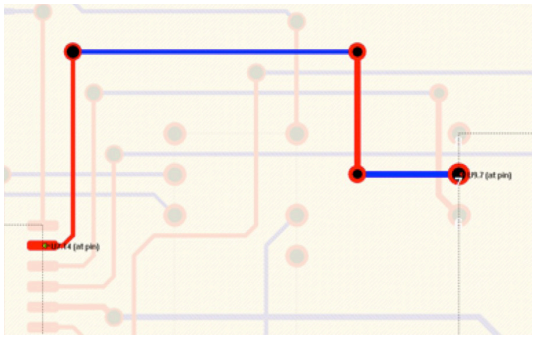

Figure 13: A trace with several vias should be further analyzed to avoid SI and EMI problems.

PADS HYPERLYNX DRC

Known radiation sources can be mitigated through careful board design, for example, by minimizing the number of vias on a trace route. But human error can leave known sources untreated, leading to failure. Identifying these sources requires knowledge, patience, time, intense labor, and… no human errors.

In addition, many SI/EMI problems are caused by unknown or unintentional sources, such as interrupted signal return paths, floating metal islands, etc. There could be dozens, hundreds, or even thousands of these sources, making it impractical to find them manually.

PADS® HyperLynx® DRC is an electrical design rule checker that reviews layout designs effectively and efficiently for electrical performance. With PADS HyperLynx DRC, potential EMI issues on PCB boards are identified automatically, preventing failure and reducing costs. By automating the inspection process, PADS HyperLynx DRC eliminates the errors that can be generated by manual inspection, reducing hours or even days of work to just minutes. Accurate and informative results enable problem examination and design corrections.

In short, PADS HyperLynx DRC is an excellent way to capture and preserve design knowledge and consolidate checks done by multiple disciplines into a single, comprehensive set of checks. All DRCs are repeatable and reusable for future designs, dramatically reducing verification time.

RULES INCLUDED IN PADS HYPERLYNX DRC

PADS HyperLynx DRC helps identify the issues described in this paper by checking the following eight signal-integrity and EMI-related DRC rules:

- SI rules: metal islands, net crossing a gap, and vertical reference plane change.
- EMI rules: crosstalk coupling, differential impedance, single-ended impedance, long stubs, and many vias.

These rules are parameterized and customizable so that violation conditions can be modified between designs to meet specific requirements. Rules can also be applied to a portion of the design, such as to critical or more vulnerable parts. For example, rules that look for changes in vertical reference planes can be run for all clocks of a DDR3 interface to ensure closed current paths.

Each rule is documented with its purpose, parameter explanations, and violation conditions. Rule documents can be viewed directly in the PADS HyperLynx DRC user interface (Figure 14).

PERFORMING CHECKS

Running SI and EMI checks in PADS HyperLynx DRC is a simple five-step process:

1. **Load layout design:** From the PADS layout environment, click 'Analysis' to load your design into PADS HyperLynx DRC.
2. **Prepare the data for cheking:** Categorize critical or vulnerable parts of your design into groups so that the necessary rules can be set up and applied.
3. **Set up DRC rules and their parameters:** Apply your rules to the entire design or to a portion of it. If desired, you can run a rule with multiple instances and run each instance on a different portion of design with different requirements.
4. **Run DRCs:** Depending on the number of checks and the complexity of your design, a complete EMI board check will take only a few minutes, to less than an hour, to run.
5. **Examine results and violations:** Examine violations inside the board viewer, prioritize them as appropriate, and share them with others via violation reports..

PADS HYPERLYNX DRC RULE EXAMPLE – NET CROSSING A GAP

The Net Crossing Gap rule, as documented below in PADS HyperLynx DRC, helps identify one of the interrupted return-path cases (Figure 14).

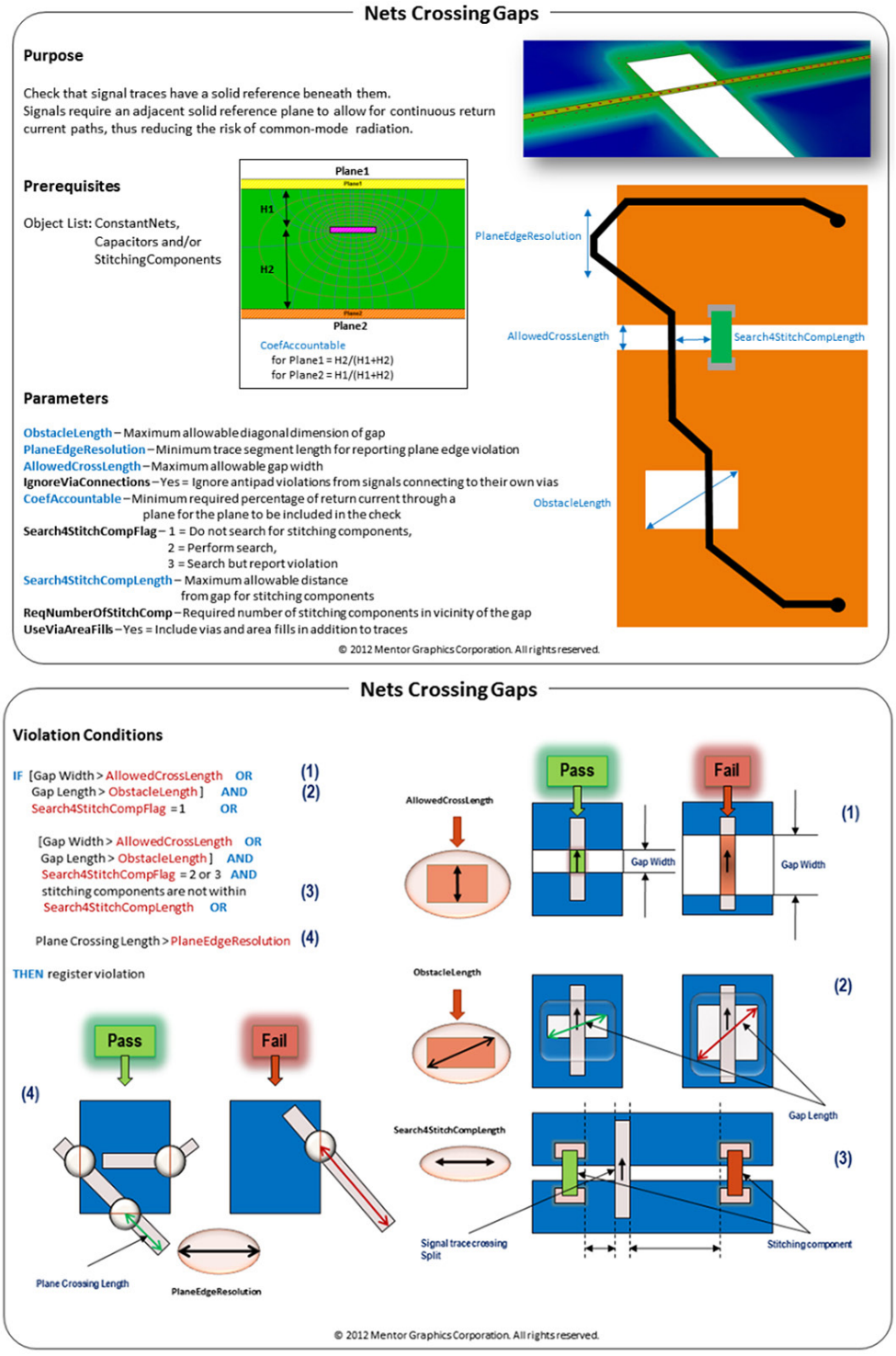

Figure 14: Unlike many tools, the documentation for PADS HyperLynx DRC provides detailed explanations of each rule.

The Net Crossing Gap rule can be applied to the entire board, or to a particular portion of interest. Figure 15 shows an example of four violations that were detected on the DDR2 clocks of a design.

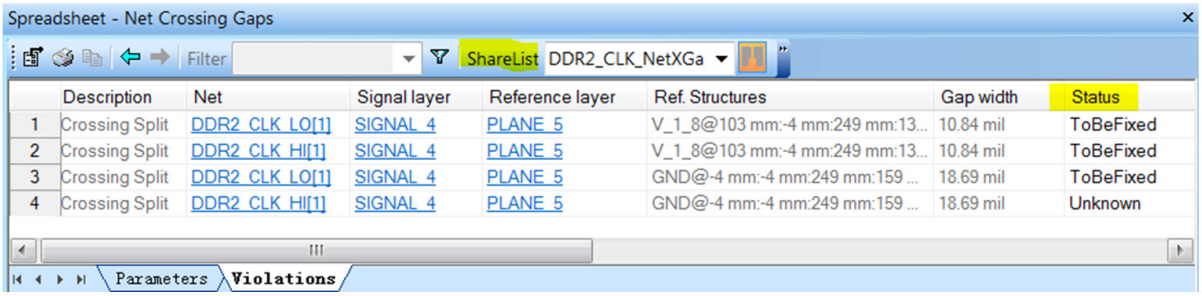

Figure 15: Here, PADS HyperLynx DRC displays four EMI violations that it discovered affecting DDR2 clock signals.

When a violation is selected from the table, its location will be highlighted in the board viewer (Figure 16). Further actions and information can be found in the Details viewer (Figure 17).

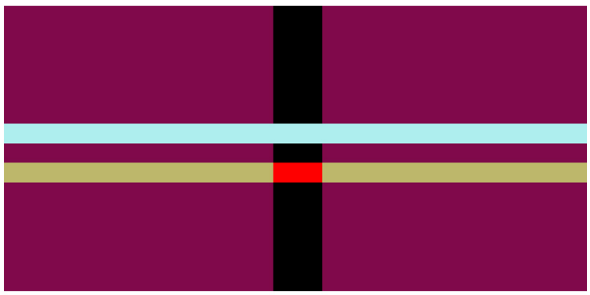

Figure 16: The violation is identified on the board viewer.

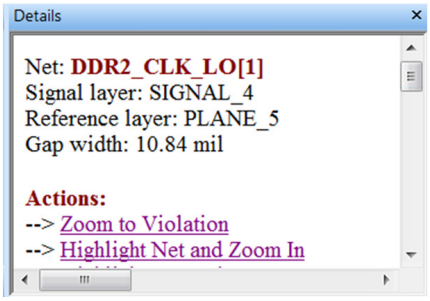

Figure 17: More details can be found in the Details viewer box.

After further examination, the status of violations can be updated and the selected violations can be added to a 'share' list that can be exported to an HTML report file. The report includes pictures of the violations that make it easy for team members to interpret.

SUMMARY

EMI and SI issues occur commonly in modern designs, especially in the high-speed design field. Some of the issues are caused by known sources and can be avoided through careful PCB design. Many SI/EMI issues, however, are caused by unintentional sources or by human error, making them difficult to find in a manual review process. PADS HyperLynx DRC easily identifies EMI and SI issues using the eight design rule checks discussed in this paper, thereby helping you improve design quality and avoid costly failures.

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