Printed Circuit Design Tutorial

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Gold Phoenix has been sale PCB board in North America since 2003, during these years we received a lot of questions from different customers about PCB designs, and customers also make some common mistakes. Finally we think that it is better to write a tutorials to cover some basic rules, tips, techniques in PCB designs. Hope this tutorial can help our customer to improve their PCB design skills.

There is three sections in this paper, 1) Basic rules in PCB design, 2) Explain some basic technology in PCB manufacture 3) Prepare the files for PCB house.

I. Basic rules in PCB Design

When you first begin to design PCB you need to setup some rules

A. The size and shape of the PCB:

The best way to define the size and shape of the PCB is use mechanical layers as shown in Fig 1. The inner cuts can also be defined on the mechanical layers, just make sure when you generate the Gerber files “SELECT THE mechanical layers”, otherwise your gerber files will not have border.

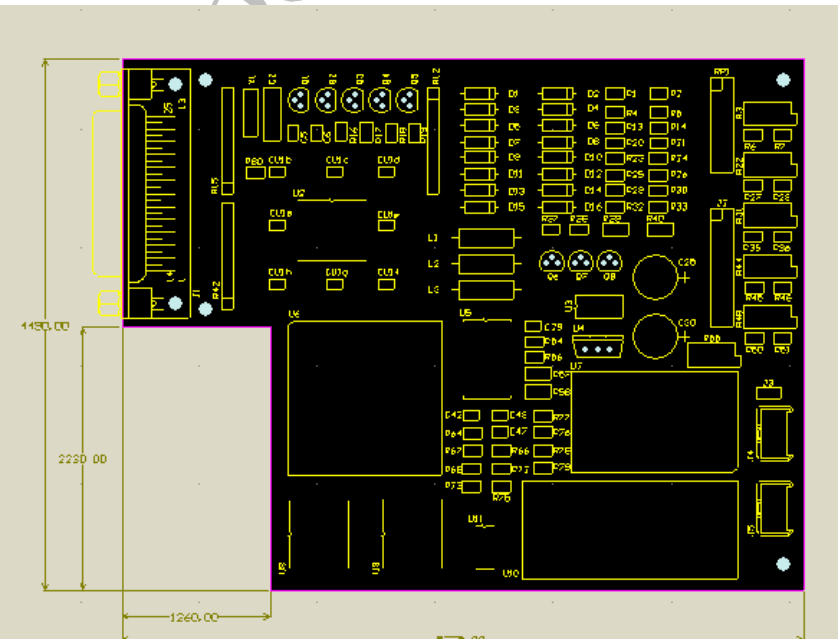

Fig 1 Border of the PCB

You can also draw the border on the silk screen layer, but if you have inner cut then you need to be careful. If you draw the inner cuts on the silk layer that will be very confuse for us. Since we will consider it is a “text” symbol. In this case what you can do is shown in Fig 2, put text “CUT OUT” in the silk box.

But define the PCB shape on the mechanical layer is till the “professional way”. The outline tolerance by routing is +/-6mil.

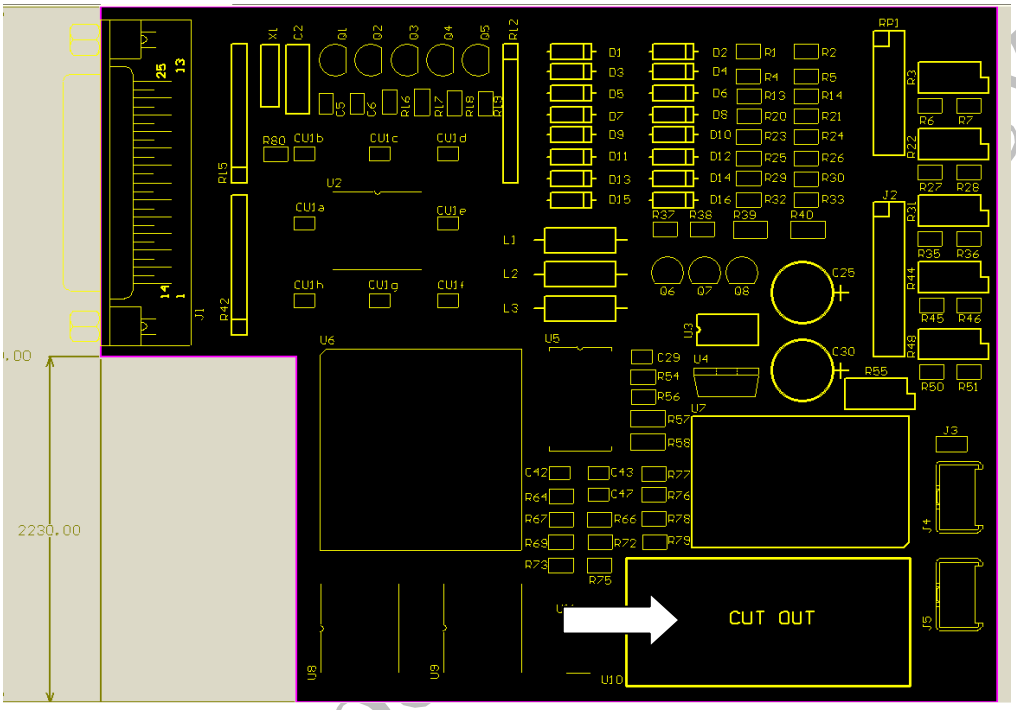

Fig 2 Define cut out in silk layer

B. Define the design rules for the PCB

After define the PCB shape the next step is to define the design rules. Most of the PCB software can define those design rules before the PCB layout, then you can make sure the PCB is designed in the right specification.

1) Min clearance& Min hole size

Min clearance means space between different networks. Usually if you want design a low cost PCB setup the clearance 7mil-10mil, and we suggest>=10mil. One example is shown in Fig 3

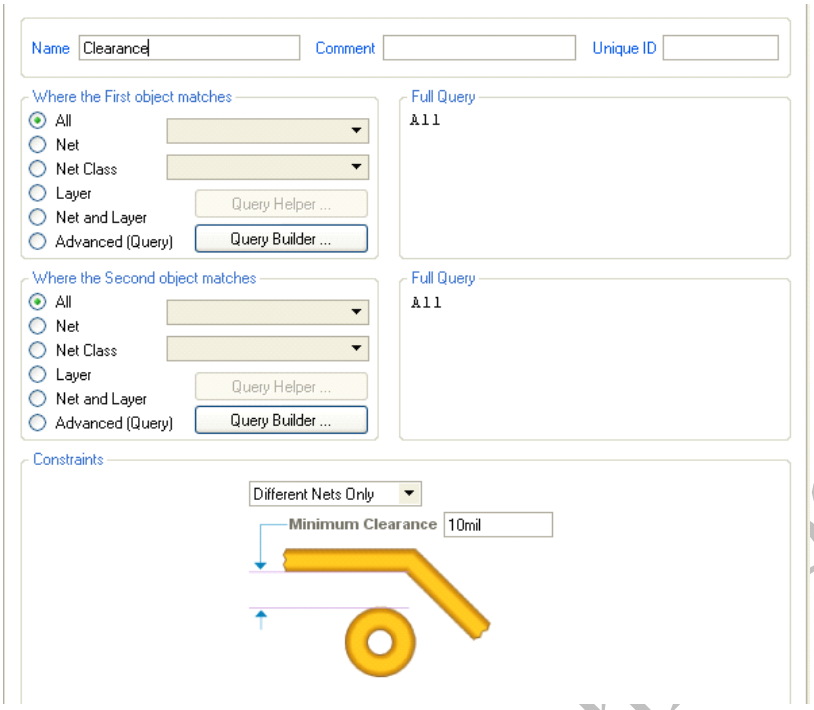

Fig 3 Define the Minimum clearance

When you use the via make sure the min hole size is>10mil, for a low cost PCB the via diameter>15mil and the pad around the via diameter >23mil, which will give a min ring of 8mil. One example is shown in Fig 4. If space is not a problem always try to have a min 15mil hole and 10mil ring.

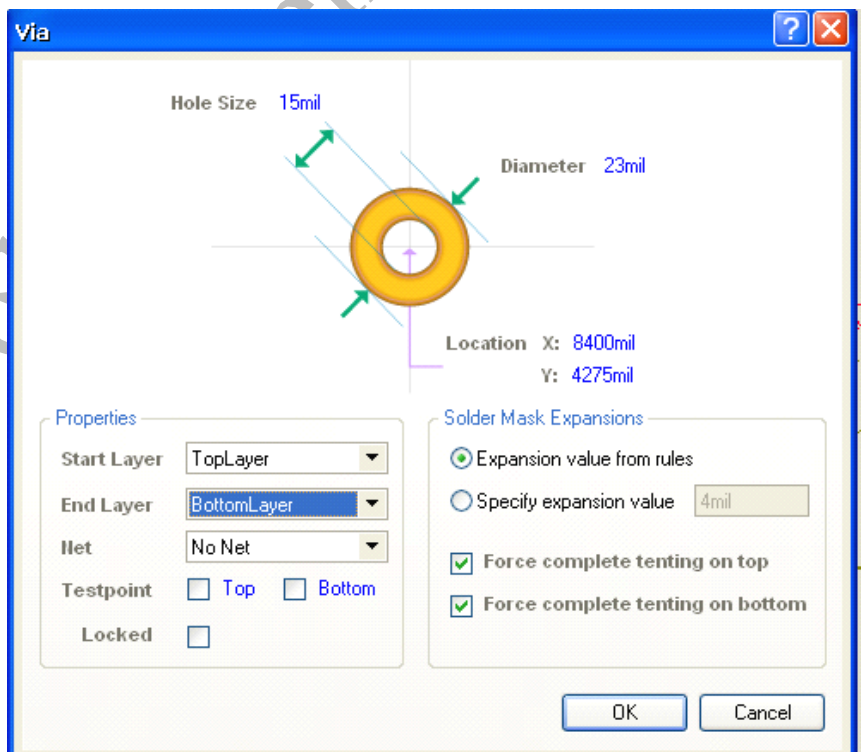

Fig 4 Define the via and ring

There is only min size limitation, so it is not a problem to define a larger clearance or hole size. The definition hole size is the “finished” hole size in the PCB and has a +/-3-5mil tolerance. Trace width on the final PCB will has tolerance +/-15%-20%.

You can also define other design rules some rules are shown in Fig 5, and those rules will not be explained one by one. Most of time we only need to define the electrical rules and use default setting for other rules.

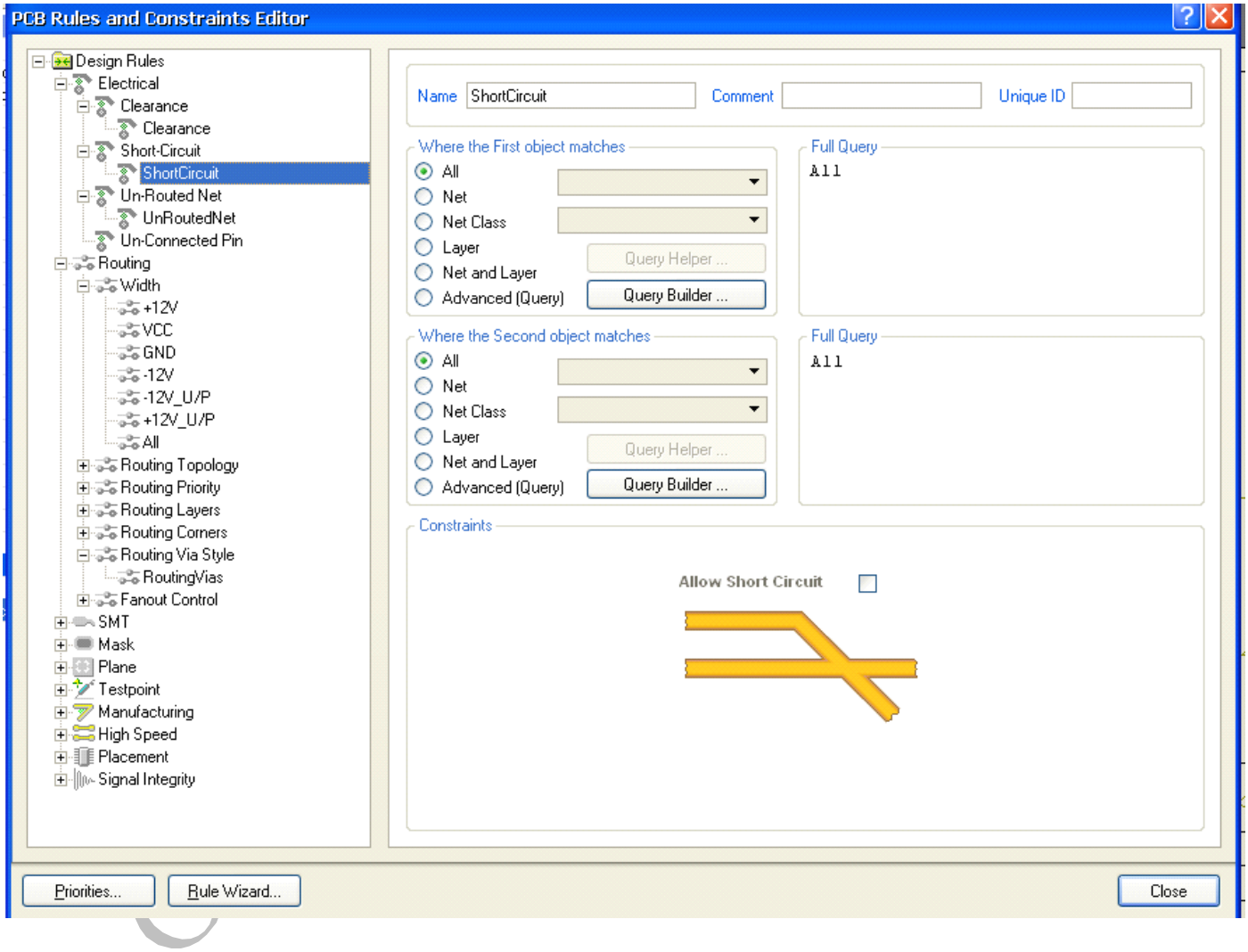

Fig 5 Other rules for the PCB design

II. Basic Technologies in PCB manufacture

In this section we will discuss some basic technologies used in PCB manufacture.

A. V Score

Most of the time we just need individual board, but to increase the efficiency of assembly, or when the board is too small (X,Y dimension less than 1inch), then we need panelize the

small boards to improve manufacturing efficiency.

Fig 6 shows a drawing for a V score panel. The clearance between boards is 30mil.Usually we keep the V score clearance 20-40mil. V core can only be used for regular shape board. And the tolerance is +/-6-8mil. In the panel usually we will add a 0.25" blank material around the panel which is called carriers, on the carriers 4 tooling holes and four fiducial marks will be added, this feature is useful for PCB assembly.

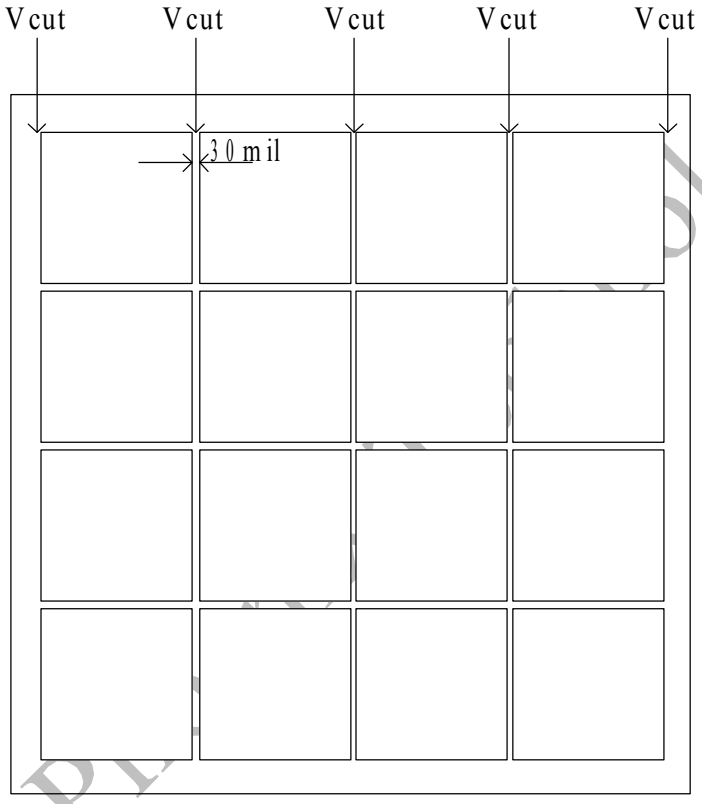

Fig 6 V score panels

Fig 7 Photo of a V score PCB

B. Tab-routing

When the board has irregular shape, or the board need a clear edge then the panel need be tab-routed. Fig 8 shows a drawing for the tab-routing panel, Fig 9 is the photo of the tab-routing panel. In the tab-routing panel in order to break the board off the panel after assembly, V score or "mouse bite holes" can be used. Mouse bite holes is a line of holes works the same way as holes on array of stamps. But keep in mind V score will give a clear edge after the boards are break away from the panels, mouse bite holes" will not give a clear

edge.

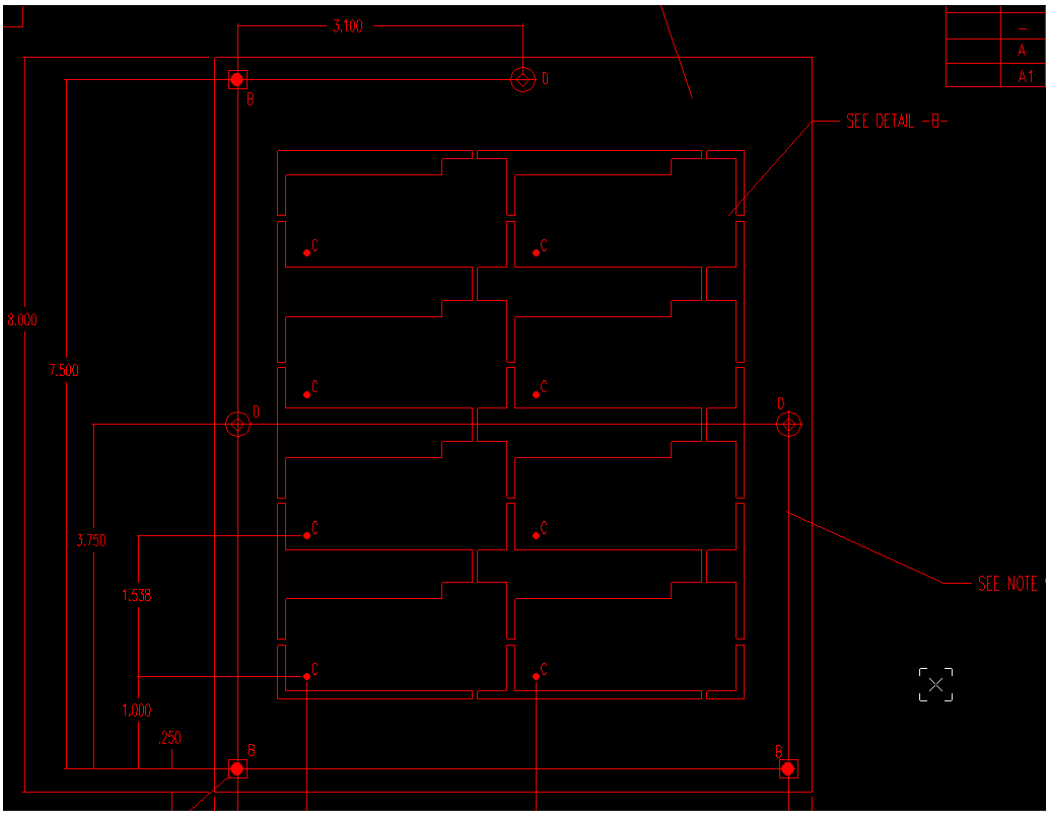

Fig 8 Tab-routing panel

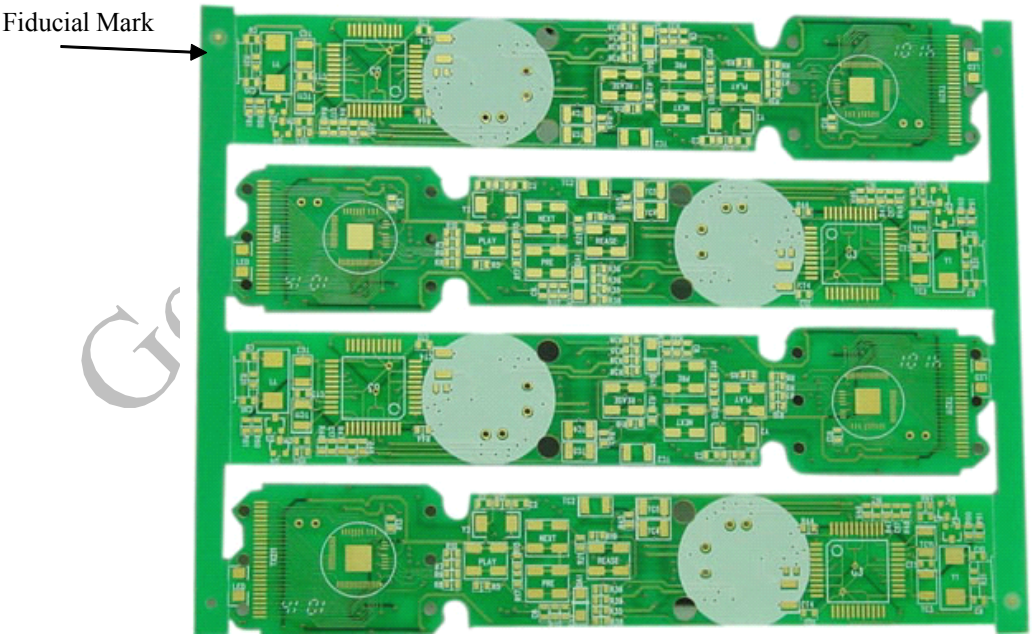

Fig 9 Photo of a tab-routing panel

C. Define Non-plated holes(NPTH)

There are several ways to define the non-plated holes in the PCB.

1) You can define certain hole size to be used as non-plated holes. For example you can define all 40mil holes in your design to be non-plated, and tell the PCB house you want all 40mil hole to be NPTH

2) You can generate separate NC drill files for NPTH holes.

3) The most professional way is to generate a draw chart as shown in Fig 10.

HOLE SUMMARY

TOTAL HOLES: 763

SYMBOL	+	X	Y	◇	Σ	▷|
FINISHED HOLE SIZE	.016	.026	.038	.047	.070	.125
HOLE TYPE	PLATED	PLATED	PLATED	PLATED	NON PLATED	NON PLATED
QUANTITY	591	136	25	4	4	3
TOOL CODE	T01	T02	T03	T04	T05	T06

Fig 10 Hole Chart

D. PCB finishing

The Plain copper on a printed circuit board oxidizes rapidly and has to be coated or plated with something to allow and maintain good solder ability. In the early years protective lacquers were used, roller Tinning quickly followed on along with Hot Air Solder Leveling (HAL; HASL), and the range of chemical finishes. In this section some regular finishing will be introduced.

1. HAL or Lead Free HAL (ROHS).

In this process the boards are fluxed then dipped into a large vertical solder tank. After which the excess solder is blown off with high temperature compressed air. This process produces a flat solder finish suitable for surface mount components.

Hot Air Solder Leveling produces one of the most stable end finishes with very good long term solder-ability. The shelf life of HAL usually can go up to be a few years. Lead free HAL actually works the same way as HAL, the only difference is that lead-free alloys are used in

the process. Usually Lead free HAL will have a higher melt temp compared with regular leaded solders. So if lead free HAL is used as finishing which means that the material used to manufacture PCB will need to with stand have a much higher temp stress. For FR4 with Tg140 usually the max temp is 280 degree for 20 second, Tg170 will can works at 260 degree for 30 minutes. Of course the cost for TG170 material is higher, roughly 30% more than Tg140 material. Tg140 can be used in the lead free HAL process, but need works within its temp specification otherwise copper can lift up.

2. Immersion silver

The immersion silver finish provides a ROHS compliant finish for printed circuit boards (PCB) but is thinner than ENIG or traditional HASL finishes. Immersion silver is a newer PCB finish that offers better performance and superior finishes for final finishes on PCBs.

In this process silver is deposited directly on the copper surface by a chemical displacement reaction and is available in the industry all co-deposit and organic anti tarnish with the immersion silver. This reaction is fast and does not require the relatively high temperatures of ENIG. During assembly the immersion silver dissipates into the solder and allows the formation of a Cu/Sn intermetallic.

Immersion silver is an active surface and readily combines with sulfur from the environment. Silver sulfide tarnishes the surface and creates doubt about the integrity of the finish. The proper packaging of immersion silver finished boards are critical to control sulfurization. The key is to minimize contact of the surface with the environment and to ensure all materials used in the packaging and during storage are sulfur free.

Compared with HAL finishing, immersion silver offers a prefect flat surface and it is more popular in RF applications than HAL.

3. Gold Finishing (Electroless Nickel Immersion Gold)

Electroless nickel immersion gold (ENIG) is a type of surface plating used for printed circuit boards. It consists of electroless nickel plating covered with a thin layer of immersion gold, which protects the nickel from oxidation. The thickness of gold during this process usually is 3-5 micro inch, the thickness of Nick is around 150-250 micro inch.

Compared with HAL ENIG have a much higher cost. But ENIG has several advantages over more conventional (and cheaper) surface platings such as HASL (solder), including excellent surface planarity (particularly helpful for PCB's with large BGA packages), good oxidation resistance, and usability for untreated contact surfaces such as membrane switches and contact points. But consider solderbility HASL is over ENIG.

4. OSP

Organic Solderability Preservatives (OSPs), also known as anti-tarnish. OSP on bare copper printed circuit boards (PCBs) are becoming more prevalent in the electronics industry as the low-cost replacement to Hot Air Solder Leveling (HASL).

The biggest advantage of an OSP finished board is the price. OSP boards tend to be cheaper than those fabricated with other surfaces such as HASL, Immersion Tin, Immersion Silver or ENIG. Another advantage that OSP has, particularly as compared to HASL finished boards, is the flatness of the pads.

The primary drawbacks are related to solderability, shelf life, re-use of misprinted boards, and multiple heating cycles. The solderability/shelf life issues are connected; if the OSP degrades through shelf life (typically less than 1 year), the Copper underneath oxidizes fairly easily and prevents the board from being generally easy to solder.

The re-use of misprinted boards can also be an issue with OSP since alcohol and other solvents used to clean misprinted boards will also remove the OSP, leaving the Copper surface very easy to oxidize. Misprinted boards that are cleaned need to be sent back through the print/place/reflow processes quickly to avoid this issue.

Finally, OSP boards can be susceptible to solderability problems when subjected to multiple heating cycles; this occurs as a result of the OSP itself being degraded by the heating processes. There are new OSP materials that can overcome all of these issues.

E. Solder mask

Solder mask or solder resist is a lacquer-like layer of polymer that provides a permanent protective coating for the copper traces of a printed circuit board (PCB) and prevents solder from bridging between conductors, thereby preventing short circuits. Solder mask was created primarily to facilitate wave soldering used in mass assembly. Solder mask is traditionally

green but is now available in many colors. You can check our website for the different color we can offer, and gold phoenix also has the capacity to mix different solder mask color on the same board, if you have this kind requirement you can email us the gerber files and we can send you a quote.

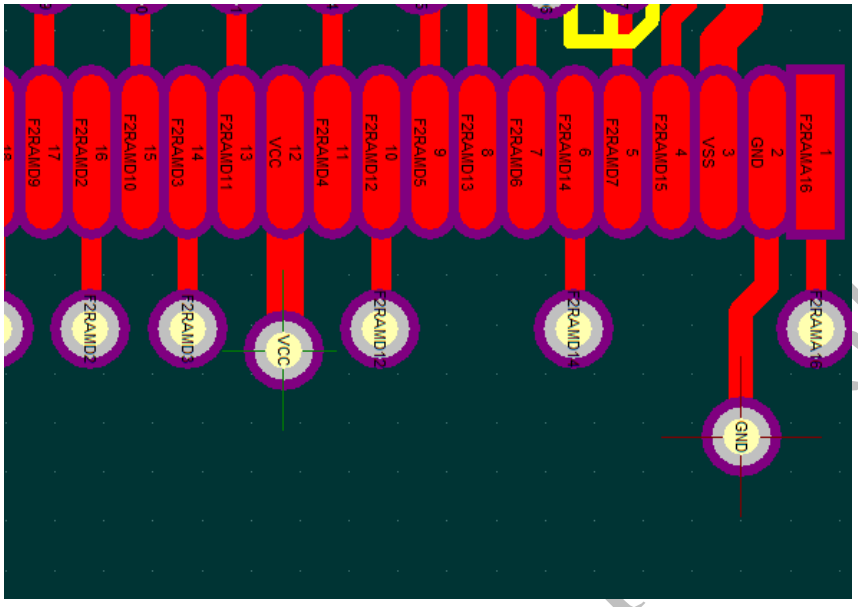

Fig 11 Solder Mask Resolution

4mil clearance is required

Fig 12 Solder Mask layers of Fig 11

For the end user what you really should care is the color of the solder mask, and then the resolution of the solder mask. In Fig 11 shows a fine pitch IC, to assembly this kind IC we would like to have solder mask between of pads so they will not be shorted during the assembly. In order to print solder mask between the pads gold phoenix will require Solder mask dam between pads: minimum: 0.004", preferred: 0.006". if the clearance between pads are less than 4mil we will not be able to print the solder mask. Fig 12 Solder Mask layers of Fig 11, in Fig 12 the black area means solder mask, and we need to have 4mil clearance

between the pads.

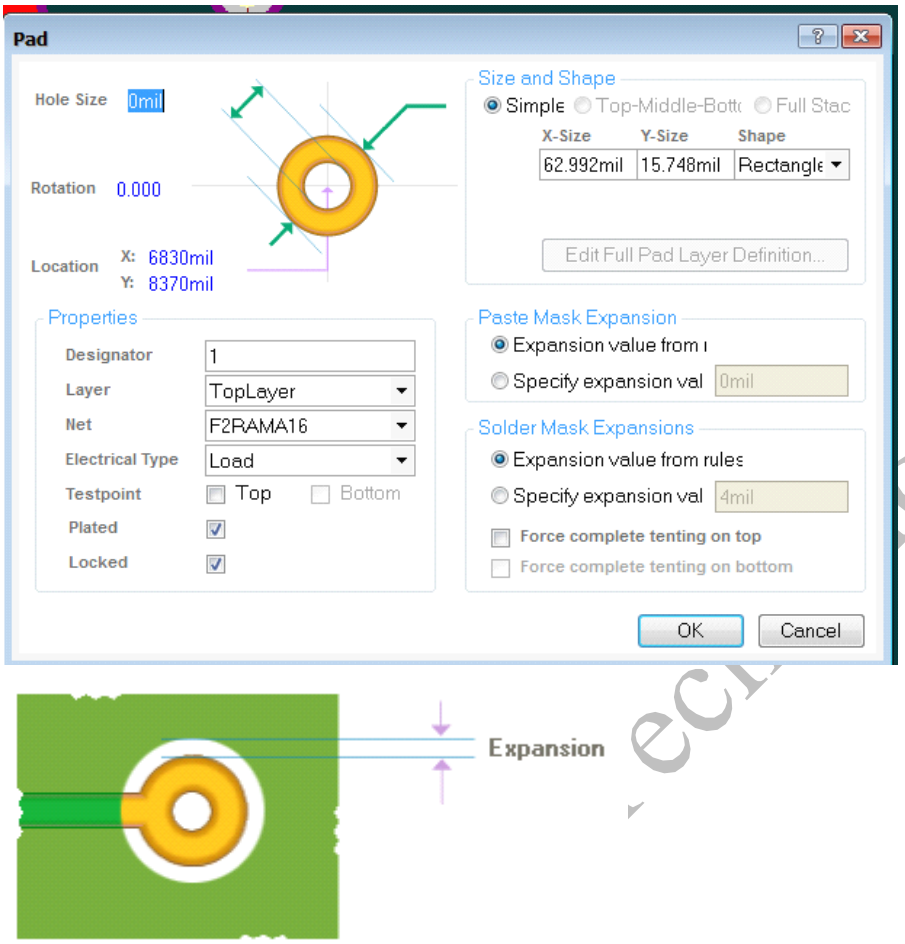

Fig 13 Solder Mask Expansion

When you design the PCB, in the PCB files if the clearance between pads is 4mil that really do not mean that you will have a solder mask dam in the boards you received. Most of the PCB design software has a feature to control the solder mask, called “solder mask expansion”. Due to the limitation of the equipment, all PCB manufacture will require a clearance between the solder pads and “solder mask”, as shown in Fig 13 there will be no solder mask in the expansion area. For example if the solder mask expansion is 4mil, and pads clearance is 4mil which means there will be no solder mask between the pads. With gold phoenix with green solder mask we need at least 4.5mil clearance between pads, and 6mil clearance for black solder mask in order to print solder mask between pads.

F. Silk Screen

Silk screen is to print the “Text” on the PCB board, usually the color of the silk screen is white, with gold phoenix we also provide black silk screen. Screen printing is a printing

technique that uses a woven mesh to support an ink-blocking stencil. The attached stencil forms open areas of mesh that transfer ink or other printable materials which can be pressed through the mesh as a sharp-edged image onto a substrate. A roller or squeegee is moved across the screen stencil, forcing or pumping ink past the threads of the woven mesh in the open areas.

For the PCB designer what you really need care is the color of the silk screen, you need one side silk screen or two side silk screen. With gold phoenix we offer white silk screen and one side silk (top side or bottom side) silk by default. Two side silk screen(print text on both top and bottom side) will result extra charge.

Another thing you maybe should know is the min size of the silk screen the PCB manufacture can support. With gold phoenix the min text size we support is height 25mil, width 6mil. Small text size make it difficult to read, the min text size we suggest is width 6mil, height 50mil.

G. Copper thickness and Via current handling capacity

In PCB industry the thickness of the copper on the PCB is defined use oz. 1oz=35um. Thicker copper means the trace and pass more current.

This PCB track width calculator determines approximations to the ANSI/IPC-D-275 and IPC-2221 design standards for PCB trace / track width.

$$W = \left(\frac{1}{1.4h}\right)\left(\frac{I}{k\Delta T^{0.421}}\right)^{1.379}$$

where:

W = Minimum required track width in mils

I = Maximum current in Amps

dT = Maximum allowable temperature rise above ambient in C

h = Thickness of the copper cladding in oz/ft^2

k = 0.024 for inner layers and k= 0.048 for outer layers

This calculator is accurate up to 35A current, up to 400mils of trace width, from 10C to 100C temperature rise, and copper of 0.5oz/ft to 3oz/ft. Outside of this ranges, calculator won't produce accurate results. The DC resistance of the trace can be calculated as below: for

copper at 25 degree p=1.724X10-8ohm/meter, at 100 degree p=2.3X10-8ohm/meter. AC resistance is more complex due to skin effect.

$$R_{DC} = p\frac{L}{A}$$

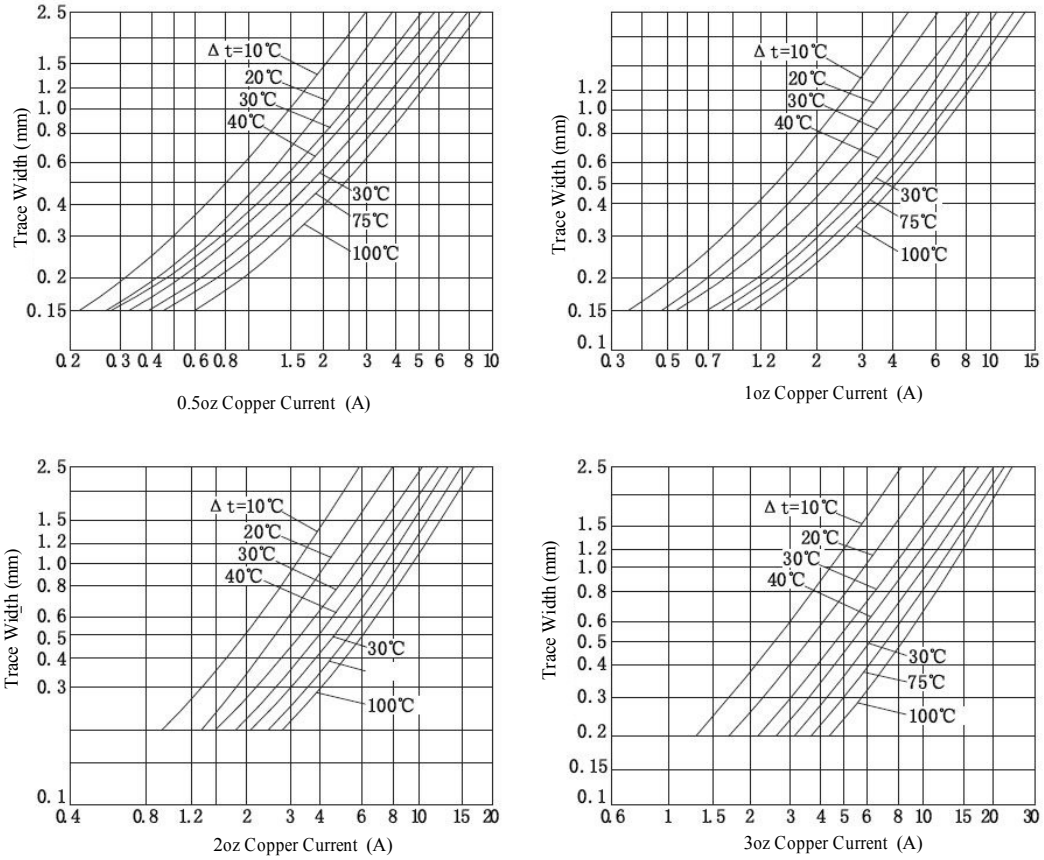

Fig 14 Current Handling Capacity of PCB Trace.

Fig 14 shows the current handling capacity of 0.5oz-3oz copper with different temp raise.

H. Via

To estimate via current handling capacity, a via can be equivalent to a trace.

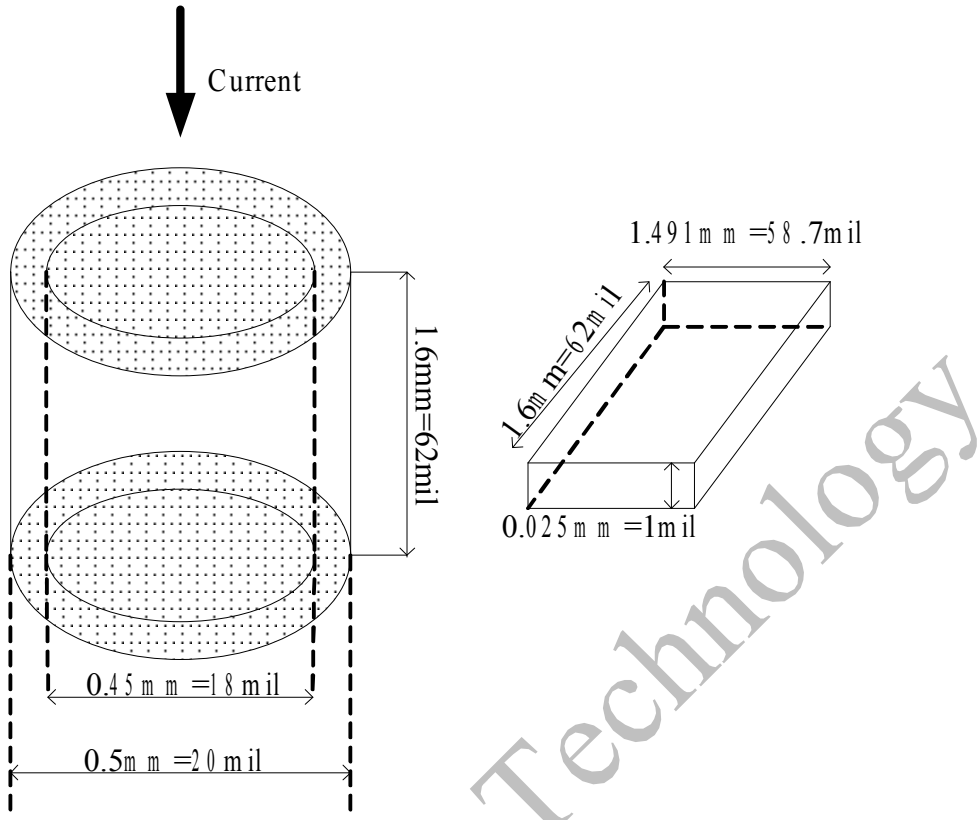

Fig 15 Via in PCB Board equivalent to PCB trace.

Fig 15 shows a via in the PCB. The current will follow through this via from top layer to the bottom layer. There is a 1mil copper plated in the via, this via can be equivalent to a trace with 1.6mm in length, 14.9mm width and 1mil copper thickness. Use the info from section F. the current handling capacity of this Via can be calculated, 2A is the result. The resistance of the Via can be calculated use following equation, and the result is 0.98mohm at 100 degree, and a 2A current will result a 2mV voltage drop. To increase the current handling capacity a multi via can be place in parallel to reduce the resistance.

$$R_{DCVia} = p\frac{L}{\pi(r_1^2 - r_2^2)} = 2.3X10^{-8}\frac{1.6 * 10^3}{3.14 * (0.25^2 - 0.225^2)}$$

I. Slot

Slot design can be a headache for a new PCB designer. The major problem for a PCB designer is that you need to make sure the PCB manufacture "KNOW" that there are slots in your design. The easiest way to design a slot is to use multi via overlap with each other to

make a slot in the shape you want. In this way the slot will be show up in the NC drill file, as long as you generate the NC drill files right you should be able to see the slot in your design.

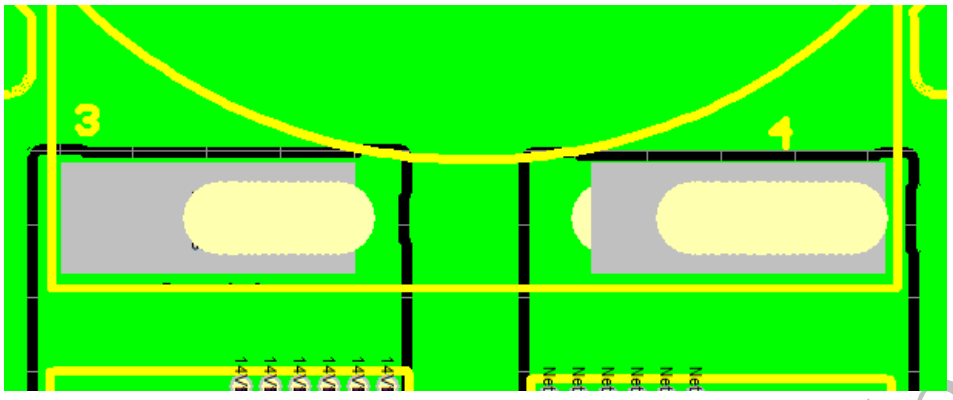

Fig 16 Make slot by using Vias overlap with each other

Fig 16 shows two slots by using vias overlap with each other. With gold phoenix the min slot size we can make is 0.65mmX0.7mm.

J. Voltage break points

There is an Experiments performed by UL in the course of analysis of silver PCB surface finish, demonstrated that the withstand voltage of a pair of parallel conductors is purely a function of conductor spacing, not surface finish. Based on the experiments, UL specified withstand voltage of 40 volts/mil or about 1.6 kW/mm in their test methods of UL796 Standard for Printed Wiring Boards. For example, for working voltage 500V you need to meet the withstanding test voltage 1740 Vrms per UL 60950-1 Table 5B. Such AC signal has 1740*√2=2461 V peak value. With the 40V/mils criterion, the required minimum spacing would be 2461/40=62 mils (or 1.6 mm). More info can be found at http://www.smps.us/pcbtracespacing.html

	Bare Board								Assembly					
	Internal layers		External conductors, uncoated		External conductors, uncoated, >3050 m		External conductors coated		External conductors with conformal coating		External component leads, uncoated		Component leads with conformal coating	
Vpk, V	mm	inch	mm	inch	mm	inch	mm	inch	mm	inch	mm	inch	mm	inch
15	0.05	0.002	0.1	0.004	0.1	0.004	0.05	0.002	0.13	0.006	0.13	0.006	0.13	0.006
30	0.05	0.002	0.1	0.004	0.1	0.004	0.05	0.002	0.13	0.006	0.25	0.01	0.13	0.006
50	0.1	0.004	0.6	0.024	0.6	0.024	0.13	0.006	0.13	0.006	0.4	0.016	0.13	0.006
100	0.1	0.004	0.6	0.024	1.5	0.06	0.13	0.006	0.13	0.006	0.5	0.02	0.13	0.006
150	0.2	0.008	0.6	0.024	3.2	0.13	0.4	0.016	0.4	0.016	0.8	0.032	0.4	0.016
170	0.2	0.008	1.25	0.05	3.2	0.13	0.4	0.016	0.4	0.016	0.8	0.032	0.4	0.016
250	0.2	0.008	1.25	0.05	6.4	0.26	0.4	0.016	0.4	0.016	0.8	0.032	0.4	0.016
300	0.2	0.008	1.25	0.05	12.5	0.5	0.4	0.016	0.4	0.016	0.8	0.032	0.8	0.032
500	0.25	0.01	2.5	0.1	12.5	0.5	0.8	0.032	0.8	0.032	1.5	0.06	0.8	0.032
1000	1.5	0.06	5	0.2	25	0.99	2.33	0.092	2.33	0.1	3.03	0.12	2.33	0.092
2000	4	0.158	10	0.4	50	1.97	5.38	0.22	5.38	0.22	6.08	0.24	5.38	0.22
3000	6.5	0.256	15	0.6	75	2.96	8.43	0.34	8.43	0.34	9.13	0.36	8.43	0.34
4000	9	0.355	20	0.79	100	3.94	11.48	0.46	11.48	0.46	12.18	0.48	11.48	0.46
5000	11.5	0.453	25	0.99	125	4.93	14.53	0.58	14.53	0.58	15.23	0.6	14.53	0.58

Fig 17 Clearance requirement of voltage level

K. Half hole design

Half PTH holes are usually designed at the edge of the board, the holes are plated. The way to design this is just to put the holes at the edge of the board, and put the border line across the middle of the holes. The min hole size will need to be 0.8mm (32mil), the min clearance between the holes need to be 1.1mm from the center from one hole to another. There is no requirements for the size of the pads, you can design the pads the same size as the hole.

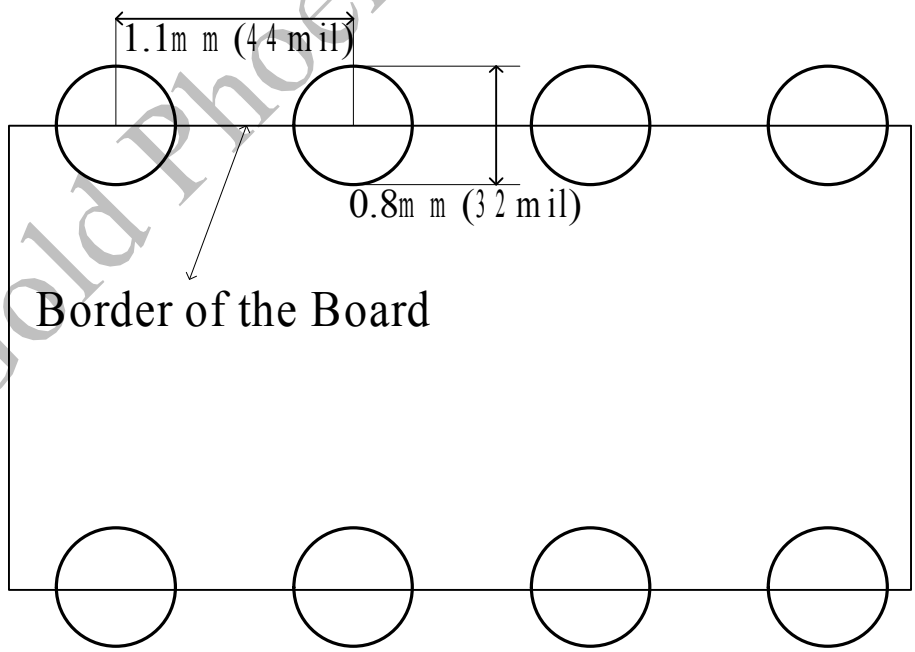

Fig 18 Half Hole Design Example

III. Prepare Manufacture Files for PCB House

The most common problem when generate gerber files is that our customer did not include all necessary files. For 2 layers you should include : Top copper layers, Bot copper layer, Top Silk Screen, Bot Silk Screen(if you have), Top Solder Mask, Bot Solder Mask. And NC drill files. If the board is multi-layers, you also need to include inner layers in the gerber file. Each layer will be one file, so for 2 layers you will have 5-6 files plus NC drill. If you define the border of the board use mechanical layers please also include ship layer in the gerber file. Each layer should have a unique extension, below give some example.

- TopCopper - ".gtl" , ".cmp", ".top"
- BottomCopper - ".gbl", ".sol", ".bot"
- TopSolderMask - ".gts", ".stc", ".smt", ".stoptop", ".tsm"
- BottomSolderMask - ".gbs", ".sts", ".smb", ".stopbot", ".bsm"
- TopSilk - ".gto", ".plc", ".sst", ".positop", ".leg", ".slk"
- BottomSilk - ".gbo", ".pls", ".ssb", ".posibot", ".bsk"
- Drill - ".drl", ".txt", ".tap", ".drill", ".gdd", ".drd", ".cnc", ".exl"
- KeepOut - ".gko"
- MiddleCopper1 - ".g2"
- MiddleCopper2 - ".g3"
- BottomStencil - ".gbp"
- TopStencil - ".gtp"
- Outline - ".outline", ".oln"

For gold phoenix we need gerber files in 274X format. After you generate the gerber files use a free gerber view to check the file, make sure the file looks right. Keep in mind gerber files sometimes does not look the same as your PCB files, so it is 100% necessary to check the files before you send the files to the board house to place order.

After the gerber files and NC drill is done, put zip the all files into one ZIP file, and name the file use the same name as your project name. We suggest do not name the file name as gerber or panel, those files are too common. If there is any version change also change the file name and add the version to the file name. In this way it will make it a lot easier when you want order the same board again, otherwise after a few months if you have too many version

everything will mass up.

Different PCB software will have different steps to generate gerber files, what you really need to keep in mind is that: IN INCLUDE ALL LAYERS YOU WANT, SELECT 274X FORMAT, INCLUDE NC DRILL FILE. Finally we would hope this tutorial is helpful for you. If you have any questions please email us

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