# CHAPTER 12: PRINTED CIRCUIT BOARD (PCB) DESIGN ISSUES

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## Introduction

Printed circuit boards (PCBs) are by far the most common method of assembling modern electronic circuits. Comprised of a sandwich of one or more insulating layers and one or more copper layers which contain the signal traces and the powers and grounds, the design of the layout of printed circuit boards can be as demanding as the design of the electrical circuit.

Most modern systems consist of multilayer boards of anywhere up to eight layers (or sometimes even more). Traditionally, components were mounted on the top layer in holes which extended through all layers. These are referred as through hole components. More recently, with the near universal adoption of surface mount components, you commonly find components mounted on both the top and the bottom layers.

The design of the printed circuit board can be as important as the circuit design to the overall performance of the final system. We shall discuss in this chapter the partitioning of the circuitry, the problem of interconnecting traces, parasitic components, grounding schemes, and decoupling. All of these are important in the success of a total design.

PCB effects that are harmful to precision circuit performance include leakage resistances, IR voltage drops in trace foils, vias, and ground planes, the influence of stray capacitance, and dielectric absorption (DA). In addition, the tendency of PCBs to absorb atmospheric moisture (*hygroscopicity*) means that changes in humidity often cause the contributions of some parasitic effects to vary from day to day.

In general, PCB effects can be divided into two broad categories—those that most noticeably affect the static or dc operation of the circuit, and those that most noticeably affect dynamic or ac circuit operation, especially at high frequencies.

Another very broad area of PCB design is the topic of grounding. Grounding is a problem area in itself for all analog and mixed signal designs, and it can be said that simply implementing a PCB based circuit doesn't change the fact that proper techniques are required. Fortunately, certain principles of quality grounding, namely the use of ground planes, are intrinsic to the PCB environment. This factor is one of the more significant advantages to PCB based analog designs, and appreciable discussion of this section is focused on this issue.

Some other aspects of grounding that must be managed include the control of spurious ground and signal return voltages that can degrade performance. These voltages can be due to external signal coupling, common currents, or simply excessive IR drops in ground conductors. Proper conductor routing and sizing, as well as differential signal

handling and ground isolation techniques enables control of such parasitic voltages.

One final area of grounding to be discussed is grounding appropriate for a mixed-signal, analog/digital environment. Indeed, the single issue of quality grounding can influence the entire layout philosophy of a high performance mixed signal PCB design—as it well should.

# SECTION 1: PARTITIONING

Any subsystem or circuit layout operating at high frequency and/or high precision with both analog and digital signals should like to have those signals physically separated as much as possible to prevent crosstalk. This is typically difficult to accomplish in practice.

Crosstalk can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. TTL and CMOS digital signals have high edge rates, implying frequency components starting with the system clock and going up form there. And most logic families are saturation logic, which has uneven current flow (high transient currents) which can modulate the ground. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal. Noise on the sampling clock manifests itself as phase jitter, which as we have seen in a previous section, translates directly to reduced SNR of the sampled signal. If clock driver packages are used in clock distribution, only one frequency clock should be passed through a single package. Sharing drivers between clocks of different frequencies in the same package will produce excess jitter and crosstalk and degrade performance.

The ground plane can act as a shield where sensitive signals cross. Figure 12.1 shows a good layout for a data acquisition board where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as simple as this, the principle remains a valid one.

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run in parallel—it is therefore imperative to separate them with ground pins (creating a Faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (typically on the order of 10 mΩ) when the board is new—as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to allocate extra PCB connector pins so that there are many ground connections (perhaps 30% to 40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection.

Manufacturers of high performance mixed-signal ICs, like Analog Devices, often offer evaluation boards to assist customers in their initial evaluations and layout. ADC evaluation boards generally contain an on-board low jitter sampling clock oscillator, output registers, and appropriate power and signal connectors. They also may have additional support circuitry such as the ADC input buffer amplifier and external reference.

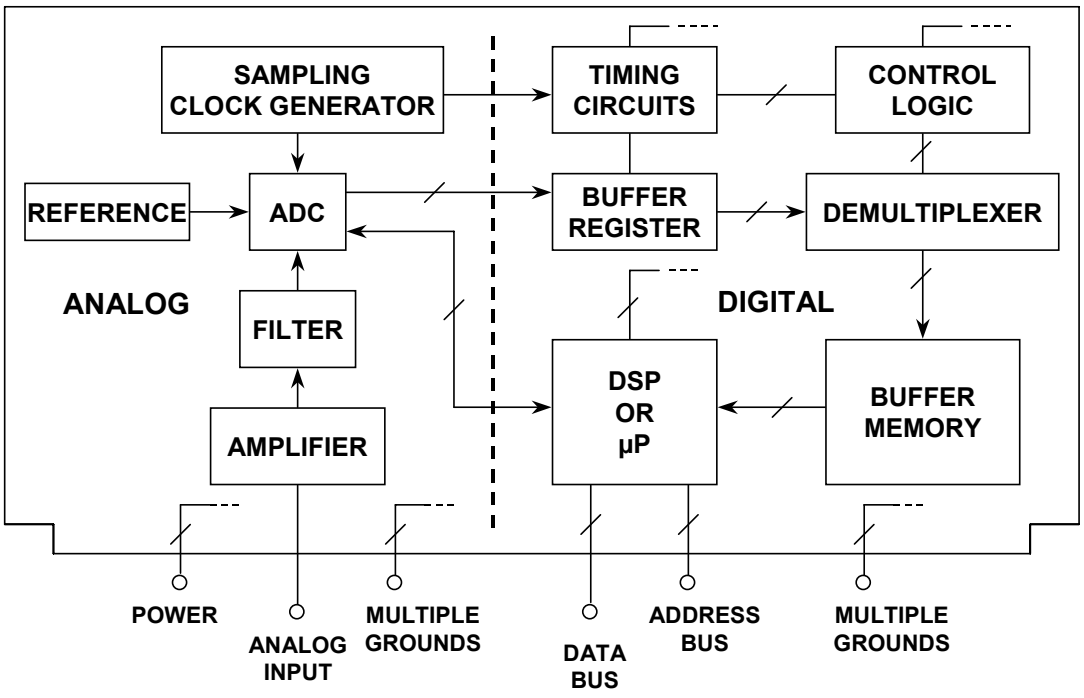



***Figure 12.1:*** *Analog and Digital Circuits Should Be Partitioned on PCB Layout*

The layout of the evaluation board is optimized in terms of grounding, decoupling, and signal routing and can be used as a model when laying out the ADC section of the PC board in a system. The actual evaluation board layout is usually available from the ADC manufacturer in the form of computer CAD files (Gerber files). In many cases, the layout of the various layers appears on the data sheet for the device. It should be pointed out, though, that an evaluation board is an extremely simple system. While some guidelines can be inferred from inspection of the evaluation board layout, the system that you are designing is undoubtedly more complicated. Therefore, direct use of the layout may not be optimum in larger systems.

# SECTION 2: TRACES

## Resistance of Conductors

Every engineer is familiar with resistors. But far too few engineers consider that all the wires and PCB traces with which their systems and circuits are assembled are also resistors (as well as inductors as well, as will be discussed later). In higher precision systems, even these trace resistances and simple wire interconnections can have degrading effects. Copper is *not* a superconductor—and too many engineers appear to think it is!

Figure 12.2 illustrates a method of calculating the sheet resistance R of a copper square, given the length Z, the width X, and the thickness Y.

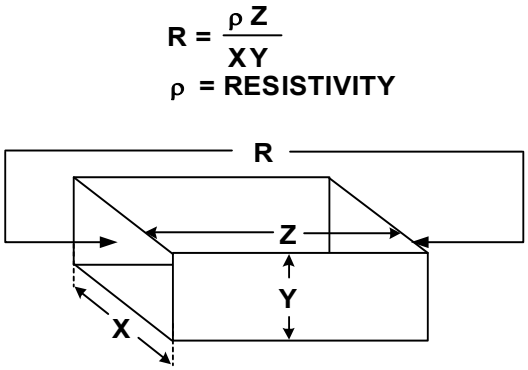



***Figure 12.2:*** *Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors*

At 25°C the resistivity of pure copper is $1.724X10^{-6}$ Ω/cm. The thickness of standard 1 ounce PCB copper foil is 0.036 mm (0.0014"). Using the relations shown, the resistance of such a standard copper element is therefore 0.48 mΩ/square. One can

readily calculate the resistance of a linear trace, by effectively "stacking" a series of such squares end to end, to make up the line's length. The line length is Z and the width is X, so the line resistance R is simply a product of Z/X and the resistance of a single square, as noted in the figure.

For a given copper weight and trace width, a resistance/length calculation can be made. For example, the 0.25 mm (10 mil) wide traces frequently used in PCB designs equates to a resistance/length of about 19 mΩ/cm (48 mΩ /inch), which is quite large. Moreover, the temperature coefficient of resistance for copper is about 0.4%/°C around room temperature. This is a factor that shouldn't be ignored, in particular within low impedance precision circuits, where the TC can shift the net impedance over temperature.

As shown in Figure 12.3, PCB trace resistance can be a serious error when conditions aren't favorable. Consider a 16-bit ADC with a 5 kΩ input resistance, driven through 5 cm of 0.25 mm wide 1 oz. PCB track between it and its signal source. The track resistance of nearly 0.1 Ω forms a divider with the 5 kΩ load, creating an error. The resulting voltage drop is a gain error of 0.1/5 k (~0.0019%), well over 1 LSB (0.0015% for 16 bits). And this ignores the issue of the return path! It also ignores inductance, which could make the situation worse at high frequencies.

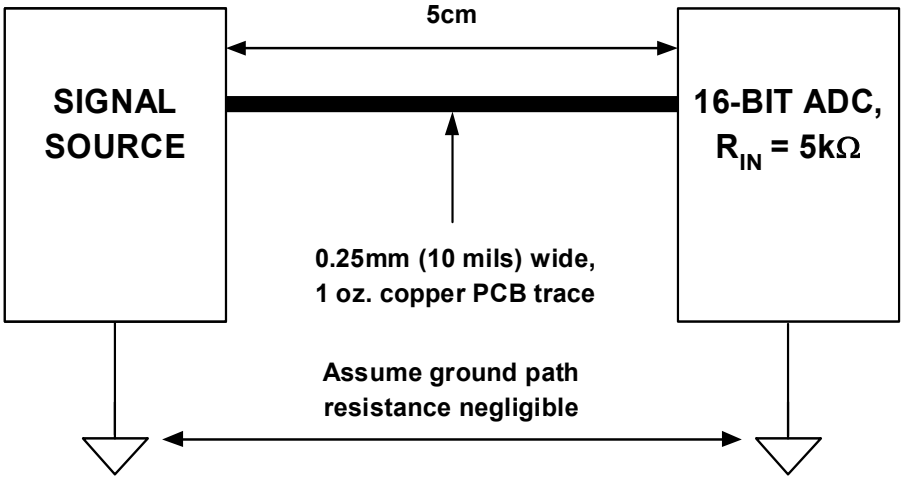



***Figure 12.3:*** *Ohm's law predicts >1 LSB of error due to drop in PCB conductor*

So, when dealing with precision circuits, the point is made that even simple design items such as PCB trace resistance cannot be dealt with casually. There are various solutions that can address this issue, such as wider traces (which may take up excessive space), and may not be a viable solution with the smallest packages and with packages with multiple rows of pins, such as a ball grid array (BGA), the use of heavier copper (which may be too expensive) or simply choosing a high input impedance converter. But, the most important thing is to think it all through, avoiding any tendency to overlook items appearing innocuous on the surface.

## Voltage Drop in Signal Leads—Kelvin Feedback

The gain error resulting from resistive voltage drop in PCB signal leads is important only with high precision and/or at high resolutions (the Figure 12.3 example), or where large signal currents flow. Where load impedance is constant and resistive, adjusting overall system gain can compensate for the error. In other circumstances, it may often be removed by the use of "Kelvin" or "voltage sensing" feedback, as shown in Figure 12.4.

In this modification to the case of Figure 12.3 a long resistive PCB trace is still used to drive the input of a high resolution ADC, with low input impedance. In this case however, the voltage drop in the signal lead does *not* give rise to an error, as feedback is taken directly from the input pin of the ADC, and returned to the driving source. This scheme allows full accuracy to be achieved in the signal presented to the ADC, despite any voltage drop across the signal trace.

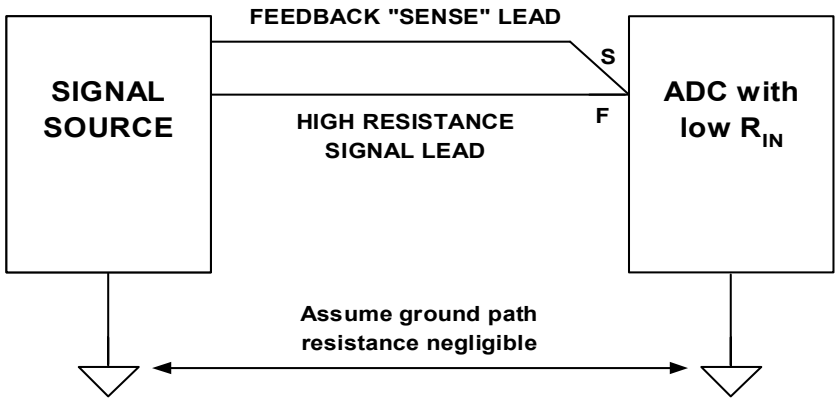



***Figure 12.4:*** *Use of a Sense Connection Moves Accuracy to the Load Point*

The use of separate force (F) and sense (S) connections (often referred to as a Kelvin connection) at the load removes any errors resulting from voltage drops in the force lead, but, of course, may only be used in systems where there is negative feedback. It is also impossible to use such an arrangement to drive two or more loads with equal accuracy, since feedback may only be taken from one point. Also, in this much-simplified system, errors in the common lead source/load path are ignored, the assumption being that ground path voltages are negligible. In many systems this may not necessarily be the case, and additional steps may be needed, as noted below.

## Signal Return Currents

Kirchoff's Law tells us that at any point in a circuit the algebraic sum of the currents is zero. This tells us that all currents flow in circles and, particularly, that the return current must always be considered when analyzing a circuit, as is illustrated in Figure 12.5 (see References 7 and 8).

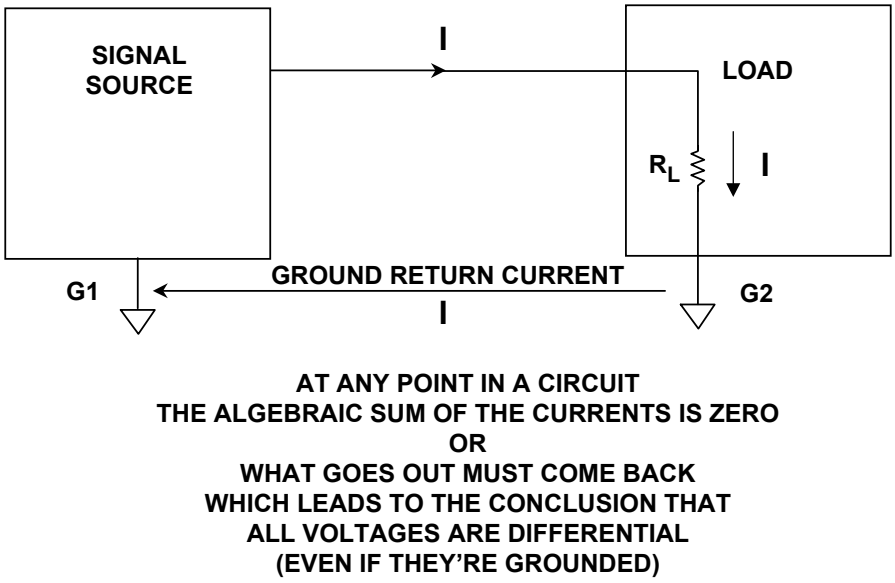



***Figure 12.5:*** *Kirchoff's Law Helps in Analyzing Voltage Drops Around a Complete Source/Load Coupled Circuit*

In dealing with grounding issues, common human tendencies provide some insight into how the correct thinking about the circuit can be helpful towards analysis. Most engineers readily consider the ground return current "I," only when they are considering a fully differential circuit.

However, when considering the more usual circuit case, where a single-ended signal is referred to "ground," it is common to assume that all the points on the circuit diagram where ground symbols are found are at the same potential. Unfortunately, this happy circumstance just ain't necessarily so!

This overly optimistic approach is illustrated in Figure 12.6 where, if it really should exist, "infinite ground conductivity" would lead to zero ground voltage difference between source ground G1 and load ground G2. Unfortunately this approach isn't a wise practice, and when dealing with high precision circuits, it can lead to disasters.

A more realistic approach to ground conductor integrity includes analysis of the impedance(s) involved, and careful attention to minimizing spurious noise voltages.

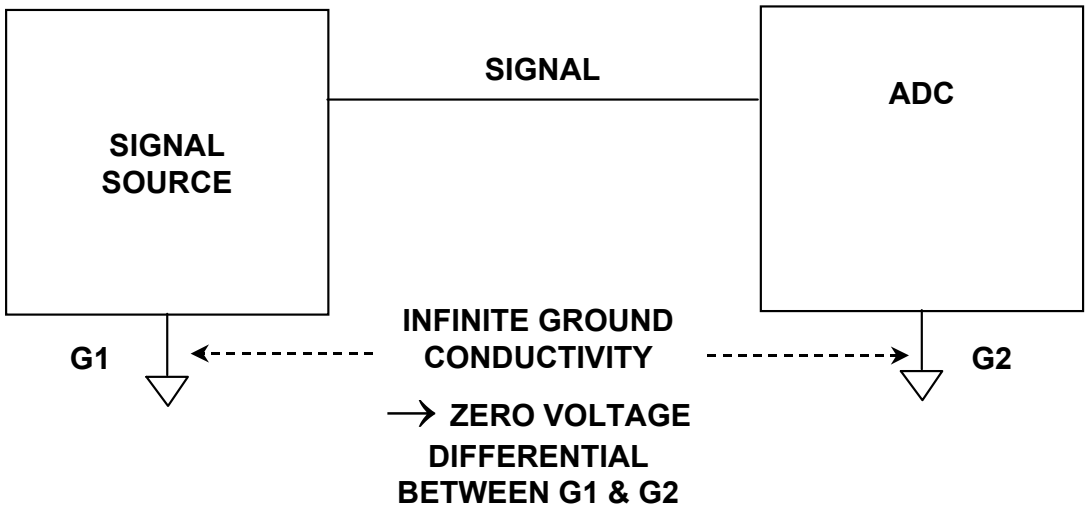



***Figure 12.6:*** *Unlike this Optimistic Diagram, it Is Unrealistic to Assume Infinite Conductivity Between Source/Load Grounds in a Real-World System*

## Ground Noise and Ground Loops

A more realistic model of a ground system is shown in Figure 12.7. The signal return current flows in the complex impedance existing between ground points G1 and G2 as shown, giving rise to a voltage drop $\Delta V$ in this path. But it is important to note that additional *external* currents, such as $I_{EXT}$, may also flow in this same path. It is critical to understand that such currents may generate uncorrelated noise voltages between G1 and G2 (dependent upon the current magnitude and relative ground impedance).

Some portion of these undesired voltages may end up being seen at the signal's load end, and they can have the potential to corrupt the signal being transmitted.

It is evident, of course, that other currents can only flow in the ground impedance, if there is a current path for them. In this case, severe problems can be caused by a high current circuit sharing an *unlooped* ground return with the signal source.

Figure 12.8 shows just such a common ground path, shared by the signal source and a high current circuit, which draws a large and varying current from its supply. This current flows in the common ground return, causing an error voltage $\Delta V$ to be developed.

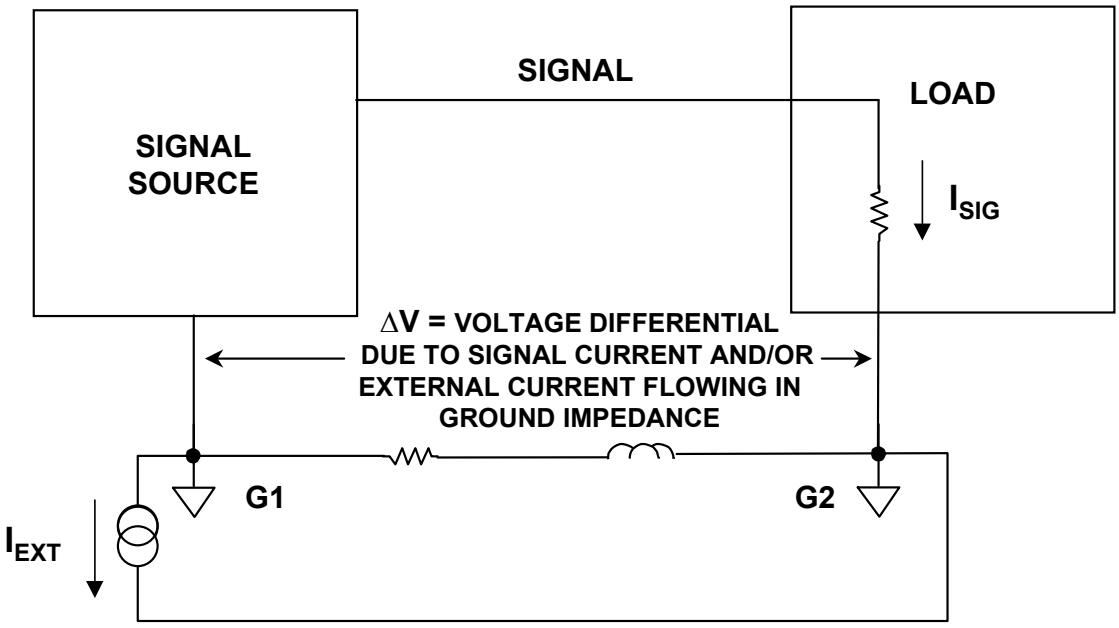



***Figure 12.7:*** *A More Realistic Source-to-Load Grounding System View Includes Consideration of the Impedance Between G1-G2, Plus the Effect of Any Nonsignal-Related Currents*

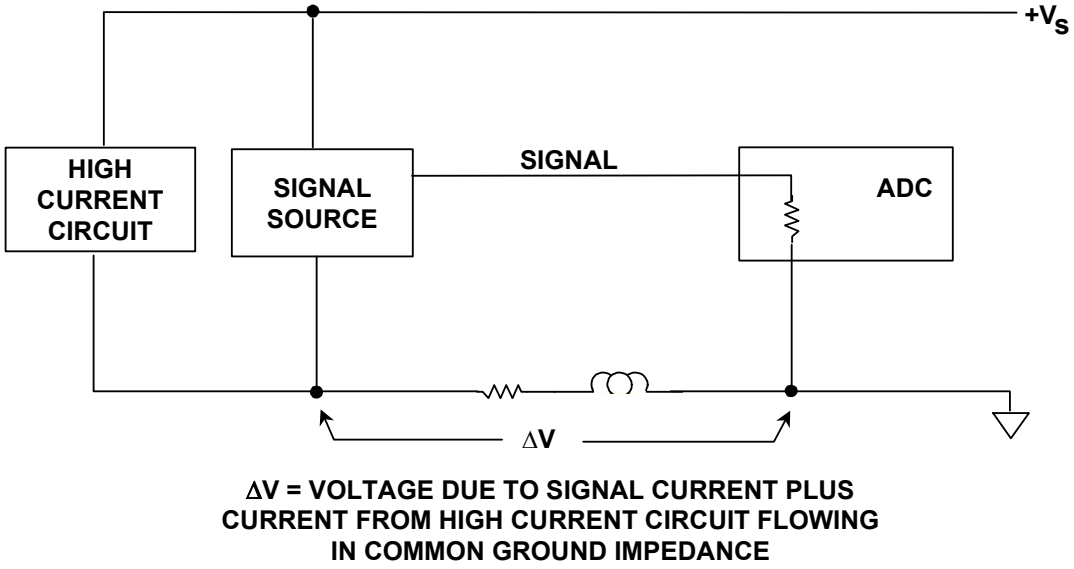



***Figure 12.8:*** *Any Current Flowing Through a Common Ground Impedance Can Cause Errors*

From Figure 12.9, it is also evident that if a ground network contains *loops,* or circular ground conductor patterns (with S1 closed), there is an even greater danger of it being vulnerable to EMFs induced by external magnetic fields. There is also a real danger of ground-current-related signals "escaping" from the high current areas, and causing noise in sensitive circuit regions elsewhere in the system.

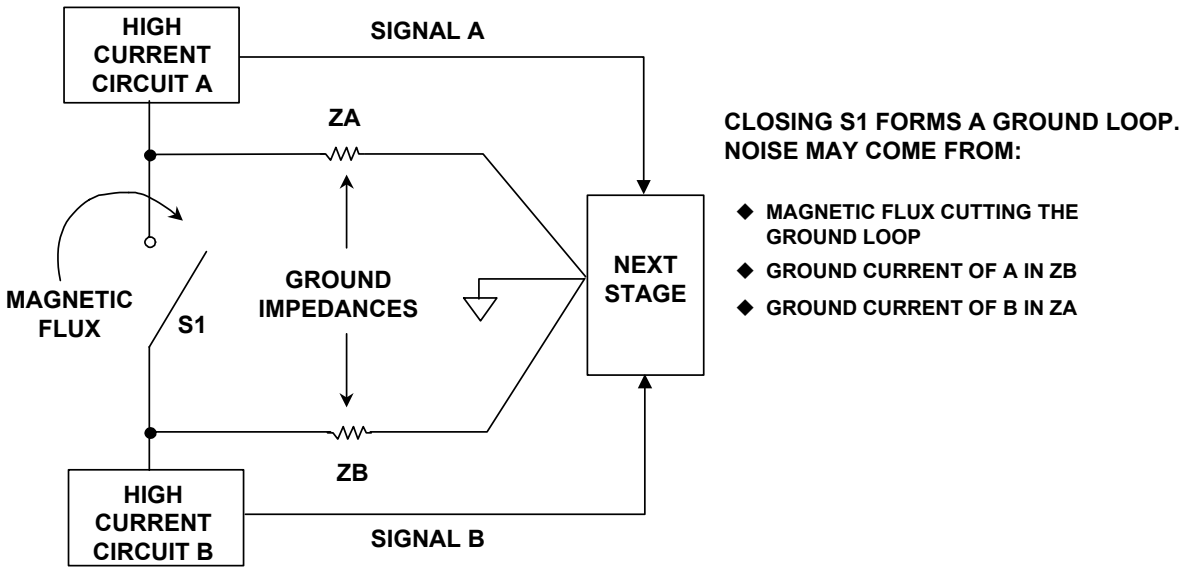



***Figure 12.9:*** *A Ground Loop*

For these reasons ground loops are best avoided, by wiring all return paths within the circuit by separate paths back to a common point, i.e., the common ground point towards the mid-right of the diagram. This would be represented by the S1 open condition.

## Ground Isolation Techniques

While the use of ground planes does lower impedance and helps greatly in lowering ground noise, there may still be situations where a prohibitive level of noise exists. In such cases, the use of ground error minimization and isolation techniques can be helpful.

Another illustration of a common-ground impedance coupling problem is shown in Figure 12.10. In this circuit a precision gain-of-100 preamp amplifies a low level signal $V_{IN}$, using an AD8551 chopper-stabilized amplifier for best dc accuracy. At the load end, the signal $V_{OUT}$ is measured with respect to G2, the local ground. Because of the small 700 μA $I_{SUPPLY}$ of the AD8551 flowing between G1 and G2, there is a 7 μV ground error—about 7 times the typical input offset expected from the op amp!

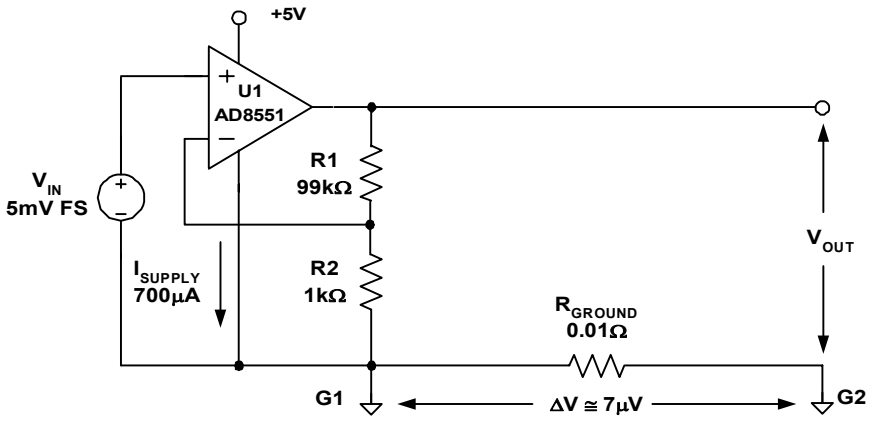



***Figure 12.10:*** *Unless Care Is Taken, Even Small Common Ground Currents Can Degrade Precision Amplifier Accuracy*

This error can be avoided simply by routing the negative supply pin current of the op amp back to star ground G2 as opposed to ground G1, by using a separate trace. This step eliminates the G1-G2 path power supply current, and so minimizes the ground leg voltage error. Note that there will be little error developed in the "hot" $V_{OUT}$ lead, so long as the current drain at the load end is small.

In some cases, there may be simply unavoidable ground voltage differences between a source signal and the load point where it is to be measured. Within the context of this "same-board" discussion, this might require rejecting ground error voltages of several tens-of-mV. Or, should the source signal originate from an "off-board" source, then the magnitude of the common-mode voltages to be rejected can easily rise into a several volt range (or even tens-of-volts).

Fortunately, full signal transmission accuracy can still be accomplished in the face of such high noise voltages, by employing a principle discussed earlier. This is the use of a differential-input, *ground isolation* amplifier. The ground isolation amplifier minimizes the effect of ground error voltages between stages by processing the signal in differential fashion, thereby rejecting CM voltages by a substantial margin (typically 60 dB or more).

Two ground isolation amplifier solutions are shown in Figure 12.11. This diagram can alternately employ either the AD629 to handle CM voltages up to ±270 V, or the AMP03, which is suitable for CM voltages up to ±20 V.

In the circuit, input voltage $V_{IN}$ is referred to G1, but must be measured with respect to G2. With the use of a high CMR unity-gain difference amplifier, the noise voltage ΔV existing between these two grounds is easily rejected. The AD629 offers a typical CMR of 88 dB, while the AMP03 typically achieves 100 dB. In the AD629, the high CMV rating is done by a combination of high CM attenuation, followed by differential gain, realizing a net differential gain of unity. The AD629 uses the first listed value resistors

noted in the figure for R1 to R5. The AMP03 operates as a precision four-resistor differential amplifier, using the 25 kΩ value R1 to R4 resistors noted. Both devices are complete, one package solutions to the ground-isolation amplifier.

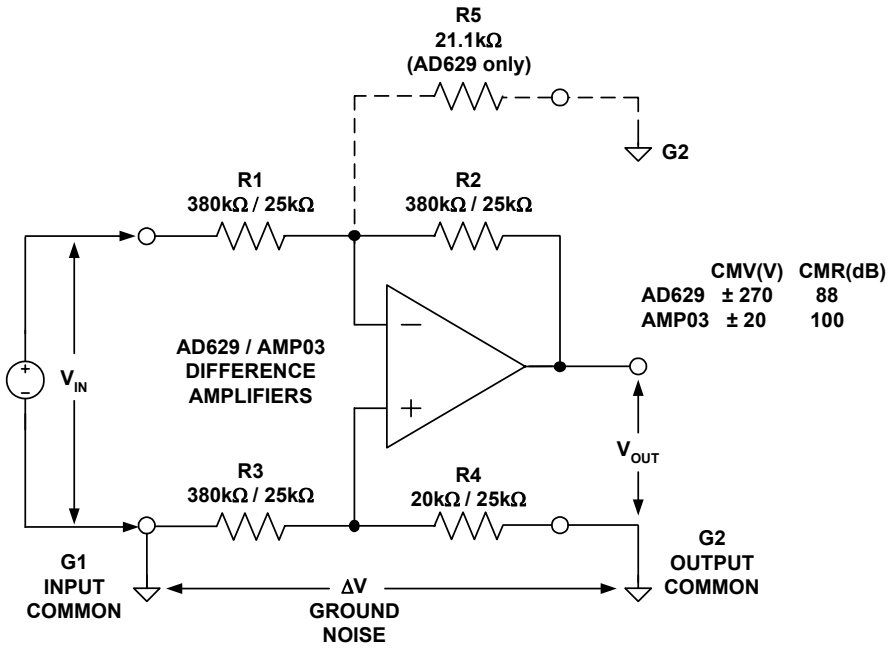



***Figure 12.11:*** *A Differential Input Ground Isolating Amplifier Allows High Transmission Accuracy by Rejecting Ground Noise Voltage Between Source (G1) and Measurement (G2) Grounds*

This scheme allows relative freedom from tightly controlling ground drop voltages, or running additional and/or larger PCB traces to minimize such error voltages. Note that it can be implemented either with the fixed gain difference amplifiers shown, or also with a standard in-amp IC, configured for unity gain. The AD623, for example, also allows single-supply use. In any case, signal polarity is also controllable, by simple reversal of the difference amplifier inputs.

In general terms, transmitting a signal from one point on a PCB to another for measurement or further processing can be optimized by two key interrelated techniques. These are the use of high impedance, differential signal-handling techniques. The high impedance loading of an in-amp minimizes voltage drops, and differential sensing of the remote voltage minimizes sensitivity to ground noise.

When the further signal processing is A/D conversion, these transmission criteria can be implemented *without* adding a differential ground isolation amplifier stage. Simply select an ADC which operates differentially. The high input impedance of the ADC minimizes load sensitivity to the PCB wiring resistance. In addition, the differential input feature allows the output of the source to be sensed directly at the source output terminals (even if single-ended). The CMR of the ADC then eliminates sensitivity to noise voltages between the ADC and source grounds.

An illustration of this concept using an ADC with high impedance differential inputs is shown in Figure 12.12. Note that the general concept can be extended to virtually any signal source, driving any load. All loads, even single-ended ones, become differential-input by adding an appropriate differential input stage. The differential input can be provided by either a fully developed high Z in-amp, or in many cases it can be a simple subtractor stage op amp, such as Figure 12.11.

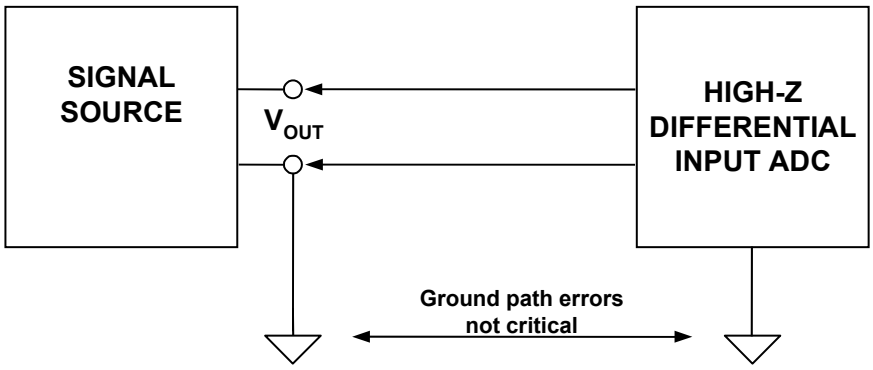



***Figure 12.12:*** *A High-Impedance Differential Input ADC Also Allows High Transmission Accuracy Between Source and Load*

## Static PCB Effects

Leakage resistance is the dominant static circuit board effect. Contamination of the PCB surface by flux residues, deposited salts, and other debris can create leakage paths between circuit nodes. Even on well-cleaned boards, it is not unusual to find 10 nA or more of leakage to nearby nodes from 15-volt supply rails. Nanoamperes of leakage current into the wrong nodes often cause volts of error at a circuit's output; for example, 10 nA into a 10 MΩ resistance causes 0.1 V of error. Unfortunately, the standard op amp pinout places the $-V_S$ supply pin next to the + input, which is often hoped to be at high impedance! To help identify nodes sensitive to the effects of leakage currents ask the simple question: If a spurious current of a few nanoamperes or more were injected into this node, would it matter?

If the circuit is already built, you can localize moisture sensitivity to a suspect node with a classic test. While observing circuit operation, blow on potential trouble spots through a simple soda straw. The straw focuses the breath's moisture, which, with the board's salt content in susceptible portions of the design, disrupts circuit operation upon contact.

There are several means of eliminating simple surface leakage problems. Thorough washing of circuit boards to remove residues helps considerably. A simple procedure includes vigorously brushing the boards with isopropyl alcohol, followed by thorough washing with deionized water and an 85°C bake out for a few hours. Be careful when selecting board-washing solvents, though. When cleaned with certain solvents, some water-soluble fluxes create salt deposits, exacerbating the leakage problem.

Unfortunately, if a circuit displays sensitivity to leakage, even the most rigorous cleaning can offer only a temporary solution. Problems soon return upon handling, or exposure to foul atmospheres, and high humidity. Some additional means must be sought to stabilize circuit behavior, such as conformal surface coating.

Fortunately, there is an answer to this, namely *guarding*, which offers a fairly reliable and permanent solution to the problem of surface leakage. Well-designed guards can eliminate leakage problems, even for circuits exposed to harsh industrial environments. Two schematics illustrate the basic guarding principle, as applied to typical inverting and noninverting op amp circuits.

Figure 12.13 illustrates an inverting mode guard application. In this case, the op amp reference input is grounded, so the guard is a grounded ring surrounding all leads to the inverting input, as noted by the dotted line.

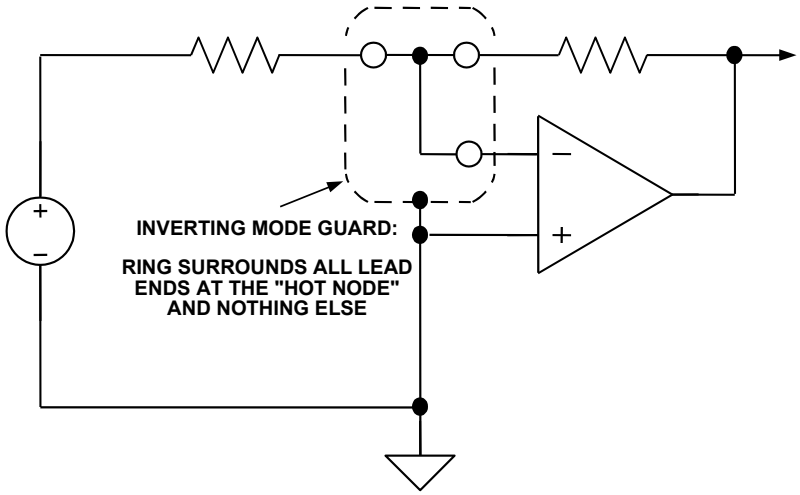



***Figure 12.13:*** *Inverting Mode Guard Encloses All Op Amp Inverting Input Connections Within a Grounded Guard Ring*

Guarding basic principles are simple: *Completely* surround sensitive nodes with conductors that can readily sink stray currents, and maintain the guard conductors at the exact potential of the sensitive node (as otherwise the guard will serve as a leakage source rather than a leakage sink). For example, to keep leakage into a node below 1 pA (assuming 1000-megohm leakage resistance) the guard and guarded node must be within 1 mV. Generally, the low offset of a modern op amp is sufficient to meet this criterion.

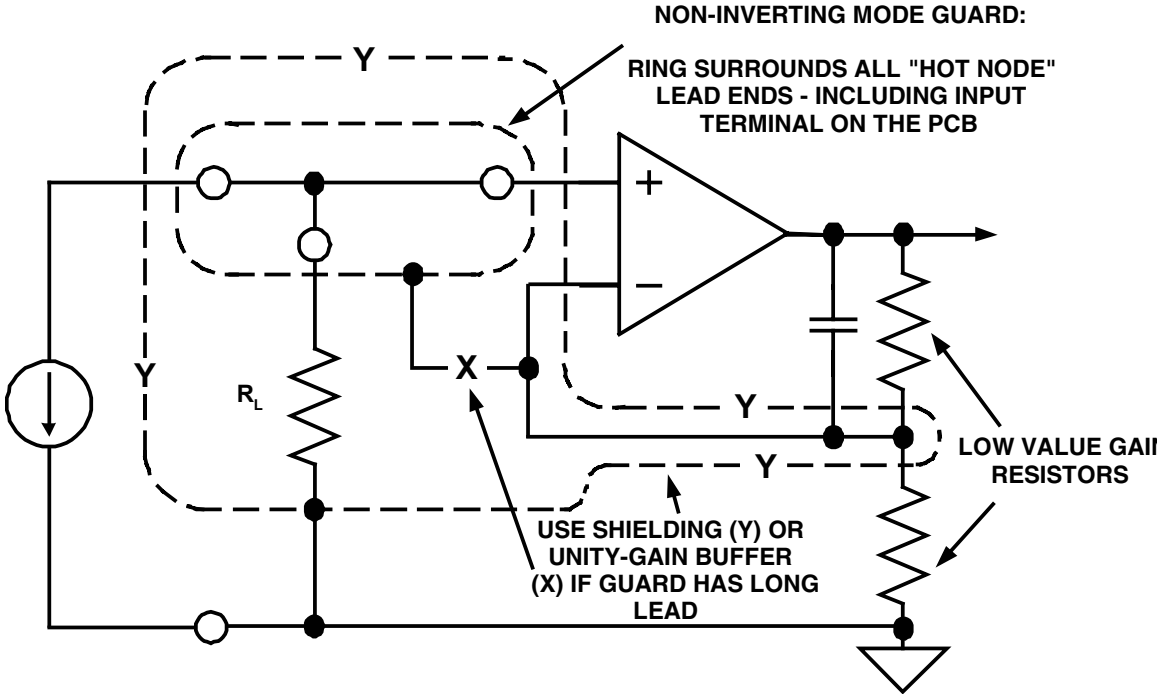



***Figure 12.14:*** *Noninverting Mode Guard Encloses all Op Amp Noninverting Input Connections Within a Low Impedance, Driven Guard Ring*

There are important caveats to be noted with implementing a true high quality guard. For traditional through hole PCB connections, the guard pattern should appear on *both* sides of the circuit board, to be most effective. And, it should also be connected along its length by several vias. Finally, when either justified or required by the system design parameters, do make an effort to include guards in the PCB design process from the outset—there is little likelihood that a proper guard can be added as an afterthought.

Figure 12.14 illustrates the case for a noninverting guard. In this instance the op amp reference input is directly driven by the source, which complicates matters considerably. Again, the guard ring completely surrounds all of the input nodal connections. In this instance, however, the guard is driven from the low impedance feedback divider connected to the inverting input.

Usually the guard-to-divider junction will be a direct connection, but in some cases a unity gain buffer might be used at "X" to drive a cable shield, or also to maintain the lowest possible impedance at the guard ring.

In lieu of the buffer, another useful step is to use an additional, directly grounded screen ring, "Y," which surrounds the inner guard and the feedback nodes as shown. This step costs nothing except some added layout time, and will greatly help buffer leakage effects into the higher impedance inner guard ring.

Of course what hasn't been addressed to this point is just how the op amp itself gets connected into these guarded islands without compromising performance. The traditional method using a TO-99 metal can package device was to employ double-sided PCB guard rings, with both op amp inputs terminated within the guarded ring.

## Sample MINI-DIP and SOIC op amp PCB guard layouts

Modern assembly practices have favored smaller plastic packages such as eight pin MINI-DIP and SOIC types. Some suggested partial layouts for guard circuits using these packages are shown in the next two figures. While guard traces may also be possible with even more tiny op amp footprints, such as SOT-23 etc., the required trace separations become even more confining, challenging the layout designer as well as the manufacturing processes.

For the ADI "N" style MINI-DIP package, Figure 12.15 illustrates how guarding can be accomplished for inverting (left) and noninverting (right) operating modes. This setup would also be applicable to other op amp devices where relatively high voltages occur at pin 1 or 4. Using a standard eight pin DIP outline, it can be noted that this package's 0.1" pin spacing allows a PC trace (here, the guard trace) to pass between adjacent pins. This is the key to implementing effective DIP package guarding, as it can adequately prevent a leakage path from the $-V_S$ supply at pin 4, or from similar high potentials at pin 1.

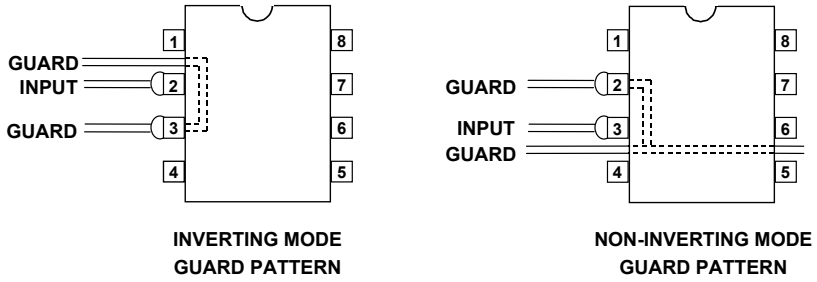



***Figure 12.15:*** *PCB Guard Patterns for Inverting and Noninverting Mode Op Amps Using Eight Pin MINI-DIP (N) Package*

For the left-side inverting mode, note that the Pin 3 connected and grounded guard traces surround the op amp inverting input (Pin 2), and run parallel to the input trace. This guard would be continued out to and around the source and feedback connections of Figure 12-36 (or other similar circuit), including an input pad in the case of a cable. In the right-side noninverting mode, the guard voltage is the feedback divider voltage to Pin 2. This corresponds to the inverting input node of the amplifier, from Figure 12.14.

Note that in both of the cases of Figure 12.15, the guard physical connections shown are only partial—an actual layout would include all sensitive nodes within the circuit. In both the inverting and the noninverting modes using the MINI-DIP or other through hole style package, the PCB guard traces should be located on both sides of the board, with top and bottom traces connected with several vias.

Things become slightly more complicated when using guarding techniques with the SOIC surface mount ("R") package, as the 0.05" pin spacing doesn't easily allow routing of PCB traces between the pins. But, there is still an effective guarding answer, at least for the inverting case. Figure 12.16 shows guards for the ADI "R" style SOIC package.

Note that for many single op amp devices in this SOIC "R" package, Pins 1, 5, and 8 are "no connect" pins. Historically these pins were used for offset adjustment and/or frequency compensation. These functions rarely are used in modern op amps. For such instances, this means that these empty locations can be employed in the layout to route guard traces. In the case of the inverting mode (left), the guarding is still completely effective, with the dummy Pin 1 and Pin 3 serving as the grounded guard trace. This is a fully effective guard without compromise. Also, with SOIC op amps, much of the circuitry around the device will not use through hole components. So, the guard ring may only be necessary on the op amp PCB side.

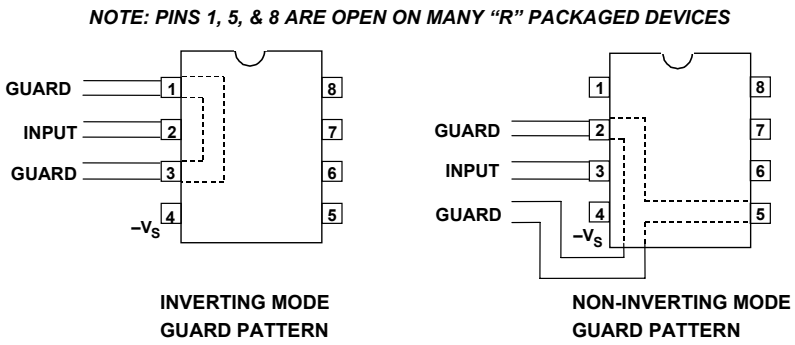



***Figure 12.16:*** *PCB Guard Patterns for Inverting and Noninverting Mode Op Amps Using Eight Pin SOIC (R) Package*

In the case of the follower stage (right), the guard trace must be routed around the negative supply at Pin 4, and thus Pin 4 to Pin 3 leakage isn't fully guarded. For this reason, a precision high impedance follower stage using an SOIC package op amp isn't generally recommended, as guarding isn't possible for dual supply connected devices.

However, an exception to this caveat does apply to the use of a *single-supply* op amp as a noninverting stage. For example, if the AD8551 is used, Pin 4 becomes ground, and some degree of intrinsic guarding is then established by default.

## Dynamic PCB Effects

Although static PCB effects can come and go with changes in humidity or board contamination, problems that most noticeably affect the dynamic performance of a circuit usually remain relatively constant. Short of a new design, washing or any other simple fixes can't fix them. As such, they can permanently and adversely affect a design's specifications and performance. The problems of stray capacitance, linked to lead and component placement, are reasonably well known to most circuit designers. Since lead placement can be permanently dealt with by correct layout, any remaining difficulty is solved by training assembly personnel to orient components or bend leads optimally.

Dielectric absorption (DA), on the other hand, represents a more troublesome and still poorly understood circuit-board phenomenon. Like DA in discrete capacitors, DA in a printed-circuit board can be modeled by a series resistor and capacitor connecting two closely spaced nodes. Its effect is inverse with spacing and linear with length.

As shown in Figure 12.17, the RC model for this effective capacitance ranges from 0.1 pF to 2.0 pF, with the resistance ranging from 50 MΩ to 500 MΩ. Values of 0.5 pF and 100 MΩ are most common. Consequently, circuit-board DA interacts most strongly with high impedance circuits.

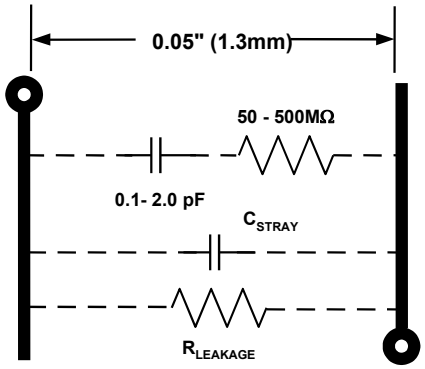



***Figure 12.17:*** *DA Plagues Dynamic Response of PCB-Based Circuits*

PCB DA most noticeably influences dynamic circuit response, for example, settling time. Unlike circuit leakage, the effects aren't usually linked to humidity or other environmental conditions, but rather, are a function of the board's dielectric properties. The chemistry involved in producing plated through holes seems to exacerbate the problem. If your circuits don't meet expected transient response specs, you should consider PCB DA as a possible cause.

Fortunately, there are solutions. As in the case of capacitor DA, external components can be used to compensate for the effect. More importantly, surface guards that totally isolate sensitive nodes from parasitic coupling often eliminate the problem (note that these guards should be duplicated on both sides of the board, in cases of through hole components). As noted previously, low loss PCB dielectrics are also available.

PCB "hook," similar if not identical to DA, is characterized by variation in effective circuit-board capacitance with frequency (see Reference 1). In general, it affects high impedance circuit transient response where board capacitance is an appreciable portion of the total in the circuit. Circuits operating at frequencies below 10 kHz are the most susceptible. As in circuit board DA, the board's chemical makeup very much influences its effects.

## Inductance

## Stray Inductance

All conductors are inductive, and at high frequencies, the inductance of even quite short pieces of wire or printed circuit traces may be important. The inductance of a straight wire of length L mm and circular cross-section with radius R mm in free space is given by the first equation shown in Figure 12.18.

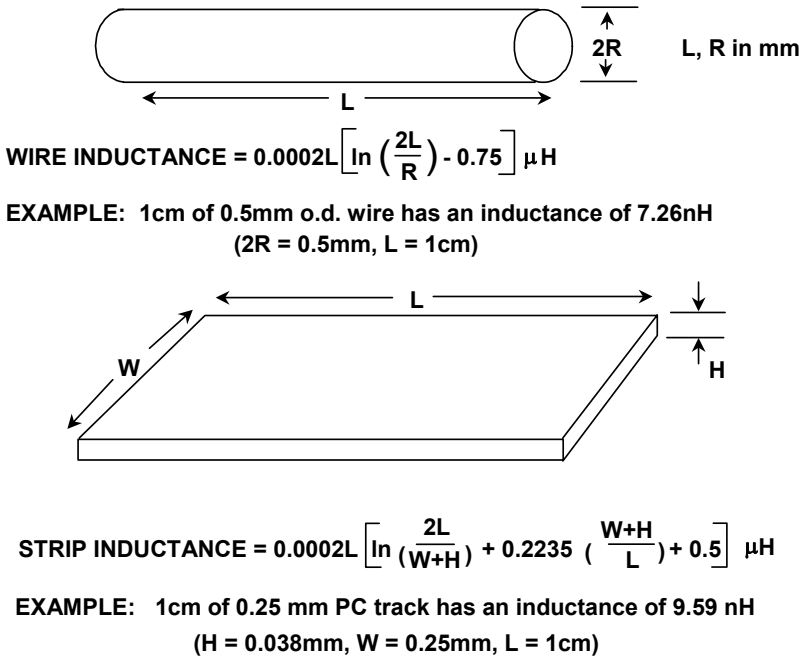



***Figure 12.18:*** *Wire and Strip Inductance Calculations*

The inductance of a strip conductor (an approximation to a PC track) of width W mm and thickness H mm in free space is also given by the second equation in Figure 12.18.

In real systems, these formulas both turn out to be approximate, but they do give some idea of the order of magnitude of inductance involved. They tell us that 1 cm of 0.5-mm of wire has an inductance of 7.26 nH, and 1 cm of 0.25-mm PC track has an inductance of 9.59 nH—these figures are reasonably close to measured results.

At 10 MHz, an inductance of 7.26 nH has an impedance of 0.46 Ω, and so can give rise to 1% error in a 50-Ω system.

## Mutual Inductance

Another consideration regarding inductance is the separation of outward and return currents. As we shall discuss in more detail later, Kirchoff's Law tells us that current flows in closed paths—there is always an outward and return path. The whole path forms a single turn inductor.

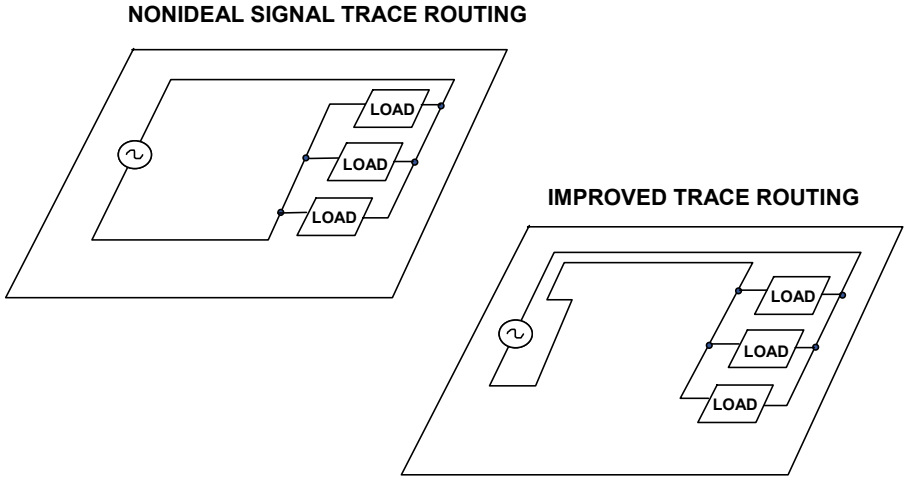
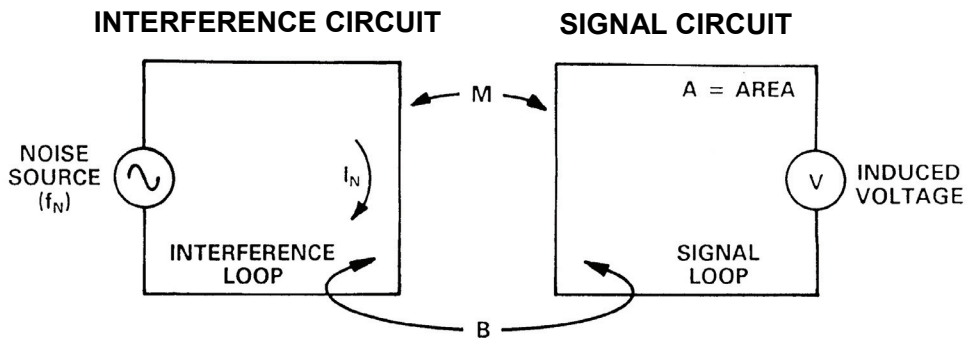



***Figure 12.19:*** *Nonideal and Improved Signal Trace Routing*

This principle is illustrated by the contrasting signal trace routing arrangements of Figure 9.10. If the area enclosed within the turn is relatively large, as in the upper "nonideal" picture, then the inductance (and hence the ac impedance) will also be large. On the other hand, if the outward and return paths are closer together, as in the lower "improved" picture, the inductance will be much smaller.

Note that the nonideal signal routing case of Figure 12.19 has other drawbacks—the large area enclosed within the conductors produces extensive external magnetic fields, which may interact with other circuits, causing unwanted coupling. Similarly, the large area is more vulnerable to interaction with external magnetic fields, which can induce unwanted signals in the loop.

The basic principle is illustrated in Figure 12.20, and is a common mechanism for the transfer of unwanted signals (noise) between two circuits.




**M = MUTUAL INDUCTANCE**
**B = MAGNETIC REFLUX DENSITY**
**A = AREA OF SIGNAL LOOP**
**$\omega_N = 2\pi f_N$ = FREQUENCY OF NOISE SOURCE**

**V = INDUCED VOLTAGE = $\omega_N M I_N = \omega AB$**

***Figure 12.20:*** *Basic Principles of Inductive Coupling*

As with most other noise sources, as soon as we define the working principle, we can see ways of reducing the effect. In this case, reducing any or all of the terms in the equations in Figure 12.20 reduces the coupling. Reducing the frequency or amplitude of the current causing the interference may be impracticable, but it is frequently possible to reduce the mutual inductance between the interfering and interfered with circuits by reducing loop areas on one or both sides and, possibly, increasing the distance between them.

A layout solution is illustrated by Figure 12.21. Here two circuits, shown as Z1 and Z2, are minimized for coupling by keeping each of the loop areas as small as is practical.

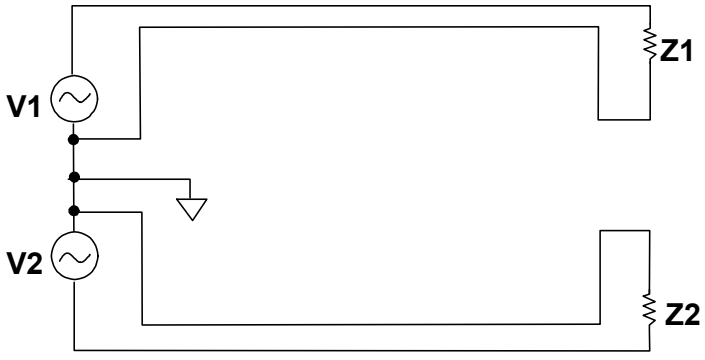
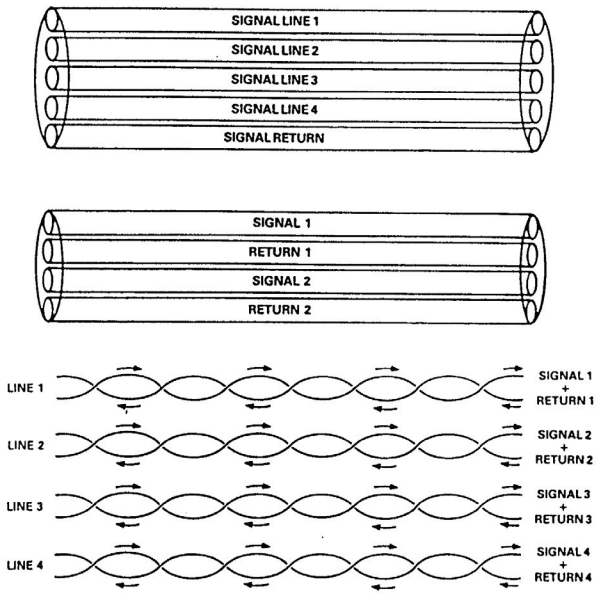



***Figure 12.21:*** *Proper Signal Routing and Layout Can Reduce Inductive Coupling*

As also illustrated in Figure 12.22, mutual inductance can be a problem in signals transmitted on cables. Mutual inductance is high in ribbon cables, especially when a single return is common to several signal circuits (top). Separate, dedicated signal and return lines for each signal circuit reduces the problem (middle). Using a cable with

twisted pairs for each signal circuit as in the bottom picture is even better (but is more expensive and often unnecessary).




- FLAT RIBBON CABLE WITH SINGLE RETURN HAS LARGE MUTUAL INDUCTANCE BETWEEN CIRCUITS
- SEPARATE AND ALTERNATE SIGNAL / RETURN LINES FOR EACH CIRCUIT REDUCES MUTUAL INDUCTANCE
- TWISTED PAIRS REDUCE MUTUAL INDUCTANCE STILL FURTHER

***Figure 12.22:*** *Mutual Inductance and Coupling Within Signal Cabling*

Shielding of magnetic fields to reduce mutual inductance is sometimes possible, but is by no means as easy as shielding an electric field with a Faraday shield (following section). HF magnetic fields are blocked by conductive material provided the skin depth in the conductor at the frequency to be screened is much less than the thickness of the conductor, and the screen has no holes (Faraday shields can tolerate small holes, magnetic screens cannot). LF and DC fields may be screened by a shield made of mu-metal sheet. Mu-metal is an alloy having very high permeability, but it is expensive, its magnetic properties are damaged by mechanical stress, and it will saturate if exposed to too high fields. Its use, therefore, should be avoided where possible.

## Parasitic Effects in Inductors

Although inductance is one of the fundamental properties of an electronic circuit, inductors are far less common as components than are resistors and capacitors. As for precision components, they are even more rare. This is because they are harder to manufacture, less stable, and less physically robust than resistors and capacitors. It is relatively easy to manufacture stable precision inductors with inductances from nH to tens or hundreds of μH, but larger valued devices tend to be less stable, and large.

As we might expect in these circumstances, circuits are designed, where possible, to avoid the use of precision inductors. We find that stable precision inductors are relatively rarely used in precision analog circuitry, except in tuned circuits for high frequency narrow-band applications.

Of course, they are widely used in power filters, switching power supplies and other applications where lack of precision is unimportant (more on this in a following section). The important features of inductors used in such applications are their current carrying and saturation characteristics, and their Q. If an inductor consists of a coil of wire with an air core, its inductance will be essentially unaffected by the current it is carrying. On the other hand, if it is wound on a core of a magnetic material (magnetic alloy or ferrite), its inductance will be nonlinear, since at high currents, the core will start to saturate. The effects of such saturation will reduce the efficiency of the circuitry employing the inductor and is liable to increase noise and harmonic generation.

As mentioned above, inductors and capacitors together form tuned circuits. Since all inductors will also have some stray capacity, all inductors will have a resonant frequency (which will normally be published on their data sheet), and should only be used as precision inductors at frequencies well below this.

## Q or "Quality Factor"

The other characteristic of inductors is their Q (or "Quality Factor"), which is the ratio of the reactive impedance to the resistance, as indicated in Figure 12.23.

- **$Q = 2\pi f L/R$**
- **The Q of an inductor or resonant circuit is a measure of the ratio of its reactance to its resistance.**
- **The resistance is the HF and NOT the DCvalue.**
- **The 3 dB bandwidth of a single tuned circuit is Fc/Q where Fc is the center frequency.**

***Figure 12.23:*** *Inductor Q or Quality Factor*

It is rarely possible to calculate the Q of an inductor from its dc resistance, since skin effect (and core losses if the inductor has a magnetic core) ensure that the Q of an inductor at high frequencies is always lower than that predicted from dc values.

Q is also a characteristic of tuned circuits (and of capacitors—but capacitors generally have such high Q values that it may be disregarded, in practice). The Q of a tuned circuit, which is generally very similar to the Q of its inductor (unless it is deliberately lowered by the use of an additional resistor), is a measure of its bandwidth around resonance. LC tuned circuits rarely have Q of much more than 100 (3 dB bandwidth of 1%), but ceramic resonators may have a Q of thousands, and quartz crystals tens of thousands.

## Don't Overlook Anything

Remember, if your precision op amp or data-converter-based design does not meet specification, try not to overlook anything in your efforts to find the error sources. Analyze both active *and* passive components, trying to identify and challenge any assumptions or preconceived notions that may blind you to the facts. Take nothing for granted.

For example, when not tied down to prevent motion, cable conductors, moving within their surrounding dielectrics, can create significant static charge buildups that cause errors, especially when connected to high impedance circuits. Rigid cables, or even costly low noise Teflon-insulated cables, are expensive alternative solutions.

As more and more high precision op amps become available, and system designs call for higher speed and increased accuracy, a thorough understanding of the error sources described in this section (as well those following) becomes more important.

Some additional discussions of passive components within a succeeding power supply filtering section complements this one. In addition, the very next section on PCB design issues also complements many points within this section. Similar comments apply to the chapter on EMI/RFI.

## Stray Capacitance

When two conductors aren't short-circuited together, or totally screened from each other by a conducting (Faraday) screen, there is a capacitance between them. So, on any PCB, there will be a large number of capacitors associated with any circuit (which may or may not be considered in models of the circuit). Where high frequency performance matters (and even dc and VLF circuits may use devices with high Ft and therefore be vulnerable to HF instability), it is very important to consider the effects of this stray capacitance.

Any basic textbook will provide formulas for the capacitance of parallel wires and other geometric configurations (see References 9 and 10). The example we need consider in this discussion is the parallel plate capacitor, often formed by conductors on opposite sides of a PCB. The basic diagram describing this capacitance is shown in Figure 12.24.

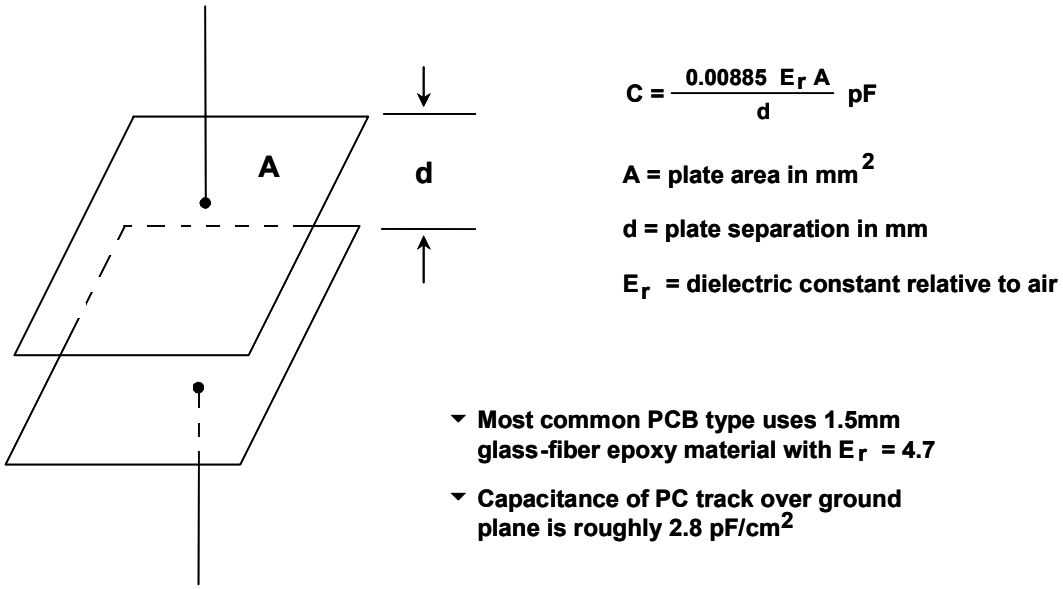



***Figure 12.24:*** *Capacitance of two parallel plates*

Neglecting edge effects, the capacitance of two parallel plates of area A $mm^2$ and separation d mm in a medium of dielectric constant $E_r$ relative to air is:

$$0.00885\ E_r\ A/d\ \text{pF}. \qquad \text{Eq. 12-1}$$

where:

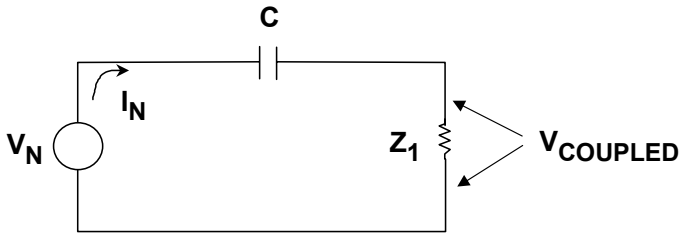
$E_r$ = the dielectric constant of the insulator material relative to air
$A$ = the plate area
$D$ = the distance between the plates

From this formula, we can calculate that for general purpose PCB material ($E_r$ = 4.7, d = 1.5 mm), the capacitance between conductors on opposite sides of the board is just under 3 $pF/cm^2$. In general, such capacitance will be parasitic, and circuits must be designed so that it does not affect their performance.

While it is possible to use PCB capacitance in place of small discrete capacitors, the dielectric properties of common PCB substrate materials cause such capacitors to behave poorly. They have a rather high temperature coefficient and poor Q at high frequencies, which makes them unsuitable for many applications. Boards made with lower loss dielectrics such as Teflon are expensive exceptions to this rule.

### Capacitive Noise & Faraday Shields

There is a capacitance between any two conductors separated by a dielectric (air or vacuum are dielectrics). If there is a change of voltage on one, there will be a movement of charge on the other. A basic model for this is shown in Figure 12.25.




$Z_1$ = CIRCUIT IMPEDANCE
Z2 = 1/jωC

$$V_{COUPLED} = V_N \left( \frac{Z_1}{Z_1 + Z_2} \right)$$

***Figure 12.25:*** *Capacitive Coupling Equivalent Circuit Model*

It is evident that the noise voltage, $V_{COUPLED}$ appearing across $Z_1$, may be reduced by several means, all of which reduce noise current in $Z_1$. They are reduction of the signal voltage $V_N$, reduction of the frequency involved, reduction of the capacitance, or reduction of $Z_1$ itself. Unfortunately however, often none of these circuit parameters can be freely changed, and an alternate method is needed to minimize the interference. The best solution towards reducing the noise coupling effect of C is to insert a grounded conductor, also known as a *Faraday shield*, between the noise source and the affected circuit. This has the desirable effect of reducing $Z_1$ noise current, thus reducing $V_{COUPLED}$.

A Faraday shield model is shown by Figure 12.26. In the left picture, the function of the shield is noted by how it effectively divides the coupling capacitance, C. In the right picture the net effect on the coupled voltage across $Z_1$ is shown. Although the noise current $I_N$ still flows in the shield, most of it is now diverted away from $Z_1$. As a result, the coupled noise voltage $V_{COUPLED}$ across $Z_1$ is reduced.

A Faraday shield is easily implemented and almost always successful. Thus capacitively coupled noise is rarely an intractable problem. However, to be fully effective, a Faraday

shield must completely block the electric field between the noise source and the shielded circuit. It must also be connected so that the displacement current returns to its source, without flowing in any part of the circuit where it can introduce conducted noise.

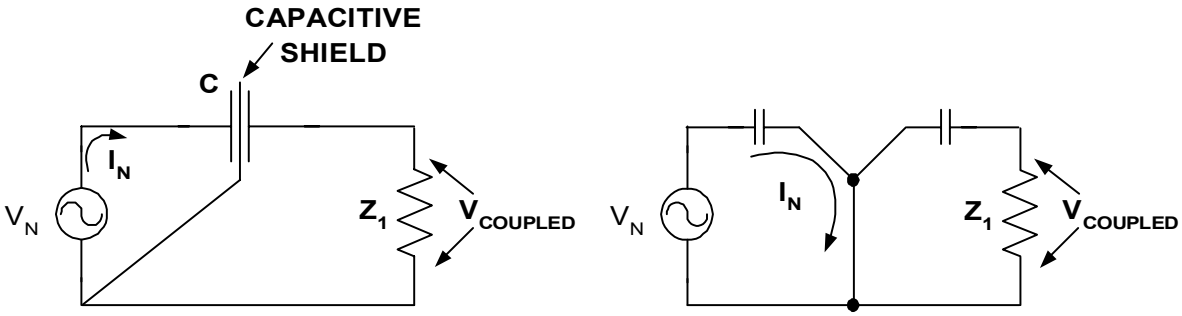



***Figure 12.26:*** *An Operational Model of a Faraday Shield*

## Buffering ADCs Against Logic Noise

If we have a high resolution data converter (ADC or DAC) connected to a high speed data bus which carries logic noise with a 2 V/ns to 5 V/ns edge rate, this noise is easily connected to the converter analog port via stray capacitance across the device. Whenever the data bus is active, intolerable amounts of noise are capacitively coupled into the analog port, thus seriously degrading performance.

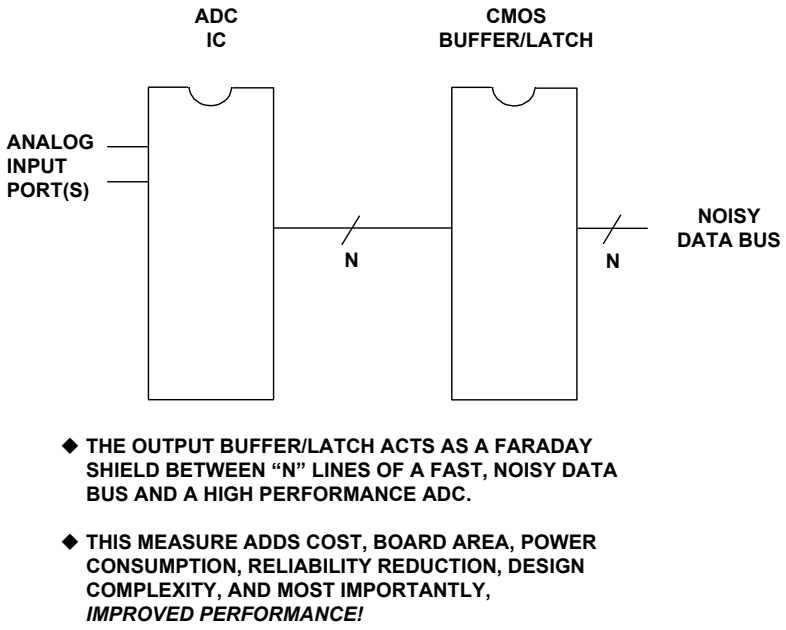



***Figure 12.27:*** *A High Speed ADC IC Sitting on a Fast Data Bus Couples Digital Noise into the Analog Port, thus Limiting Performance*

This particular effect is illustrated by the diagram of Figure 12.27, where multiple package capacitors couple noisy edge signals from the data bus into the analog input of an ADC.

Present technology offers no cure for this problem, within the affected IC device itself. The problem also limits performance possible from other broadband monolithic mixed signal ICs with single chip analog and digital circuits. Fortunately, this coupled noise problem can be simply avoided, by *not* connecting the data bus directly to the converter.

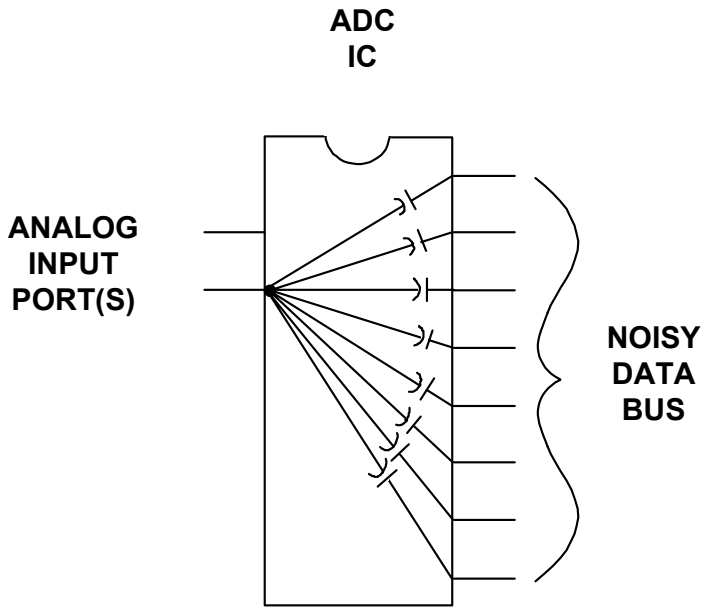



***Figure 12.28:*** *A High Speed ADC IC Using a CMOS Buffer/Latch at the Output Shows Enhanced Immunity of Digital Data Bus Noise*

Instead, *use a CMOS latched buffer as a converter-to-bus interface*, as shown by Figure 12.28. Now the CMOS buffer IC acts as a Faraday shield, and dramatically reduces noise coupling from the digital bus. This solution costs money, occupies board area, reduces reliability (very slightly), consumes power, and it complicates the design—but it does improve the signal-to-noise ratio of the converter! The designer must decide whether it is worthwhile for individual cases, but in general it is highly recommended.

## High Circuit Impedances are Susceptible to Noise Pickup

Since low power circuits tend to use high value resistors to conserve power, this tends to make the circuit more susceptible to externally induced radiated noise and conducted noise. Even a small amount of parasitic capacitance can create a significant conduction path for noise to penetrate.

For example, as little as 1 pF of parasitic capacitance allows a 5 V logic transition to cause a large disturbance in a 100 kΩ circuit as illustrated in Figure 12.29

This serves to illustrate that high impedance circuits are full of potential parasitics which can cause a good paper design to perform poorly when actually implemented. One needs to pay particular attention to the routing of signals. Interestingly, many high frequency layout techniques for eliminating parasitics can also be applied here for low frequency, low power circuits—for different reasons. While circuit parasitics cause unwanted phase shifts and instabilities in high frequency circuits, the same parasitics pick up unwanted noise in low power precision circuits.

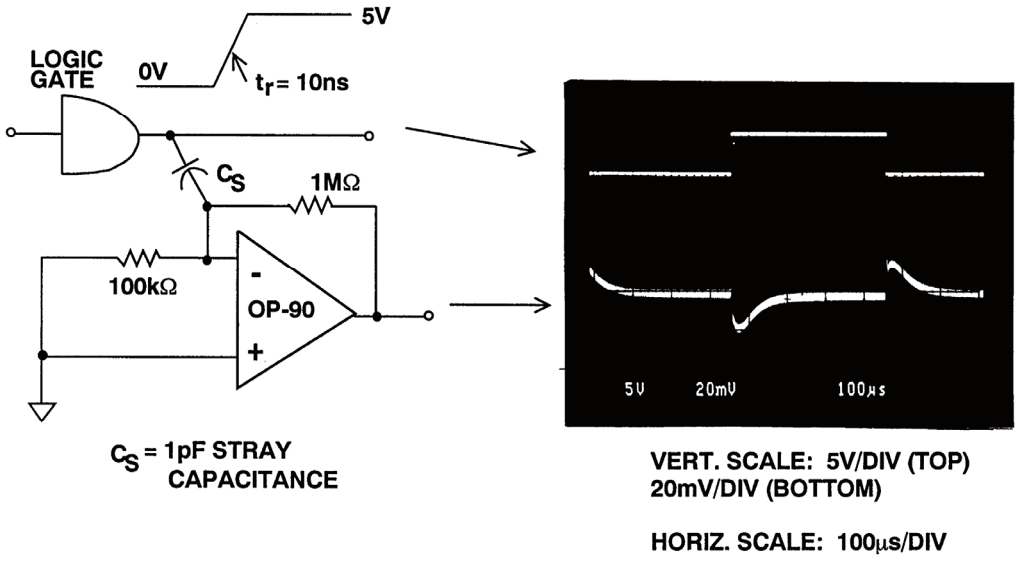



***Figure 12.29*** *High Circuit Impedances Increase Susceptibility to Noise Pickup*

As discussed in the chapter on amplifiers, current feedback amplifiers do not like to have capacitances on their inputs. To that end, ground planes should be cut back from the input pins as shown in Fig. 12.30, which is an evaluation board for the AD8001 high speed current feedback amplifier. The effect of even small capacitance on the input of a current feedback amplifier is shown in Fig. 12.31. Note the ringing on the output.

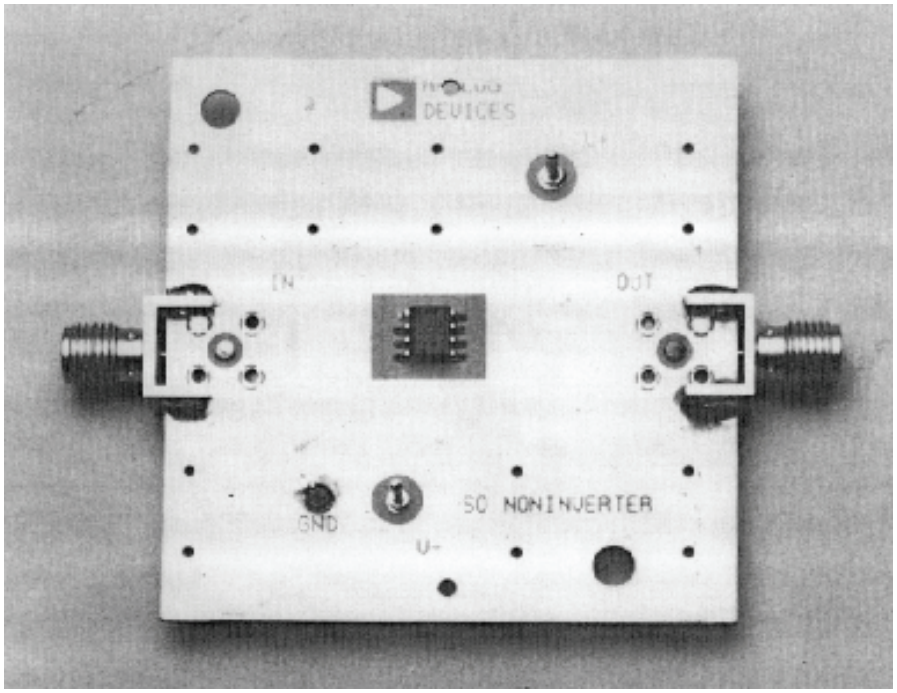



***Fig. 12.30a:*** *AD8001AR (SOIC) Evaluation Board—Top View*

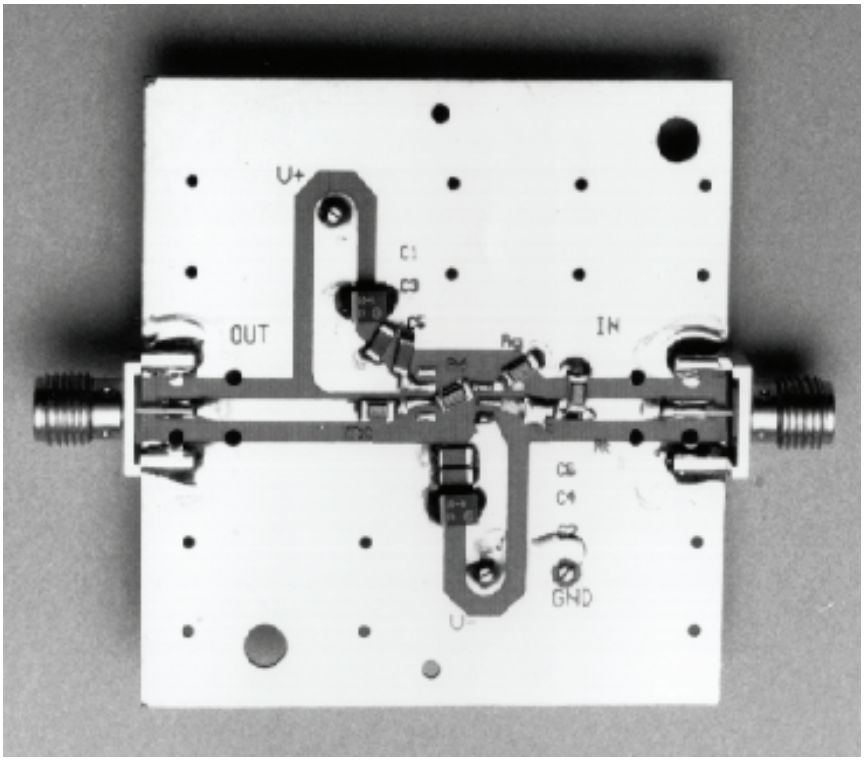



***Fig. 12.30b:*** *AD8001AR (SOIC) Evaluation Board—Bottom View*

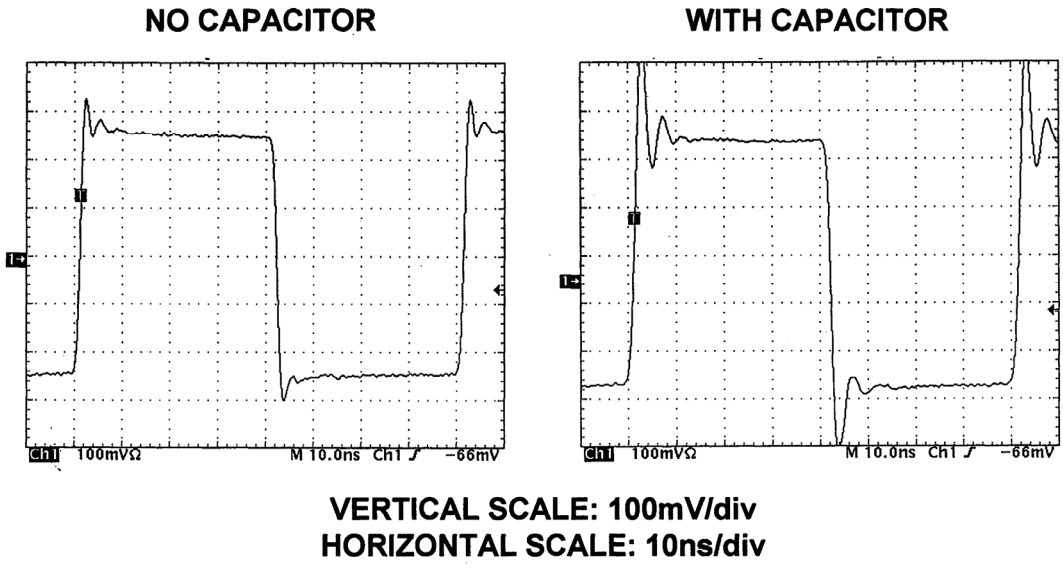



***Figure 12.31:*** *Effects of 10 pF Stray Capacitance on the Inverting Input on Amplifier (AD8001) Pulse Response*

## Skin Effect

At high frequencies, also consider *skin effect*, where inductive effects cause currents to flow only in the outer surface of conductors. Note that this is in contrast to the earlier discussions of this section on dc resistance of conductors.

The skin effect has the consequence of increasing the resistance of a conductor at high frequencies. Note also that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased.

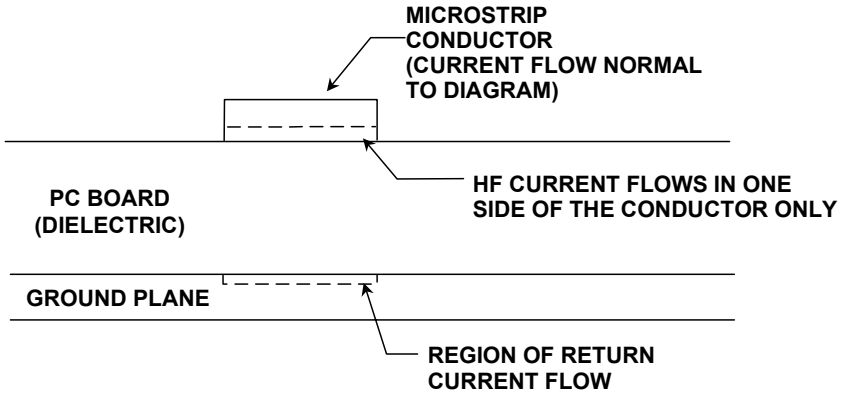



***Figure 12.32:*** *Skin Depth in a PCB Conductor*

Skin effect is quite a complex phenomenon, and detailed calculations are beyond the scope of this discussion. However, a good approximation for copper is that the skin depth in centimeters is $6.61/\sqrt{f}$, (f in Hz). A summary of the skin effect within a typical PCB conductor foil is shown in Figure 12.32. Note that this copper conductor cross-sectional view assumes looking into the *side* of the conducting trace. Assuming that skin effects become important when the skin depth is less than 50% of the thickness of the conductor, this tells us that for a typical PC foil, we must be concerned about skin effects at frequencies above approximately 12 MHz.

Where skin effect is important, the resistance for copper is $2.6 \times 10^{-7} \sqrt{f}\ \Omega$/square, (f in Hz). This formula is invalid if the skin thickness is greater than the conductor thickness (i.e., at dc or LF).

Figure 12.33 illustrates a case of a PCB conductor with current flow, as separated from the ground plane underneath.

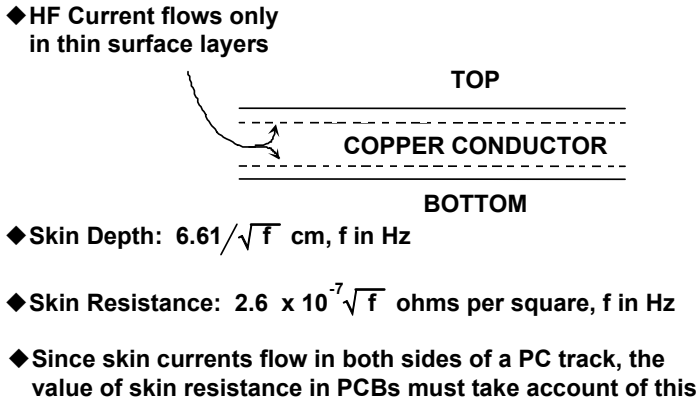



***Figure 12.33:*** *Skin Effect with PCB Conductor and Ground Plane*

In this diagram, note the (dotted) regions of HF current flow, as reduced by the skin effect. When calculating skin effect in PCBs, it is important to remember that current generally flows in both sides of the PC foil (this is not necessarily the case in microstrip lines, see below), so the resistance per square of PC foil may be half the above value.

## Transmission Lines

We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. As shown previously in Figure 7-30, when an HF signal flows in a PC track running over a ground plane, the arrangement functions as a *microstrip* transmission line, and the majority of the return current flows in the ground plane directly underneath the line.

Figure 12.34 shows the general parameters for a microstrip transmission line, given the conductor width, w, dielectric thickness, h, and the dielectric constant, $E_r$.

The characteristic impedance of such a microstrip line will depend upon the width of the track and the thickness and dielectric constant of the PCB material. Designs of microstrip lines are covered in more detail later in this chapter.

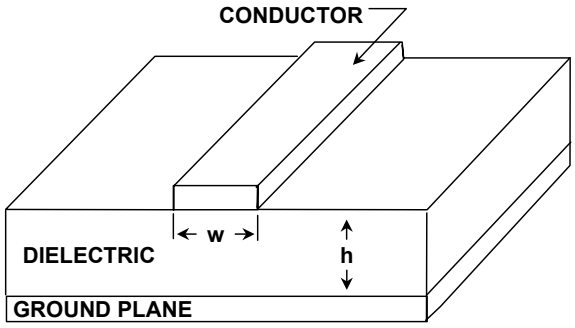



***Figure 12.34:*** *A PCB Microstrip Transmission Line Is an Example of a Controlled Impedance Conductor Pair*

For most dc and lower frequency applications, the characteristic impedance of PCB traces will be relatively unimportant. Even at frequencies where a track over a ground plane behaves as a transmission line, it is not necessary to worry about its characteristic impedance or proper termination if the free space wavelengths of the frequencies of interest are greater than ten times the length of the line.

However, at VHF and higher frequencies it is possible to use PCB tracks as microstrip lines within properly terminated transmission systems. Typically the microstrip will be designed to match standard coaxial cable impedances, such as 50 Ω, 75 Ω, or 100 Ω, simplifying interfacing.

Note that if losses in such systems are to be minimized, the PCB material must be chosen for low/high frequency losses. This usually means the use of Teflon or some other comparably low-loss PCB material. Often, though, the losses in short lines on cheap glass-fiber board are small enough to be quite acceptable.

## Design PCBs Thoughtfully

Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution. Critical signal paths should be routed by hand, to avoid undesired coupling and/or emissions.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to RF fields, by a factor of 10 or more, compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes, nor analog and digital power planes.

## Designing Controlled Impedances Traces on PCBs

A variety of trace geometries are possible with controlled impedance designs, and they may be either integral to or allied to the PCB pattern. In the discussions below, the basic patterns follow those of the IPC, as described in standard 2141 (see Reference 16).

Note that the figures below use the term "ground plane." It should be understood that this plane is in fact a large area, low impedance *reference* plane. In practice it may actually be either a ground plane or a power plane, both of which are assumed to be at zero ac potential.

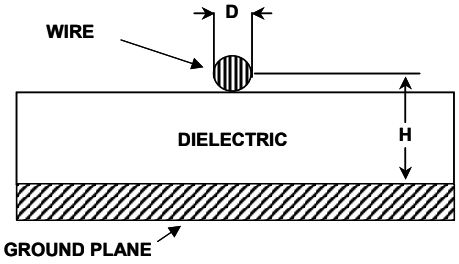



***Figure 12.35:*** *A Wire Microstrip Transmission Line With Defined Impedance is Formed by an Insulated Wire Spaced From a Ground Plane*

The first of these is the simple wire-over-a-plane form of transmission line, also called a *wire microstrip*. A cross-sectional view is shown in Figure 12.35. This type of transmission line might be a signal wire used within a breadboard, for example. It is

composed simply of a discrete insulated wire spaced a fixed distance over a ground plane. The dielectric would be either the insulation wall of the wire, or a combination of this insulation and air.

The impedance of this line in ohms can be estimated with Eq. 12-2.

$$Z_O(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4H}{D}\right] . \qquad \text{Eq. 12-2}$$

where:

$D$ = the conductor diameter
$H$ = the wire spacing above the plane
$\varepsilon_r$ = the dielectric constant of the material relative to air.

For patterns integral to the PCB, there are a variety of geometric models from which to choose, single-ended and differential. These are covered in some detail within IPC standard 2141 (see Reference 16), but information on two popular examples is shown here.

Before beginning any PCB-based transmission line design, it should be understood that there are abundant equations, all claiming to cover such designs. In this context, "Which of these are accurate?" is an extremely pertinent question. The unfortunate answer is, *none are perfectly so!* All of the existing equations are approximations, and thus accurate to varying degrees, depending upon specifics. The best known and most widely quoted equations are those of Reference 16, but even these come with application caveats.

Reference 17 has evaluated the Reference 16 equations for various geometric patterns against test PCB samples, finding that predicted accuracy varies according to target impedance. Reference 18 also evaluates the Reference 16 equations, offering an alternative and even more complex set (see Reference 19). The equations quoted below are from Reference 16, and are offered here as a starting point for a design, subject to further analysis, testing and design verification. The bottom line is, study carefully, and take PCB trace impedance equations with a proper dose of salt.

## Microstrip PCB Transmission Lines

For a simple two-sided PCB design where one side is a ground plane, a signal trace on the other side can be designed for controlled impedance. This geometry is known as a *surface microstrip,* or more simply, *microstrip*.

A cross-sectional view of a two-layer PCB illustrates this microstrip geometry as shown in Figure 12.36.

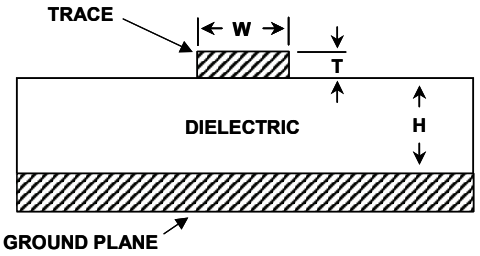



***Figure 12.36:*** *A Microstrip Transmission Line with Defined Impedance Is Formed by a PCB Trace of Appropriate Geometry, Spaced from a Ground Plane*

For a given PCB laminate and copper weight, note that all parameters will be predetermined except for W, the width of the signal trace. Eq. 12-3 can then be used to design a PCB trace to match the impedance required by the circuit. For the signal trace of width W and thickness T, separated by distance H from a ground (or power) plane by a PCB dielectric with dielectric constant $\varepsilon_r$, the characteristic impedance is:

$$Z_o(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{(0.8W + T)}\right] \qquad \text{Eq. 12-3}$$

Note that in these expressions, measurements are in common dimensions (mils).

These transmission lines will have not only a characteristic impedance, but also capacitance. This can be calculated in terms of pF/in as shown in Eq. 12-4.

$$C_o(\text{pF/in}) = \frac{0.67(\varepsilon_r + 1.41)}{\ln[5.98H/(0.8W + T)]} \qquad \text{Eq. 12-4}$$

As an example including these calculations, a 2-layer board might use 20-mil wide (W), 1 ounce (T = 1.4) copper traces separated by 10-mil (H) FR-4 ($\varepsilon$ = 4.0) dielectric material. The resulting impedance for this microstrip would be about 50 Ω. For other standard impedances, for example the 75 Ω video standard, adjust "W" to about 8.3 mils.

## Some Microstrip Guidelines

This example touches an interesting and quite handy point. Reference 17 discusses a useful guideline pertaining to microstrip PCB impedance. For a case of dielectric constant of 4.0 (FR-4), it turns out that when W/H is 2/1, the resulting impedance will be close to 50 Ω (as in the first example, with W=20 mils).

Careful readers will note that Eq. 9.21 predicts $Z_o$ to be about 46 Ω, generally consistent with accuracy quoted in Reference 17 (>5%). The IPC microstrip equation is most accurate between 50 Ω and 100 Ω, but is substantially less so for lower (or higher) impedances. Reference 20 gives tabular results of various PCB industry impedance calculator tools.

The propagation delay of the microstrip line can also be calculated, as per Eq. 12-5. This is the one-way transit time for a microstrip signal trace. Interestingly, for a given geometry model, *the delay constant in ns/ft is a function only of the dielectric constant, and not the trace dimensions* (see Reference 21). Note that this is quite a convenient situation. It means that, with a given PCB laminate (and given $\varepsilon_r$), the propagation delay constant is fixed for various impedance lines.

$$t_{pd}\left(\text{ns/ft}\right) = 1.017\sqrt{0.475\,\varepsilon_r + 0.67} \qquad \text{Eq. 12-5}$$

This delay constant can also be expressed in terms of ps/in, a form which will be more practical for smaller PCBs. This is:

$$t_{pd}\left(\text{ps/in}\right) = 85\sqrt{0.475\,\varepsilon_r + 0.67} \qquad \text{Eq. 12.6}$$

Thus for an example PCB dielectric constant of 4.0, it can be noted that a microstrip's delay constant is about 1.63 ns/ft, or 136 ps/in. These two additional guidelines can be useful in designing the timing of signals across PCB trace runs.

## Symmetric Stripline PCB Transmission Lines

A method of PCB design preferred from many viewpoints is a multilayer PCB. This arrangement *embeds* the signal trace between a power and a ground plane, as shown in the cross-sectional view of Figure 9.142. The low impedance ac-ground planes and the embedded signal trace form a *symmetric stripline* transmission line.

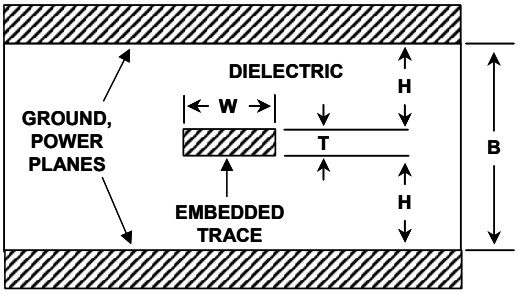



***Figure 12.37:*** *A Symmetric Stripline Transmission Line With Defined Impedance is Formed by a PCB Trace of Appropriate Geometry Embedded Between Equally Spaced Ground and/or Power Planes*

As can be noted from the figure, the return current path for a high frequency signal trace is located directly above and below the signal trace on the ground/power planes. The high frequency signal is thus contained entirely inside the PCB, minimizing emissions, and providing natural shielding against incoming spurious signals.

The characteristic impedance of this arrangement is again dependent upon geometry and the $\varepsilon_r$ of the PCB dielectric. An expression for $Z_O$ of the stripline transmission line is:

$$Z_O(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(B)}{(0.8W + T)}\right]. \qquad \text{Eq. 12.7}$$

Here, all dimensions are again in mils, and B is the spacing between the two planes. In this symmetric geometry, note that B is also equal to 2H + T. Reference 17 indicates that the accuracy of this Reference 16 equation is typically on the order of 6%.

Another handy guideline for the symmetric stripline in an $\varepsilon_r = 4.0$ case is to make B a multiple of W, in the range of 2 to 2.2. This will result in an stripline impedance of about 50 Ω. Of course this rule is based on a further approximation, by neglecting T. Nevertheless, it is still useful for ballpark estimates.

The symmetric stripline also has a characteristic capacitance, which can be calculated in terms of pF/in:

$$C_o\left(\text{pF/in}\right) = \frac{1.41\left(\varepsilon_r\right)}{\ln\left[3.81H/\left(0.8W + T\right)\right]} \qquad \text{Eq. 12-8}$$

The propagation delay of the symmetric stripline is shown in Eq. 12-9.

$$t_{pd}\left(\text{ns/ft}\right) = 1.017\sqrt{\varepsilon_r} \qquad \text{Eq. 12-9}$$

or, in terms of ps:

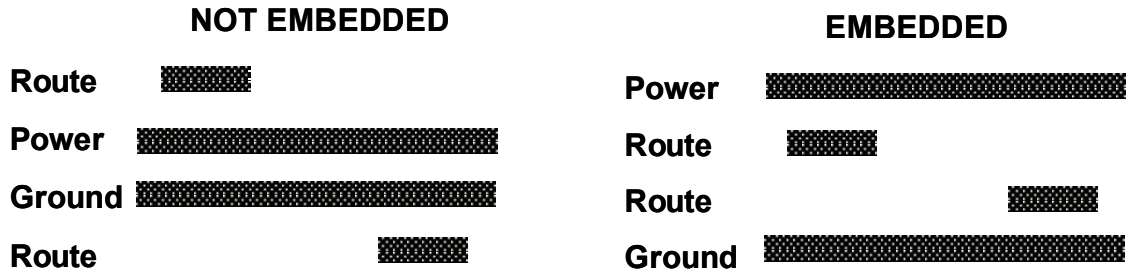
$$t_{pd}\left(\text{ps/in}\right) = 85\sqrt{\varepsilon_r} \qquad \text{Eq. 12-10}$$

For a PCB dielectric constant of 4.0, it can be noted that the symmetric stripline's delay constant is almost exactly 2 ns/ft, or 170 ps/in.

## Some Pros and Cons of Embedding Traces

The above discussions allow the design of PCB traces of defined impedance, either on a surface layer or embedded between layers. There of course are many other considerations beyond these impedance issues.

Embedded signals do have one major and obvious disadvantage—the debugging of the hidden circuit traces is difficult to impossible. Some of the pros and cons of embedded signal traces are summarized in Figure 12.38.




- **Advantages**
  - **Signal traces shielded and protected**
  - **Lower impedance, thus lower emissions and crosstalk**
  - **Significant improvement > 50MHz**
- **Disadvantages**
  - **Difficult prototyping and troubleshooting**
  - **Decoupling may be more difficult**
  - **Impedance may be too low for easy matching**

***Figure 12.38:*** *The Pros and Cons of Not Embedding vs. Embedding of Signal Traces in Multilayer PCB Designs*

Multilayer PCBs can be designed *without* the use of embedded traces, as is shown in the left-most cross-sectional example. This embedded case could be considered as a doubled two layer PCB design (i.e., four copper layers overall). The routed traces at the top form a microstrip with the power plane, while the traces at the bottom form a microstrip with the ground plane. In this example, the signal traces of both outer layers are readily accessible for measurement and troubleshooting purposes. But, the arrangement does nothing to take advantage of the shielding properties of the planes.

This nonembedded arrangement will have greater emissions and susceptibility to external signals, vis-à-vis the embedded case at the right, which uses the embedding, and does take full advantage of the planes. As in many other engineering efforts, the decision of embedded vs. nonembedded for the PCB design becomes a tradeoff, in this case one of reduced emissions vs. ease of testing.

## Dealing with High Speed Logic

Much has been written about terminating PCB traces in their characteristic impedance, to avoid signal reflections. A good guideline to determine when this is necessary is as follows: *Terminate the transmission line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster*). For example, a 2 inch microstrip line over an $E_r$ = 4.0 dielectric would have a delay of ~270 ps. Using the above rule strictly, termination would be appropriate whenever the signal rise time is < ~500 ps. A more conservative rule is to use a 2 inch (PCB track length)/nanosecond (rise/fall time) rule. If the signal trace exceeds this trace-length/speed criterion, then termination should be used.

For example, PCB tracks for high speed logic with rise/fall time of 5 ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (where measured length *includes* meanders).

As an example of what can be expected today in modern systems, Figure 12.39 shows typical rise/fall times for several logic families including the SHARC DSPs operating on +3.3V supplies. As would be expected, the rise/fall times are a function of load capacitance.

- **GaAs: 0.1ns**
- **ECL: 0.75ns**
- **ADI SHARC DSPs: 0.5ns TO 1ns (OPERATING ON +3.3V SUPPLY)**

**ASDP-21060l SHARC:**

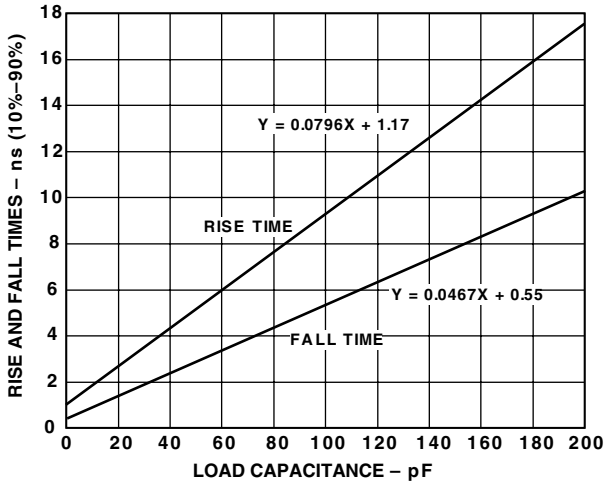



***Figure 12.39:*** *Typical DSP Output Rise Times and Fall Times*

In the analog domain, it is important to note that this same 2 inch/nanosecond rule of thumb should also be used with op amps and other circuits, to determine the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of $f_{max}$, then the equivalent rise time $t_r$ is related to this $f_{max}$. This limiting rise time, $t_r$, can be calculated as:

$$t_r = 0.35/f_{max} \qquad \text{Eq. 12-11}$$

The maximum PCB track length is then calculated by multiplying $t_r$ by 2 inch/nanosecond. For example, a maximum frequency of 100 MHz corresponds to a rise time of 3.5 ns, so a 7-inch or more track carrying this signal should be treated as a transmission line.

The best ways to keep sensitive analog circuits from being affected by fast logic are to physically separate the two by the PCB layout, and to use no faster logic family than is dictated by system requirements. In some cases, this may require the use of several logic families in a system. An alternative is to use series resistance or ferrite beads to slow down the logic transitions where highest speed isn't required. Figure 12.40 shows two methods.

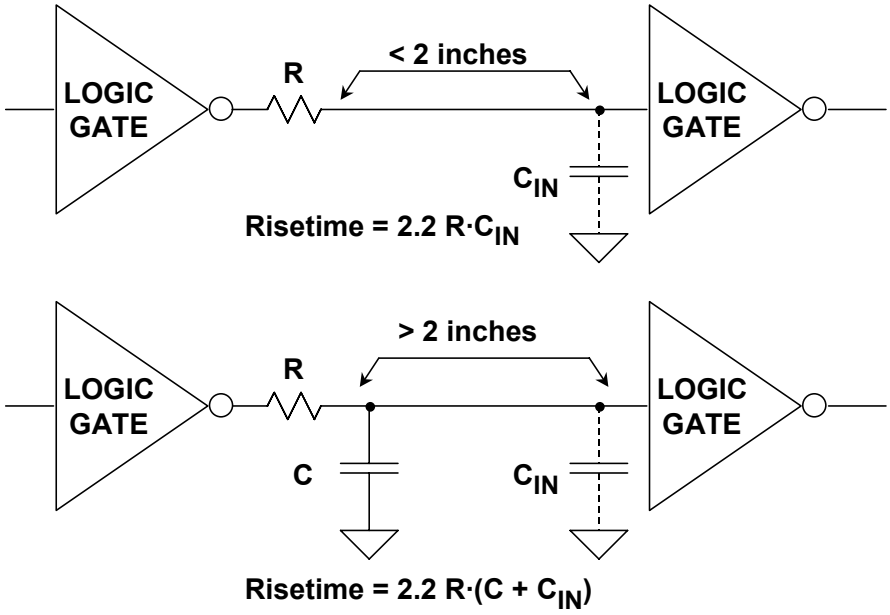



***Figure 12.40:*** *Damping Resistors Slow Down Fast Logic Edges to Minimize EMI/RFI Problems*

In the first, the series resistance and the input capacitance of the gate form a low-pass filter. Typical CMOS input capacitance is 5 pF to10 pF. Locate the series resistor close to the driving gate. The resistor minimizes transient currents and may eliminate the necessity of using transmission line techniques. The value of the resistor should be chosen such that the rise and fall times at the receiving gate are fast enough to meet system requirement, but no faster. Also, make sure that the resistor is not so large that the logic levels at the receiver are out of specification because of the voltage drop caused by the source and sink current which flow through the resistor. The second method is suitable for longer distances (>2 inches), where additional capacitance is added to slow down the edge speed. Notice that either one of these techniques increases delay and increases the rise/fall time of the original signal. This must be considered with respect to the overall timing budget, and the additional delay may not be acceptable.

Figure 12.41 shows a situation where several DSPs must connect to a single point, as would be the case when using read or write strobes bidirectionally connected from several DSPs. Small damping resistors shown in Figure 12.41A can minimize ringing provided the length of separation is less than about 2 inches. This method will also increase rise/fall times and propagation delay. If two groups of processors must be connected, a single resistor between the pairs of processors as shown in Figure 12.41B can serve to damp out ringing.

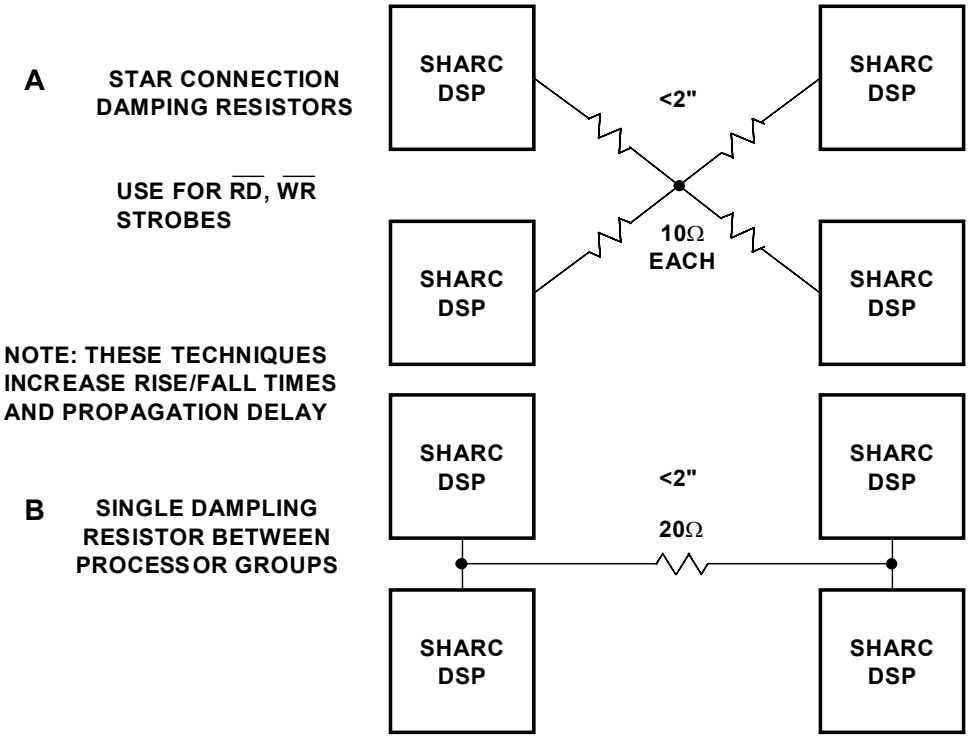



***Figure 12.41:*** *Series Damping Resistors for High Speed DSP Interconnections*

The only way to preserve 1 ns or less rise/fall times over distances greater than about 2 inches without ringing is to use transmission line techniques. Figure 12.42 shows two popular methods of termination: end termination and source termination. The end termination method (Figure 12.42A) terminates the cable at its terminating point in the characteristic impedance of the microstrip transmission line. Although higher impedances can be used, 50 Ω is popular because it minimizes the effects of the termination impedance mismatch due to the input capacitance of the terminating gate (usually 5 pF to 10 pF).

In Figure 12.42A, the cable is terminated in a Thevenin impedance of 50 Ω terminated to +1.4 V (the midpoint of the input logic threshold of 0.8 V and 2.0 V). This requires two resistors (91 Ω and 120 Ω), which add about 50 mW to the total quiescent power dissipation to the circuit. Figure 12.42A also shows the resistor values for terminating with a +5 V supply (68 Ω and 180 Ω). Note that 3.3-V logic is much more desirable in line driver applications because of its symmetrical voltage swing, faster speed, and lower power. Drivers are available with less than 0.5 ns time skew, source, and sink current

capability greater than 25 mA, and rise/fall times of about 1 ns. Switching noise generated by 3.3 V logic is generally less than 5 V logic because of the reduced signal swings and lower transient currents.

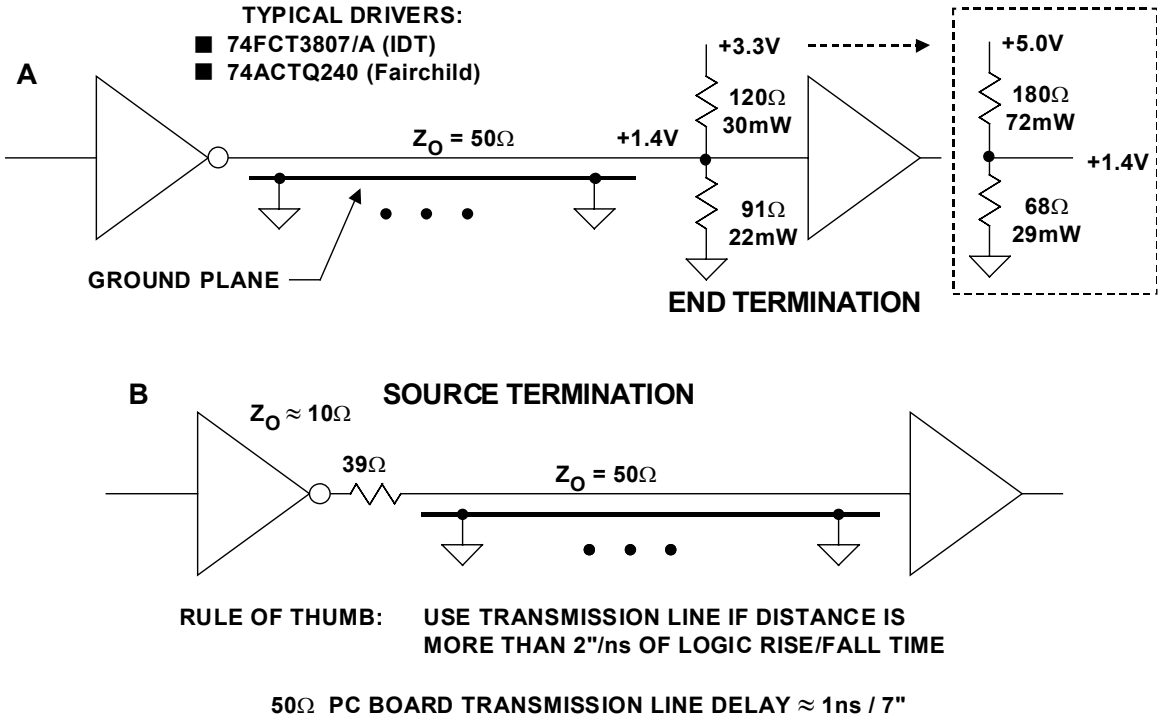



***Figure 12.42:*** *Termination Techniques for Controlled Impedance Microstrip Transmission Lines*

The source termination method, shown in Figure 12.42B, absorbs the reflected waveform with an impedance equal to that of the transmission line. This requires about 39 Ω in series with the internal output impedance of the driver, which is generally about 10 Ω. This technique requires that the end of the transmission line be terminated in an open circuit, therefore no additional fanout is allowed. The source termination method adds no additional quiescent power dissipation to the circuit.

Figure 12.43 shows a method for distributing a high speed clock to several devices. The problem with this approach is that there is a small amount of time skew between the clocks because of the propagation delay of the microstrip line (approximately 1 ns /7"). This time skew may be critical in some applications. It is important to keep the stub length to each device less than 0.5" in order to prevent mismatches along the transmission line.

The clock distribution method shown in Figure 12.44 minimizes the clock skew to the receiving devices by using source terminations and making certain the length of each microstrip line is equal. There is no extra quiescent power dissipation as would be the case using end termination resistors.

Figure 12.45 shows how source terminations can be used in bidirectional link port transmissions between SHARC DSPs. The output impedance of the SHARC driver is approximately 17 Ω, and therefore a 33 Ω series resistor is required on each end of the transmission line for proper source termination.

The method shown in Figure 12.46 can be used for bidirectional transmission of signals from several sources over a relatively long transmission line. In this case, the line is terminated at both ends, resulting in a dc load impedance of 25 Ω. SHARC drivers are capable of driving this load to valid logic levels.

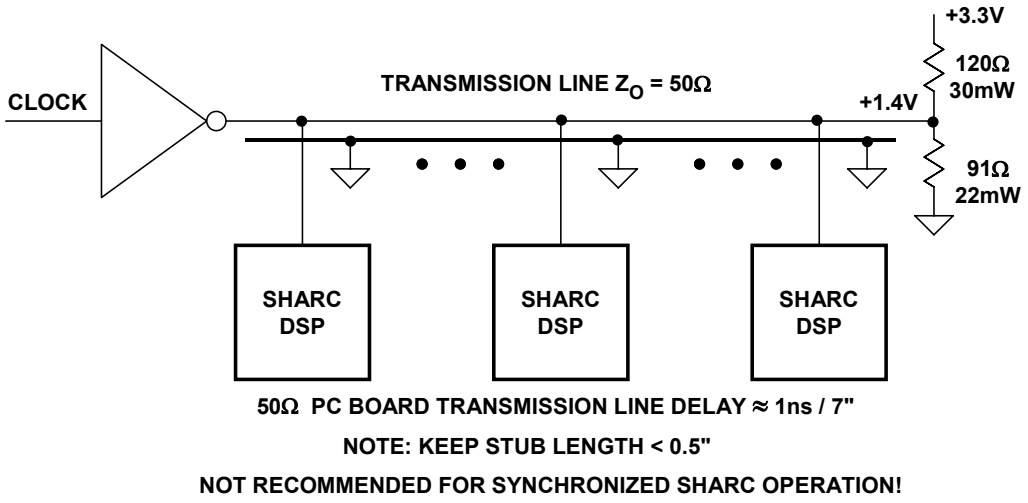



***Figure 12.43:*** *Clock Distribution Using End-of-Line Termination*

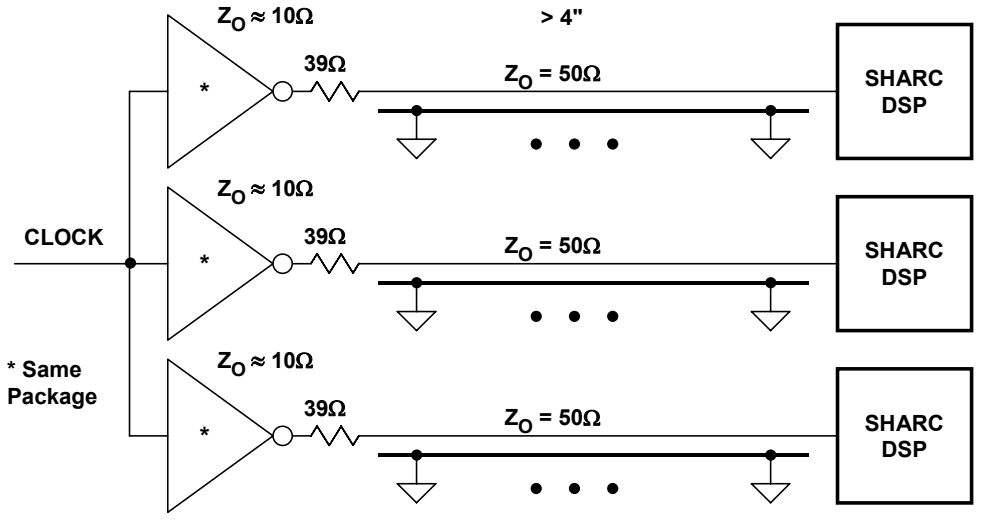



***Figure 12.44:*** *Preferred Method of Clock Distribution Using Source Terminated Transmission Lines*

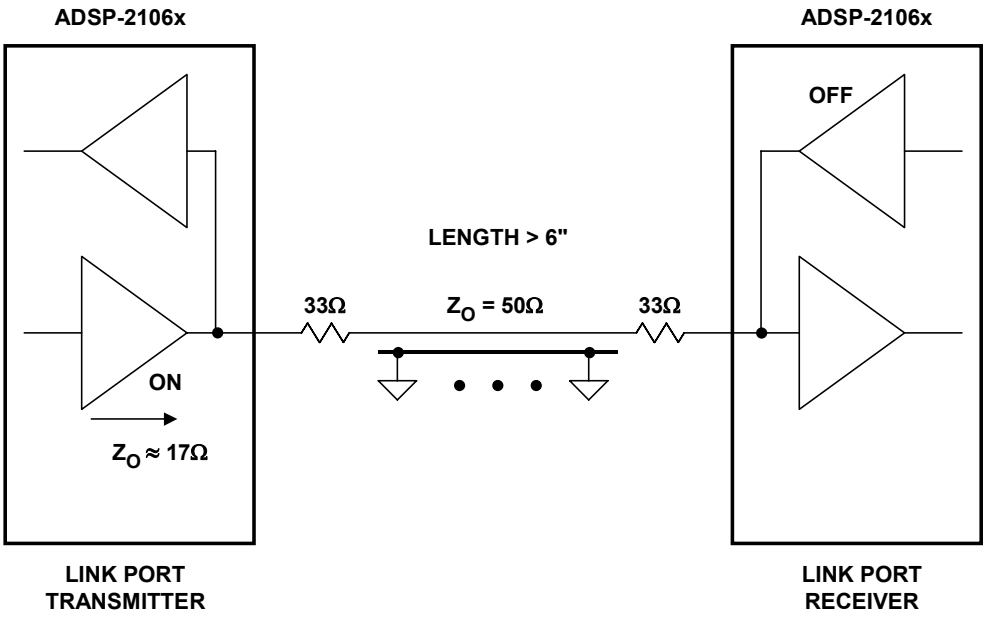



***Figure 12.45:*** *Source Termination for Biirectional Transmission Between SHARC DSPs*

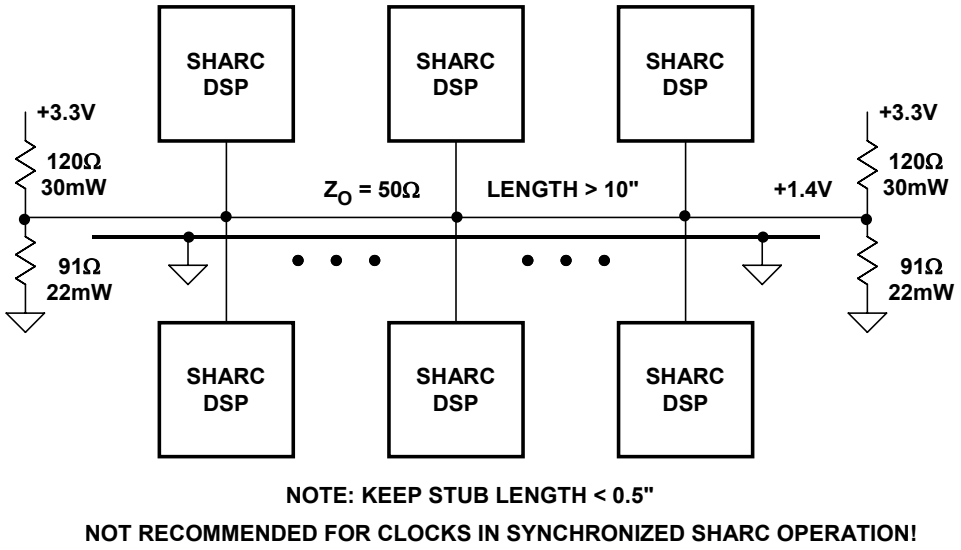



***Figure 12.46:*** *Single Transmission Line Terminated at Both Ends*

Emitter-coupled-logic (ECL) has long been known for low noise and its ability to drive terminated transmission lines with rise/fall times less than 2 ns. The family presents a constant load to the power supply, and the low level differential outputs provide a high degree of common-mode rejection. However, ECL dissipates lots of power.

## Low Voltage Differential Signaling (LVDS)

Recently, low-voltage-differential-signaling (LVDS) logic has attained widespread popularity because of similar characteristics, but with lower amplitudes and lower power dissipation than ECL. The defining LVDS specification can be found in the References. The LVDS logic swing is typically 350 mV peak-to-peak centered about a common-mode voltage of +1.2 V. A typical driver and receiver configuration is shown in Figure 12.47. The driver consists of a nominal 3.5 mA current source with polarity switching provided by PMOS and NMOS transistors as in the case of the AD9430 12-bit, 170-MSPS/210-MSPS ADC. The output voltage of the driver is nominally 350 mV peak-to-peak at each output, and can vary between 247 mV and 454 mV. The output current can vary between 2.47 mA and 4.54 mA. The LVDS receiver is terminated in a 100 Ω line-to-line. According to the LVDS specification, the receiver must respond to signals as small as 100 mV, over a common-mode voltage range of 50 mV to +2.35 V. The wide common-mode receiver voltage range is to accommodate ground voltage differences up to ±1 V between the driver and receiver.

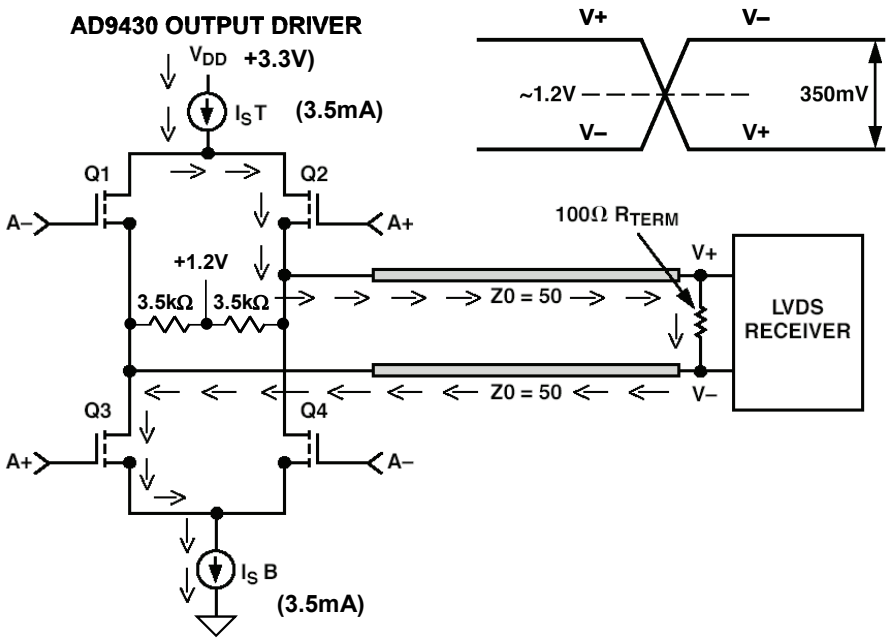
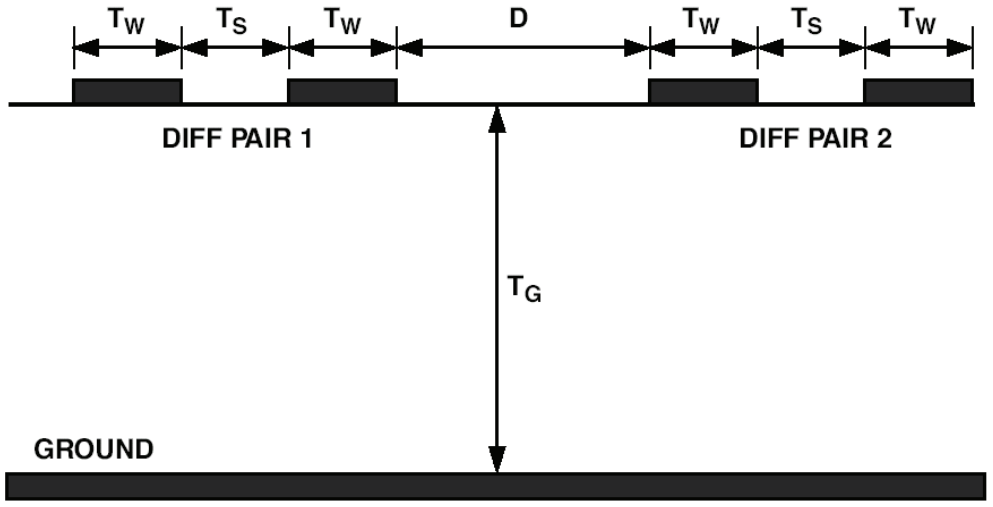



***Figure 12.47:*** *LVDS Driver and Receiver*

The LVDS edge speed is defined as the 20% to 90% rise/fall time (as opposed to 10% to 90% for CMOS logic) and specified to be less than < 0.3 $t_{ui}$, where $t_{ui}$ is the inverse of the data signaling rate. For a 210 MSPS sampling rate, $t_{ui}$ = 4.76 ns, and the 20% to 80% rise/fall time must be less than 0.3 × 4.76 = 1.43 ns. For the AD9430, the rise/fall time is nominally 0.5 ns.

LVDS outputs for high performance ADCs should be treated differently than standard LVDS outputs used in digital logic. While standard LVDS can drive 1 meter to 10 meters in high speed digital applications (dependent on data rate), it is not recommended to let a high performance ADC drive that distance. It is recommended to keep the output trace lengths short (< 2 in.), minimizing the opportunity for any noise coupling onto the outputs from the adjacent circuitry, which may get back to the analog inputs. The differential output traces should be routed close together, maximizing common-mode rejection, with the 100 Ω termination resistor close to the receiver. Users should pay attention to PCB trace lengths to minimize any delay skew. A typical differential microstrip PCB trace cross section is shown in Figure 12.48 along with some recommended layout guidelines.




- **Keep $T_W$, $T_S$, and D constant over the trace length**
- **Keep $T_S$ ~ < $2T_W$**
- **Avoid use of vias if possible**
- **Keep D > $2T_S$**
- **Avoid 90° bends if possible**
- **Design $T_W$ and $T_G$ for ~ 50Ω**

***Figure 12.48:*** *Microstrip PCB Layout for Two Pairs of LVDS Signals*

LVDS also offers some benefits in reduced EMI. The EMI fields generated by the opposing LVDS currents tend to cancel each other (for matched edge rates). In high speed ADCs, LVDS offers simpler timing constraints compared to demultiplexed CMOS outputs at similar data rates. A demultiplexed data bus requires a synchronization signal that is not required in LVDS. In demuxed CMOS buses, a clock equal to one-half the ADC sample rate is needed, adding cost and complexity, that is not required in LVDS.

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# SECTION 3: GROUNDING

In this section we discuss grounding. This is undoubtedly one of the most difficult subjects in system design. While the basic concepts are relatively simple, implementation is very involved.

For linear systems the ground is the reference against which we base our signal. Unfortunately, it has also become the return path for the power supply current in unipolar supply systems. Improper application of grounding strategies can destroy high accuracy linear system performance.

Grounding is an issue for all analog designs, and it can be said that implementing a PCB based circuit doesn't change the fact that proper implementation is essential. Fortunately, certain principles of quality grounding, namely the use of ground planes, are intrinsic to the PCB environment. This factor is one of the more significant advantages to PCB based analog designs, and appreciable discussion of this section is focused on this issue.

Some other aspects of grounding that must be managed include the control of spurious ground and signal return voltages that can degrade performance. These voltages can be due to external signal coupling, common currents, or simply excessive IR drops in ground conductors. Proper conductor routing and sizing, as well as differential signal handling and ground isolation techniques enable control of such parasitic voltages.

One final area of grounding to be discussed is grounding appropriate for a mixed-signal, analog/digital environment. Indeed, the single issue of quality grounding can influence the entire layout philosophy of a high performance mixed signal PCB design—as it well should.

Today's signal processing systems generally require mixed-signal devices such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) as well as fast digital signal processors (DSPs). Requirements for processing analog signals having wide dynamic ranges increase the importance of high performance ADCs and DACs. Maintaining wide dynamic range with low noise in hostile digital environments is dependent upon using good high speed circuit design techniques, including proper signal routing, decoupling, and grounding.

In the past, "high precision, low speed" circuits have generally been viewed differently than so-called "high speed" circuits. With respect to ADCs and DACs, the sampling (or update) frequency has generally been used as the distinguishing speed criteria. However, the following two examples show that in practice, most of today's signal processing ICs are really "high speed," and must therefore be treated as such in order to maintain high performance. This is certainly true of DSPs, and also true of ADCs and DACs.

All sampling ADCs (ADCs with an internal sample-and-hold circuit) suitable for signal processing applications operate with relatively high speed clocks with fast rise and fall times (generally a few nanoseconds) and must be treated as high speed devices, even though throughput rates may appear low. For example, a medium speed 12-bit successive

approximation (SAR) ADC may operate on 10-MHz internal clock, while the sampling rate is only 500 kSPS.

Sigma-delta (Σ-Δ) ADCs also require high speed clocks because of their high oversampling ratios. Even high resolution, so-called "low frequency" Σ-Δ industrial measurement ADCs (having throughputs of 10 Hz to 7.5 kHz) operate on 5-MHz or higher clocks and offer resolution to 24-bits (for example, the Analog Devices AD77xx-series).

To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. In addition, some mixed-signal ICs have relatively low digital currents, while others have high digital currents. In many cases, these two types must be treated differently with respect to optimum grounding.

Digital and analog design engineers tend to view mixed-signal devices from different perspectives, and the purpose of this section is to develop a general grounding philosophy that will work for most mixed signal devices, without having to know the specific details of their internal circuits.

From the previous discussion it should be clear that the issue of grounding can not be handled in a “cookbook” approach. Unfortunately we can not give a list of things to do that will guarantee success. We can say that there are certain things that if they aren’t done will probably lead do difficulties. And, what works in one frequency range may not necessarily work in another frequency range. And, often, there are competing requirements. The best way to handle grounding is to understand how the currents flow.

## Star Ground

The "star" ground philosophy builds on the theory that there is one single ground point in a circuit to which all voltages are referred. This is known as the *star ground* point. It can be better understood by a visual analogy—the multiple conductors extending radially from the common schematic ground resemble a star. Note that the star point need not look like a star—it may be a point on a ground plane—but the key feature of the star ground system is that all voltages are measured with respect to a particular point in the ground network, not just to an undefined "ground" (i.e., wherever one can clip a probe).

This star grounding philosophy is reasonable theoretically, but is difficult to implement practically. For example, if we design a star ground system, drawing out all signal paths to minimize signal interaction and the effects of high impedance signal or ground paths, we often find implementation problems. When the power supplies are added to the circuit diagram, they either add unwanted ground paths, or their supply currents flowing in the existing ground paths are sufficiently so large, or noisy (or both) so as to corrupt the signal transmission. This particular problem can often be avoided by having separate power supplies (and thus separate ground returns) for the various circuit portions. For example, separate analog and digital supplies with separate analog and digital grounds, joined at the star point, are common in mixed signal applications.

## Separate Analog and Digital Grounds

As a fact of life, digital circuitry is noisy. Saturating logic, such as TTL and CMOS, draws large, fast current spikes from its supply during switching. However, logic stages, with hundreds of millivolts (or more) of noise immunity, usually have little need for high levels of supply decoupling.

On the other hand, analog circuitry is quite vulnerable to noise on both power supply rails and grounds. So, it is very sensible to separate analog and digital circuitry, to prevent digital noise from corrupting analog performance. Such separation involves separation of both ground returns *and* power rails, which is inconvenient in a mixed signal system.

Nevertheless, if a mixed signal system is to deliver full performance capability, it is often essential to have separate analog and digital grounds, and separate power supplies. The fact that some analog circuitry will "operate" (i.e., function) from a single +5 V supply does *not* mean that it may optimally be operated from the same noisy +5 V supply as the microprocessor and dynamic RAM, the electric fan, and other high current devices! What is required is that the analog portion *operate with full performance from such a low voltage supply*, not just be functional. This distinction will by necessity require quite careful attention to both the supply rails and the ground interfacing.

Note that analog and digital ground in a system must be joined at some point (the star ground concept), to allow signals to be referred to a common potential. This star point, or analog/digital common point, is chosen so that it does not introduce digital currents into the ground of the analog part of the system—it is often convenient to make the connection at the power supplies.

Note also that many ADCs and DACs have separate *analog ground* (AGND) and *digital ground* (DGND) pins. On the device data sheets, users are often advised to connect these pins together at the package. This seems to conflict with the advice to connect analog and digital ground at the power supplies, and, in systems with more than one converter, with the advice to join the analog and digital ground at a single point.

There is, in fact, no conflict. The labels "analog ground" and "digital ground" on these pins refer to the internal parts of the converter to which the pins are connected, and not to the system grounds to which they must go. For example, with an ADC, generally these two pins should be joined together and to the *analog* ground of the system. It is not possible to join the two pins within the IC package, because the analog part of the converter cannot tolerate the voltage drop resulting from the digital current flowing in the bond wire to the chip. But they can be so tied, *externally*.

Figure 12.49 illustrates this concept of ground connections for an ADC. If these pins are connected in this way, the digital noise immunity of the converter is diminished somewhat, by the amount of common-mode noise between the digital and analog system grounds. However, since digital noise immunity is of the order of hundreds or thousands of millivolts, this factor is unlikely to be important.

The analog noise immunity is diminished only by the external digital currents of the converter itself flowing in the analog ground. These currents should be kept quite small, and this can be minimized by ensuring that the converter outputs don't see heavy loads. A good solution towards this is to use a low input current buffer at the ADC output, such as a CMOS buffer-register IC.

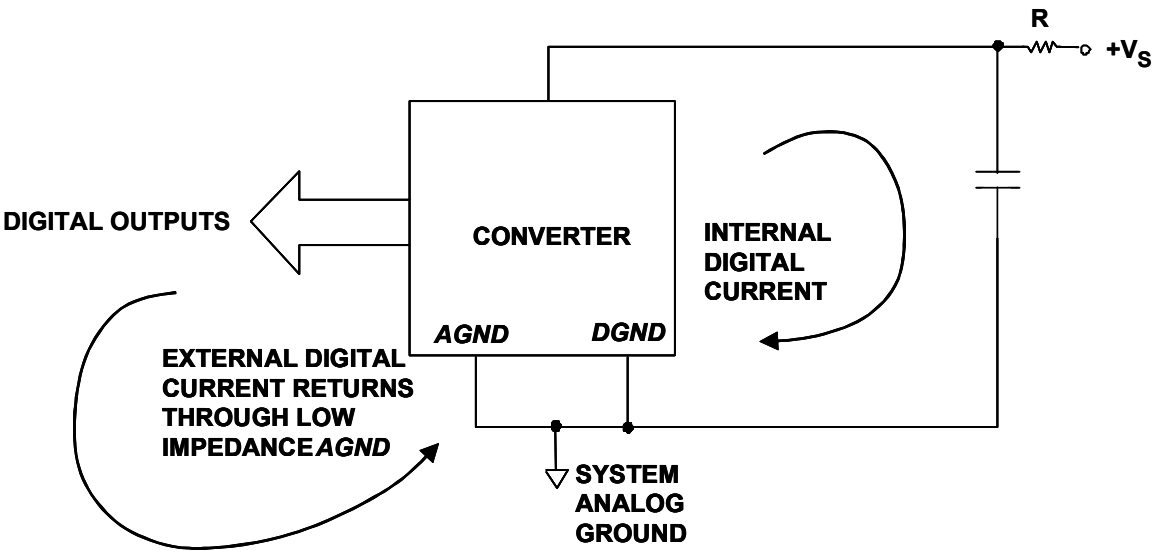


***Figure 12.49:*** *Analog (AGND) and Digital Ground (DGND) Pins of a Data Converter Should Be Returned to System Analog Ground*

If the logic supply to the converter is isolated with a small resistance and decoupled to analog ground with a local 0.1 μF capacitor, all the fast-edge digital currents of the converter will return to ground through the capacitor, and will not appear in the external ground circuit. If the analog ground impedance is maintained low, as it should be for adequate analog performance, additional noise due to the external digital ground current should rarely present a problem.

## Ground Planes

Related to the star ground system discussed earlier is the use of a *ground plane*. To implement a ground plane, one side of a double-sided PCB (or one layer of a multilayer one) is made of continuous copper and used as ground. The theory behind this is that the large amount of metal will have as low a resistance as is possible. It will, because of the large flattened conductor pattern, also have as low an inductance as possible. It then offers the best possible conduction, in terms of minimizing spurious ground difference voltages across the conducting plane.

Note that ground plane concept can also be extended to include *voltage planes*. A voltage plane offers advantages similar to a ground plane, i.e., a very low impedance conductor,

but is dedicated to a one (or more) of the system supply voltages. Thus a system can have more than one voltage plane, as well as a ground plane.

While ground planes solve many ground impedance problems, it should still be understood they aren't a panacea. Even a continuous sheet of copper foil has residual resistance and inductance, and in some circumstances, these can be enough to prevent proper circuit function. Designers should be wary of injecting very high currents in a ground plane, as they can produce voltage drops that interfere with sensitive circuitry.

The importance of maintaining a low impedance large area ground plane is critical to all analog circuits today. The ground plane not only acts as a low impedance return path for decoupling high frequency currents (caused by fast digital logic) but also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced.

Ground planes also allow the transmission of high speed digital or analog signals using transmission line techniques (microstrip or stripline) where controlled impedances are required.

The use of "buss wire" is totally unacceptable as a ground because of its impedance at the equivalent frequency of most logic transitions. For instance, #22 gauge wire has about 20 nH/inch inductance. A transient current having a slew rate of 10 mA/ns created by a logic signal would develop an unwanted voltage drop of 200 mV at this frequency flowing through 1 inch of this wire:

$$\Delta v = L\frac{\Delta i}{\Delta t} = 20\ \text{nH} * \frac{10\ \text{mA}}{\text{ns}} = 200\ \text{mV} \qquad \text{Eq. 12-12}$$

For a signal having a 2 V peak-to-peak range, this translates into an error of about 200 mV, or 10% (approximate 3.5-bit accuracy). Even in all-digital circuits, this error would result in considerable degradation of logic noise margins.

Figure 12.50 shows an illustration of a situation where the digital return current modulates the analog return current (top figure). The ground return wire inductance and resistance is shared between the analog and digital circuits, and this is what causes the interaction and resulting error. A possible solution is to make the digital return current path flow directly to the GND REF as shown in the bottom figure. This is the fundamental concept of a "star," or single-point ground system. Implementing the true single-point ground in a system which contains multiple high frequency return paths is difficult because the physical length of the individual return current wires will introduce parasitic resistance and inductance which can make obtaining a low impedance high frequency ground difficult. In practice, the current returns must consist of large area ground planes for low impedance to high frequency currents. Without a low impedance ground plane, it is therefore almost impossible to avoid these shared impedances, especially at high frequencies.

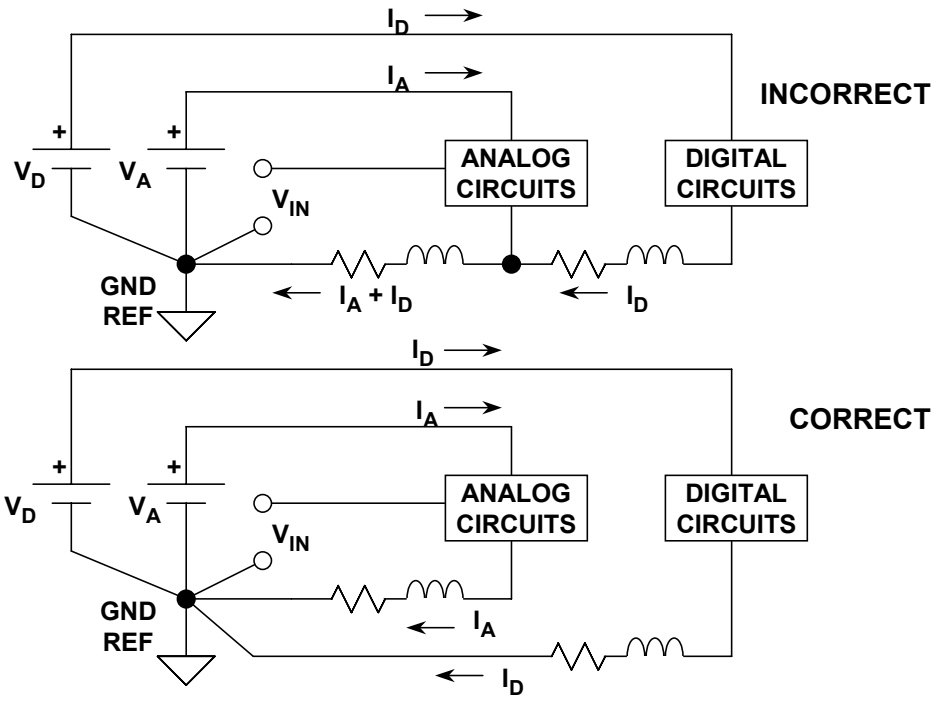


***Figure 12.50:*** *Digital Currents Flowing in Analog Return Path Create Error Voltages*

All integrated circuit ground pins should be soldered directly to the low impedance ground plane to minimize series inductance and resistance. The use of traditional IC sockets is not recommended with high speed devices. The extra inductance and capacitance of even "low profile" sockets may corrupt the device performance by introducing unwanted shared paths. If sockets must be used with DIP packages, as in prototyping, individual "pin sockets" or "cage jacks" may be acceptable. Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6). They have spring-loaded gold contacts which make good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade their performance.

Power supply pins should be decoupled directly to the ground plane using low inductance ceramic surface mount capacitors. If through hole mounted ceramic capacitors must be used, their leads should be less than 1 mm. The ceramic capacitors should be located as close as possible to the IC power pins. Ferrite beads may also be required for additional decoupling.

So, the more ground the better—right? Ground planes solve many ground impedance problems, but not all. Even a continuous sheet of copper foil has residual resistance and inductance, and in some circumstances, they can be enough to prevent proper circuit function. Figure 12.51 shows such a problem—and a possible solution.

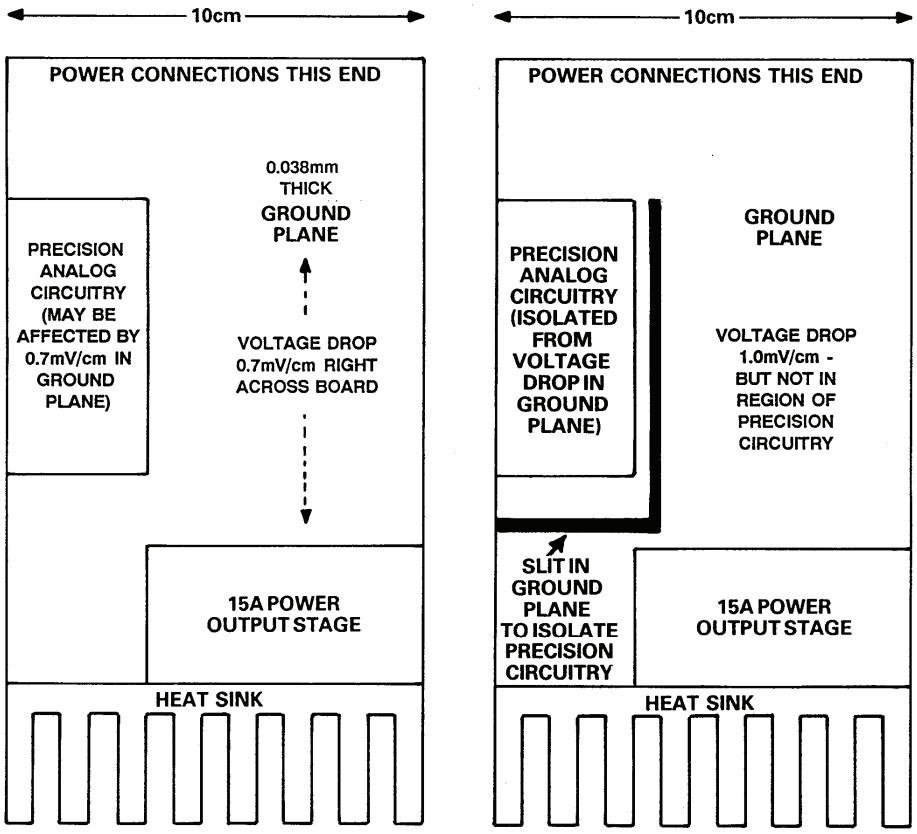


**Figure 12.51:** A Slit in the Ground Plane Can Reconfigure Current Flow for Better Accuracy

Consider the application in Fig. 12.51. Due to the realities of the mechanical design, the connector, which has power input is on one side and the power output section, which needs to be near the heat sinking, which, in turn, needs to be on the other side of the board. The board has a ground-plane 100 mm wide and a power amplifier draws 15 A. If the ground plane is 0.038 mm thick and 15 A flows in it, there will be a voltage drop of 68 μV/mm. This voltage drop would cause quite serious problems to any ground-referenced precision circuitry sharing the PCB. We can slit the ground plane so that high current does not flow in the region of the precision circuitry, instead forcing it to flow around the slit. This can possibly solve the problem (which in this case it did)—even though the voltage gradient will increase in those parts of the ground plane where the current does flow.

## Grounding and Decoupling Mixed-Signal ICs with Low Digital Currents

Sensitive analog components such as amplifiers and voltage references are always referenced and decoupled to the analog ground plane. *The ADCs and DACs (and other mixed-signal ICs) with low digital currents should generally be treated as analog components and also grounded and decoupled to the analog ground plane*. At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually has pins designated as *analog ground* (AGND) and *digital ground* (DGND). The diagram shown in Figure 12.52 will help to explain this seeming dilemma.

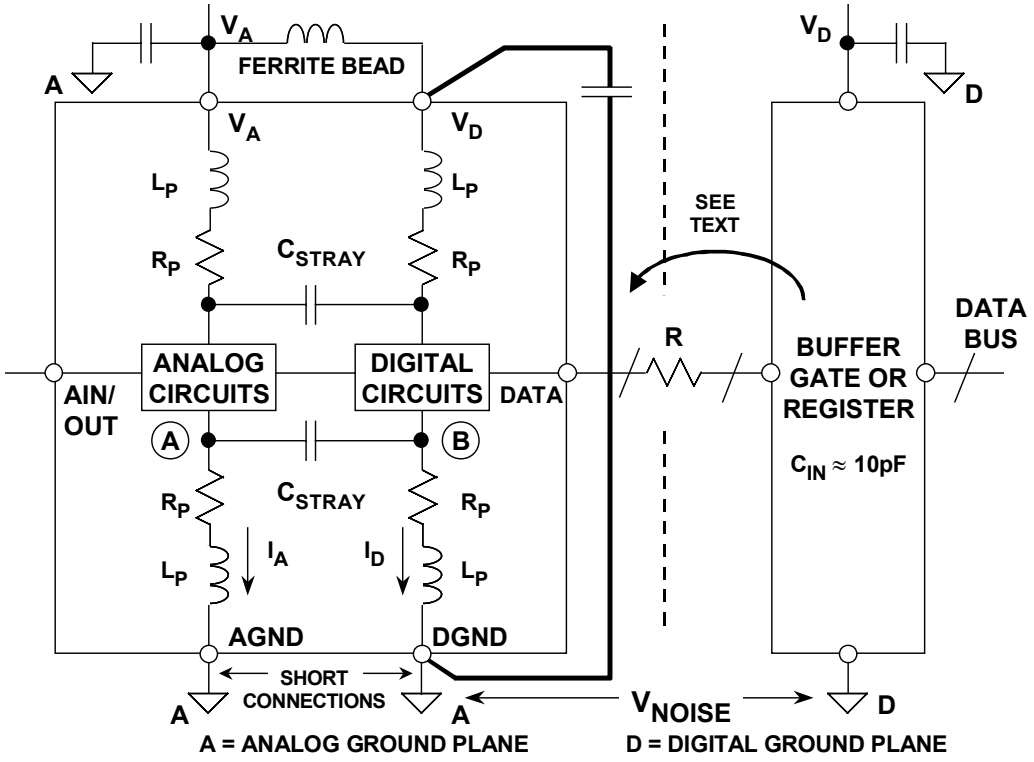


***Figure 12.52:*** *Proper Grounding of Mixed-signal ICs with Low Internal Digital Currents*

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 12.52 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the bond pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, $C_{STRAY}$. In addition, there is approximately 0.2 pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together

externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance. *Note that connecting DGND to the digital ground plane applies $V_{NOISE}$ across the AGND and DGND pins and invites disaster!*

*The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system. It could correctly be referred to as "Digital Return."*

It is true that this arrangement may inject a small amount of digital noise onto the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter output does not drive a large fanout (they normally can't, by design). Minimizing the fanout (which, in turn, means lower currents) on the converter's digital port will also keep the converter logic transitions relatively free from ringing and minimize digital switching currents, and thereby reducing any potential coupling into the analog port of the converter. The logic supply pin ($V_D$) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 12.32. The internal transient digital currents of the converter will flow in the small loop from $V_D$ through the decoupling capacitor and to DGND (this path is shown with a heavy line on the diagram). The transient digital currents will therefore not appear on the external analog ground plane, but are confined to the loop. The $V_D$ pin decoupling capacitor should be mounted as close to the converter as possible to minimize parasitic inductance. These decoupling capacitors should be low inductance ceramic types, typically between 0.01 μF and 0.1 μF.

Again, not one grounding scheme will be appropriate for all applications. But by understanding the options and planning ahead problems will be minimized.

## Treat the ADC Digital Outputs with Care

It is always a good idea (as shown in Figure 12.52) to place a buffer register adjacent to the converter to isolate the converter's digital lines from noise on the data bus. The register also serves to minimize loading on the digital outputs of the converter and acts as a Faraday shield between the digital outputs and the data bus (See Figure 12.53). Even though many converters have three-state outputs/inputs, these registers are on the die and still allow the signals on the data pins to couple into sensitive areas. This isolation register still represents good design practice. In some cases it may be desirable to add an additional buffer register on the analog ground plane next to the converter output to provide greater isolation.

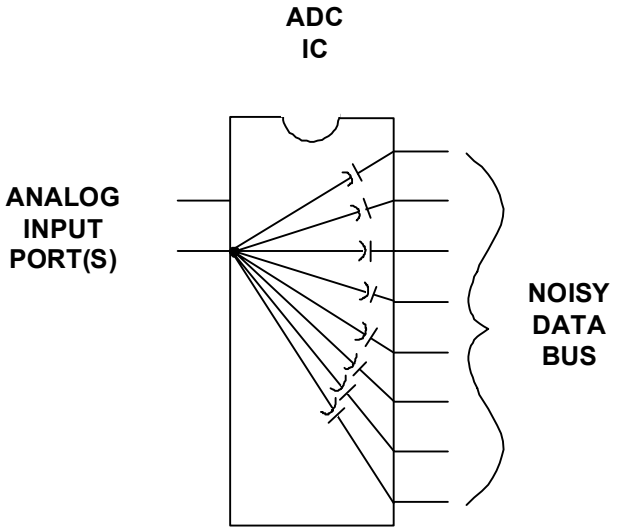


***Figure 12.53:*** *A High Speed ADC IC Using a Buffer/Latch at the Output Shows Enhanced Immunity to Digital Data Bus Noise*

The series resistors (labeled "R" in Figure 12.53) between the ADC output and the buffer register input help to minimize the digital transient currents which may affect converter performance. The resistors isolate the digital output drivers from the capacitance of the buffer register inputs. In addition, the RC network formed by the series resistor and the buffer register input capacitance acts as a lowpass filter to slow down the fast edges.

A typical CMOS gate combined with PCB trace and a through hole will create a load of approximately 10 pF. A logic output slew rate of 1 V/ns will produce 10 mA of dynamic current if there is no isolation resistor:

$$\Delta I = C \frac{\Delta v}{\Delta t} = 10\ pF * \frac{1\ V}{ns} = 10\ mA \qquad \text{Eq. 12-13}$$

.

A 500 Ω series resistors will minimize this output current and result in a rise and fall time of approximately 11 ns when driving the 10 pF input capacitance of the register:

$$t_r = 22*t = 22*R*C = 22*\ 500\ \Omega\ *\ 10\ pF = 11\ ns. \qquad \text{Eq. 12-14}$$

TTL registers should be avoided, since they can appreciably add to the dynamic switching currents because of their higher input capacitance.

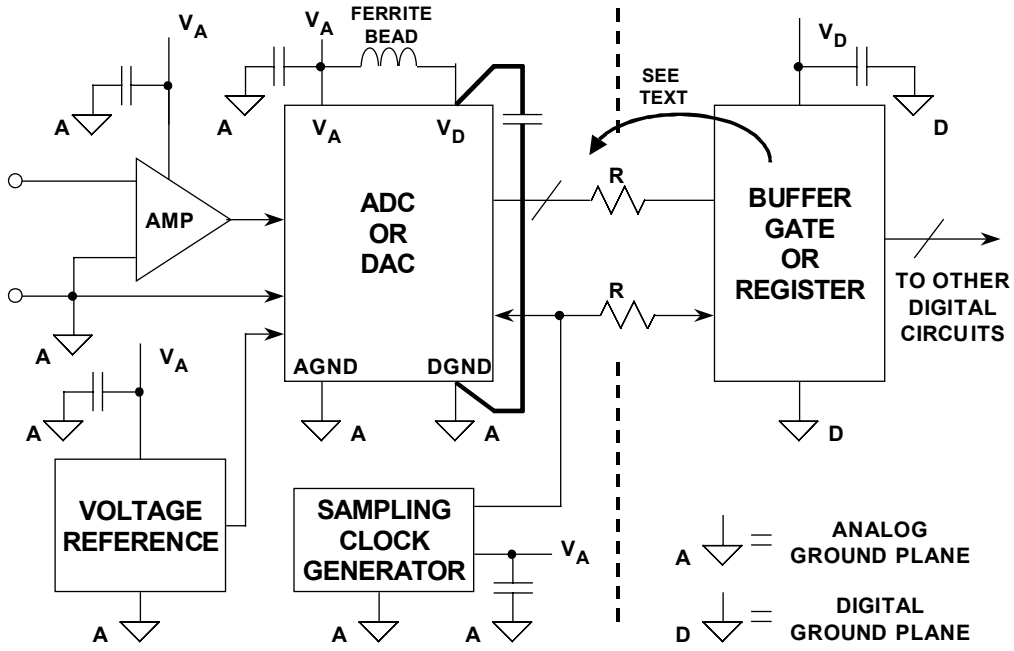


***Figure 12.54:*** *Grounding and Decoupling Points*

The buffer register and other digital circuits should be grounded and decoupled to the *digital* ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter. The analog ground plane will generally not be very noisy, but if the noise on the digital ground plane (relative to the analog ground plane) exceeds a few hundred millivolts, then steps should be taken to reduce the digital ground plane impedance, thereby maintaining the digital noise margins at an acceptable level. Under no circumstances should the voltage between the two ground planes exceed 300 mV, or the ICs may be damaged.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin ($V_D$), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be

decoupled to the digital ground plane as shown in Figure 12.54. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

In some cases it may not be possible to connect $V_D$ to the analog supply. Some of the newer, high speed ICs may have their analog circuits powered by +5 V, but the digital interface powered by +3 V to interface to 3 V logic. In this case, the +3 V pin of the IC should be decoupled directly to the analog ground plane. It is also advisable to connect a ferrite bead in series with the power trace that connects the pin to the +3 V digital logic supply.

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily decoupled to the analog ground plane. Phase noise on the sampling clock produces degradation in system SNR as will be discussed shortly.

## Sampling Clock Considerations

In a high performance sampled data system a low phase noise crystal oscillator should be used to generate the ADC (or DAC) sampling clock because sampling clock jitter modulates the analog input/output signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

The effect of sampling clock jitter on ADC Signal-to-Noise Ratio (SNR) is given approximately by the equation:

$$SNR = 20\log_{10}\left[\frac{1}{2\pi f t_j}\right], \qquad \text{Eq. 12-15}$$

where SNR is the SNR of a perfect ADC of infinite resolution where the only source of noise is that caused by the rms sampling clock jitter, $t_j$. Note that f in the above equation is the analog input frequency. Just working through a simple example, if $t_j$ = 50 ps rms, f = 100 kHz, then SNR = 90 dB, equivalent to about 15-bits dynamic range.

It should be noted that $t_j$ in the above example is the root-sum-square (rss) value of the external clock jitter *and* the internal ADC clock jitter (called aperture jitter). However, in most high performance ADCs, the internal aperture jitter is negligible compared to the jitter on the sampling clock.

Since degradation in SNR is primarily due to external clock jitter, steps must be taken to ensure the sampling clock is as noise free as possible and has the lowest possible phase jitter. This requires that a crystal oscillator be used. There are several manufacturers of small crystal oscillators with low jitter (less than 5 ps rms) CMOS-compatible outputs. (For example, MF Electronics, 10 Commerce Dr., New Rochelle, NY 10801,

Tel. 914-576-6570 and Wenzel Associates, Inc., 2215 Kramer Lane, Austin, Texas 78758 Tel. 512-835-2038).

Ideally, the sampling clock crystal oscillator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multipurpose system clock which is generated on the digital ground plane. It must then pass from its origin on the digital ground plane to the ADC on the analog ground plane. Ground noise between the two planes adds directly to the clock signal and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics.

This can be remedied somewhat by transmitting the sampling clock signal as a differential signal using either a small RF transformer as shown in Figure 12.55 or a high speed differential driver and receiver IC. If an active differential driver and receiver are used, they should be ECL to minimize phase jitter. In a single +5 V supply system, ECL logic can be connected between ground and +5 V (PECL), and the outputs ac coupled into the ADC sampling clock input. In either case, the original master system clock must be generated from a low phase noise crystal oscillator.

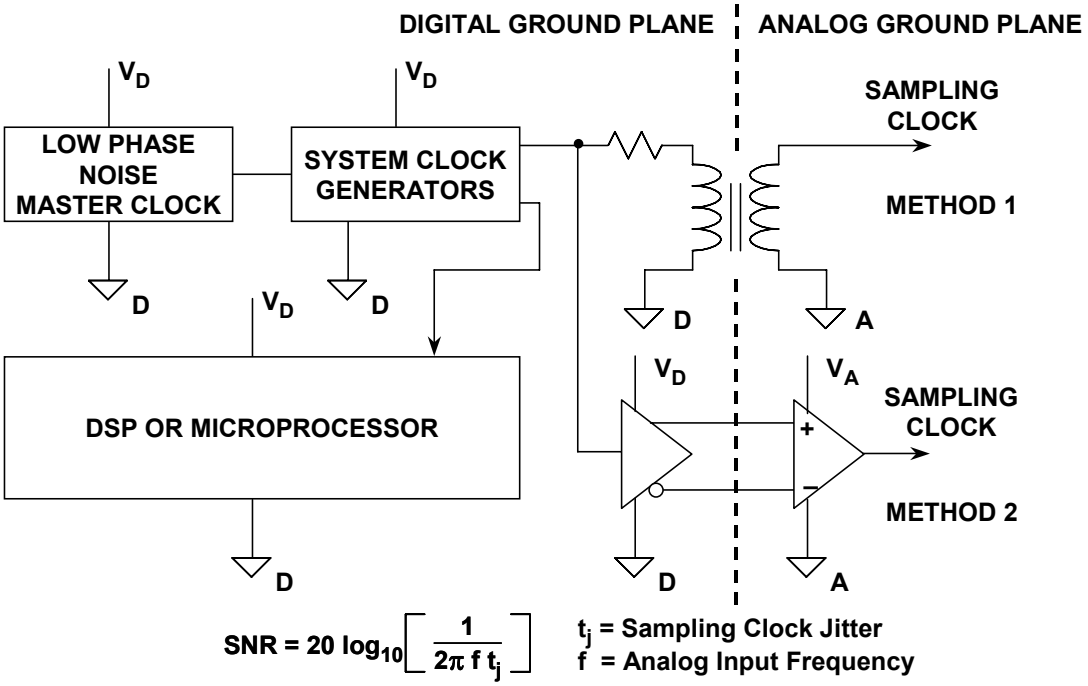


***Figure 12.55:*** *Sampling Clock Distribution from Digital to Analog Ground Planes*

## The Origins of the Confusion About Mixed-Signal Grounding

Most ADC, DAC, and other mixed-signal device data sheets discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. This has been a source of confusion when trying to apply these principles to multicard or multi-ADC/DAC systems. The recommendation is usually to split the PCB ground plane into an analog plane and a digital plane. It is then further recommended that the AGND and DGND pins of a converter be tied together and that the analog ground plane and digital ground planes be connected at that same point as shown in Figure 12.56. This essentially creates the system "star" ground at the mixed-signal device.

All noisy digital currents flow through the digital power supply to the digital ground plane and back to the digital supply; they are isolated from the sensitive analog portion of the board. The system star ground occurs where the analog and digital ground planes are joined together at the mixed signal device. While this approach will generally work in a simple system with a single PCB and single ADC/DAC, it is not optimum for multicard mixed-signal systems. In systems having several ADCs or DACs on different PCBs (or on the same PCB, for that matter), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point "star" ground system impossible. For these reasons, this grounding approach is not recommended for multicard systems, and the approach previously discussed should be used for mixed-signal ICs with low digital currents.

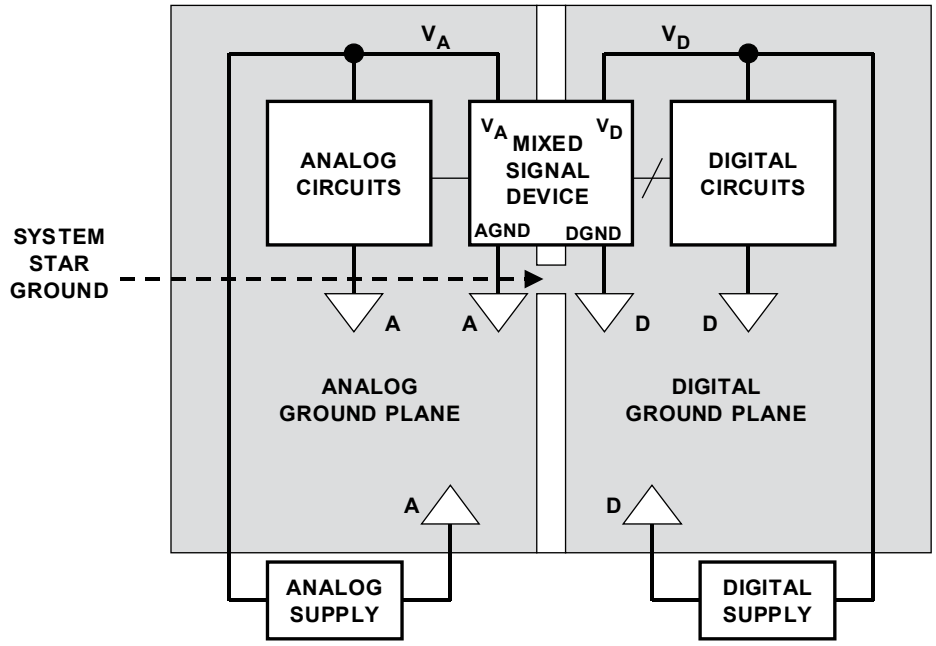


***Figure 12.56:*** *Grounding Mixed-Signal ICs: Single PC Board (Typical Evaluation/Test Board)*

## Summary: Grounding Mixed-Signal Devices with Low Digital Currents in a Multicard System

Figure 12.57 summarizes the approach previously described for grounding a mixed signal device which has low digital currents. The analog ground plane is not corrupted because the small digital transient currents flow in the small loop between $V_D$, the decoupling capacitor, and DGND (shown as a heavy line). The mixed signal device is for all intents and purposes treated as an analog component. The noise $V_N$ between the ground planes reduces the noise margin at the digital interface but is generally not harmful if kept less than 300 mV by using a low impedance digital ground plane all the way back to the system star ground.

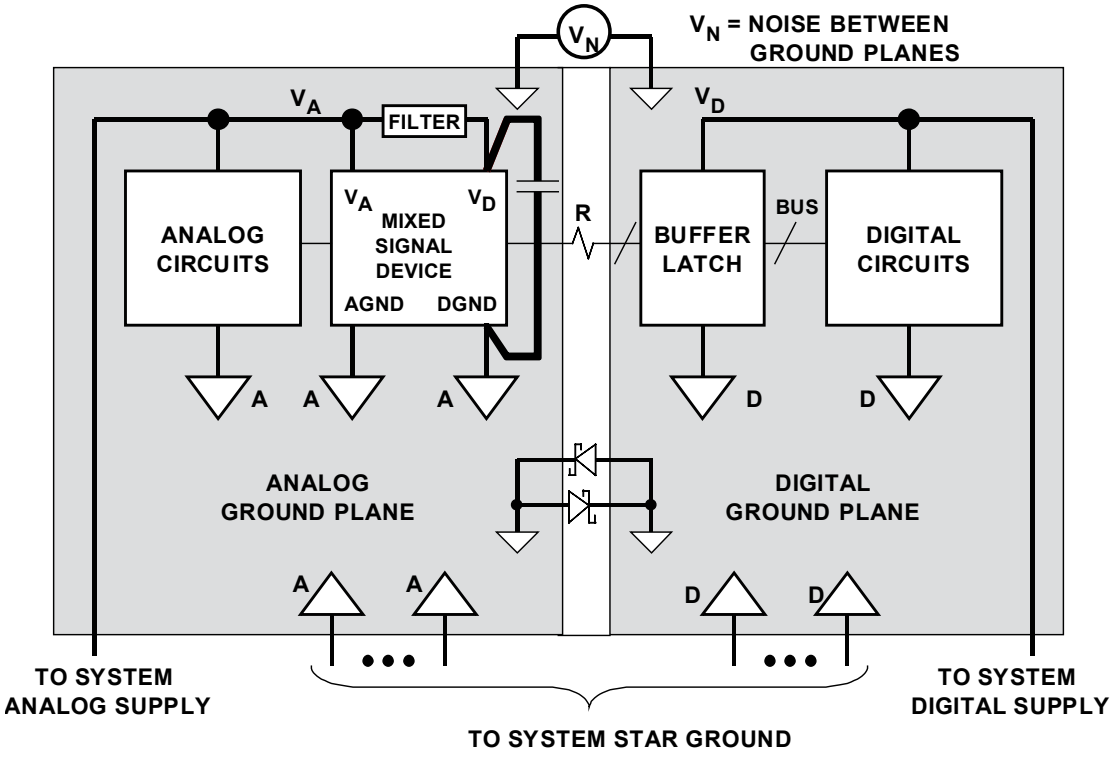


***Figure 12.57:*** *Grounding Mixed Signal ICs with Low Internal Digital Currents: Multiple PC Boards*

However, mixed-signal devices such as sigma-delta ADCs, codecs, and DSPs with on-chip analog functions are becoming more and more digitally intensive. Along with the additional digital circuitry come larger digital currents and noise. For example, a sigma-delta ADC or DAC contains a complex digital filter which adds considerably to the digital current in the device. The method previously discussed depends on the decoupling capacitor between $V_D$ and DGND to keep the digital transient currents and isolated in a small loop. However, if the digital currents are significant enough and have components at dc or low frequencies, the decoupling capacitor may have to be so large that it is impractical. Any digital current which flows outside the loop between $V_D$ and DGND

must flow through the analog ground plane. This may degrade performance, especially in high resolution systems.

It is difficult to predict what level of digital current flowing into the analog ground plane will become unacceptable in a system. All we can do at this point is to suggest an alternative grounding method which may yield better performance.

## Summary: Grounding Mixed-Signal Devices with High Digital Currents in a Multicard System

An alternative grounding method for a mixed-signal device with high levels of digital currents is shown in Figure 12.58. The AGND of the mixed signal device is connected to the analog ground plane, and the DGND of the device is connected to the digital ground plane. The digital currents are isolated from the analog ground plane, but the noise between the two ground planes is applied directly between the AGND and DGND pins of the device. For this method to be successful, the analog and digital circuits within the mixed signal device must be well isolated. The noise between AGND and DGND pins must not be large enough to reduce internal noise margins or cause corruption of the internal analog circuits.

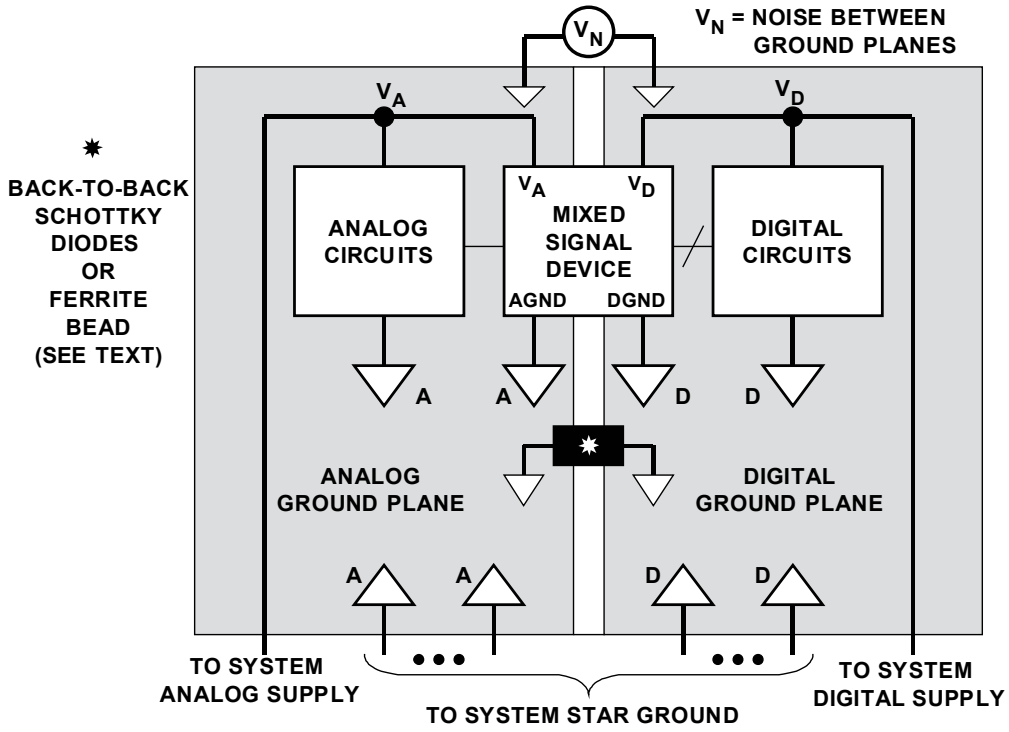


***Figure 12.58:*** *High Digital Currents: Multiple PC Boards*

Figure 12.58 shows optional Schottky diodes (back-to-back) or a ferrite bead connecting the analog and digital ground planes. The Schottky diodes prevent large dc voltages or low frequency voltage spikes from developing across the two planes. These voltages can

potentially damage the mixed-signal IC if they exceed 300 mV because they appear directly between the AGND and DGND pins. As an alternative to the back-to-back Schottky diodes, a ferrite bead provides a dc connection between the two planes but isolates them at frequencies above a few MHz where the ferrite bead becomes resistive. This protects the IC from dc voltages between AGND and DGND, but the dc connection provided by the ferrite bead can introduce unwanted dc ground loops and may not be suitable for high resolution systems.

## Grounding DSPs with Internal Phase-Locked Loops

As if dealing with mixed-signal ICs with AGND and DGNDs wasn't enough, DSPs such as the ADSP-21160 SHARC with internal phase-locked-loops (PLLs) raise issues with respect to proper grounding. The ADSP-21160 PLL allows the internal core clock (determines the instruction cycle time) to operate at a user selectable ratio of 2, 3, or 4 times the external clock frequency, CLKIN. The CLKIN rate is the rate at which the synchronous external ports operate. Although this allows using a lower frequency external clock, care must be taken with the power and ground connections to the internal PLL as shown in Figure 12.59.

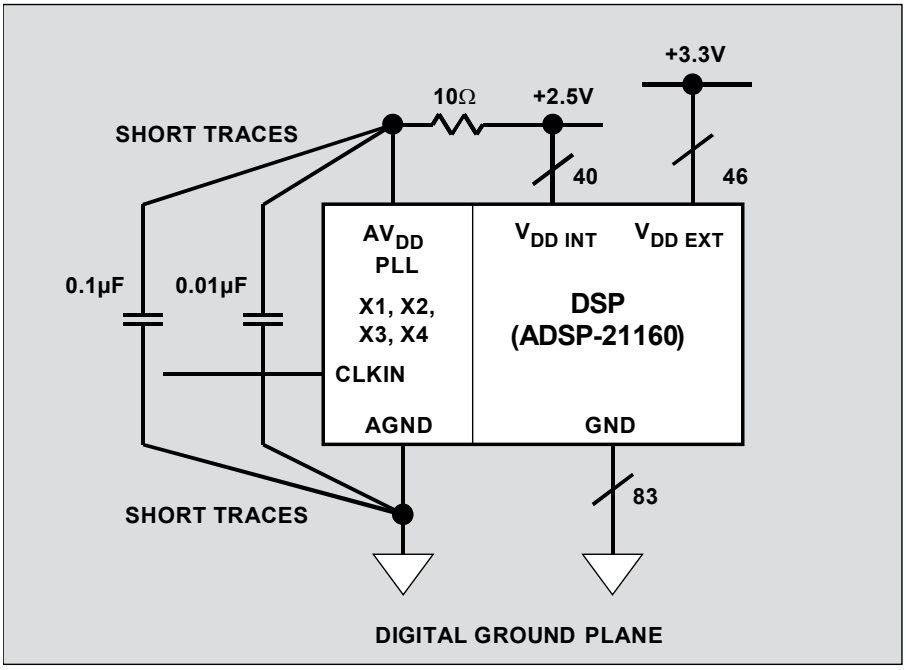


***Figure 12.59:*** *Grounding DSPs with Internal Phase-Locked-Loops (PLLs)*

In order to prevent internal coupling between digital currents and the PLL, the power and ground connections to the PLL are brought out separately on pins labeled $AV_{DD}$ and AGND, respectively. The $AV_{DD}$ +2.5 V supply should be derived from the $V_{DD\ INT}$ +2.5 V supply using the filter network as shown. This ensures a relatively noise-free

supply for the internal PLL. The AGND pin of the PLL should be connected to the digital ground plane of the PC board using a short trace. The decoupling capacitors should be routed between the $AV_{DD}$ pin and AGND pin using short traces.

## Grounding Summary

There is no single grounding method which will guarantee optimum performance 100% of the time! This section has presented a number of possible options depending upon the characteristics of the particular mixed signal devices in question. It is helpful, however to provide for as many options as possible when laying out the initial PC board.

It is mandatory that at least one layer of the PC board be dedicated to ground plane. The initial board layout should provide for nonoverlapping analog and digital ground planes, but pads and vias should be provided at several locations for the installation of back-to-back Schottky diodes or ferrite beads, if required. Pads and vias should also be provided so that the analog and digital ground planes can be connected together with jumpers if required.

The AGND pins of mixed-signal devices should in general always be connected to the analog ground plane. An exception to this are DSPs which have internal phase-locked-loops (PLLs), such as the ADSP-21160 SHARC. The ground pin for the PLL is labeled AGND, but should be connected directly to the digital ground plane for the DSP.

## Grounding for High-Frequency Operation

The “ground plane” layer is often advocated as the best return for power and signal currents, while providing a reference node for converters, references, and other subcircuits. However, even extensive use of a ground plane does not ensure a high quality ground reference for an ac circuit.

The simple circuit of Figure 12.59, built on a two layer printed circuit board, has an ac and dc current source on the top layer connected to a via (via 1) at one end and to a single U-shaped copper trace connected to via 2. Both vias go through the circuit board and connect to the ground plane. Ideally, the impedance is zero and the voltage appearing across the current source is also zero.

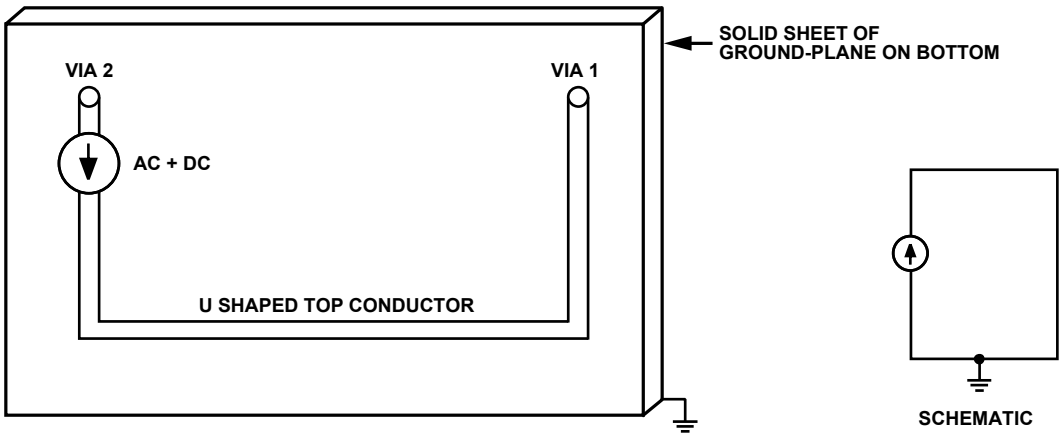


**Figure 12.60:** *Schematic and Layout of Current Source with U-shaped Trace on PC Board and Return through Ground Plane.*

This simple schematic hardly begins to show the actual subtleties. But an understanding of how the current flows in the ground plane from via 1 to via 2 makes the realities apparent and shows how ground noise in high frequency layouts can be avoided.

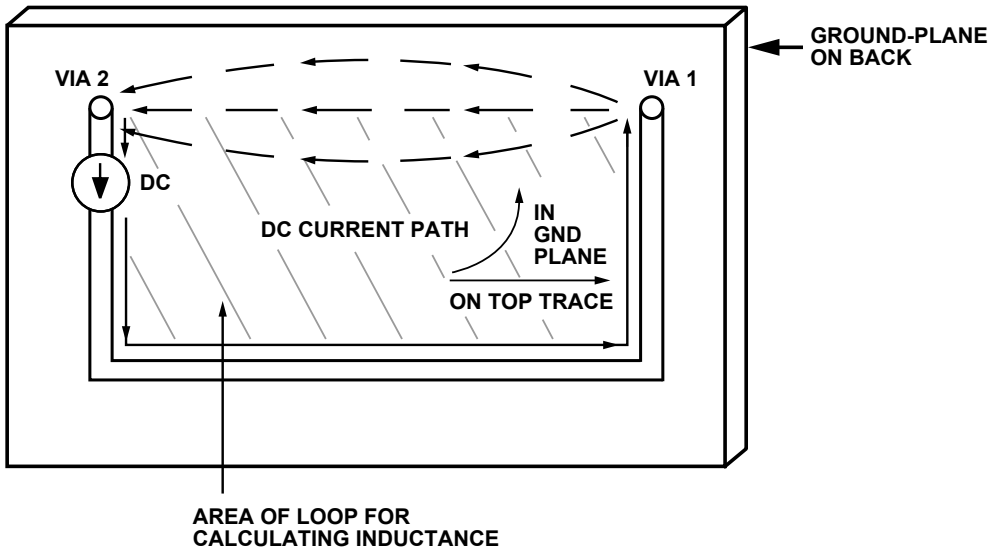


***Figure 12.61:*** *DC Current Flow for Figure 12.60*

The dc current flows in the manner in Figure 12.61, as one might surmise, taking the path of least resistance from via 1 to via 2. Some current spreading occurs, but little current flows a substantial distance from this path. In contrast, the ac current does not take the path of least resistance, it take the path of least impedance, which, in turn, depends on inductance.

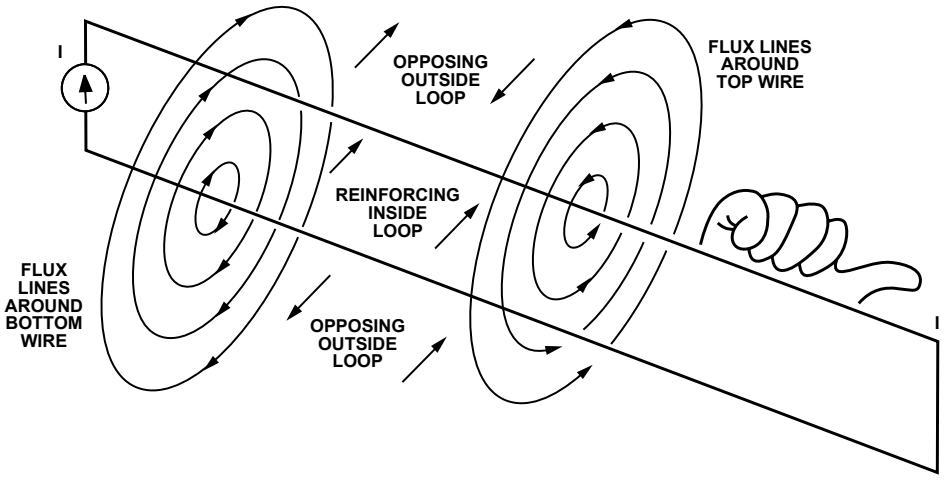


**Figure 12.62:** Magnetic Field Lines and Inductive Loop (Right Hand Rule)

Inductance is proportional to the area of the loop made by the current flow; the relationship can be illustrated by the right hand rule and the magnetic field shown in Figure 12.62 Inside the loop, current along all parts of the loop produces magnetic field lines that add constructively. Away from the loop, however, field lines form different parts add destructively, thus the field is confined principally within the loop. A larger loop has greater inductance. This means that, for a given current level, it has more stored magnetic energy ($Li^2$), greater impedance ($X_L = j\omega L$), and hence will develop more voltage a given frequency.

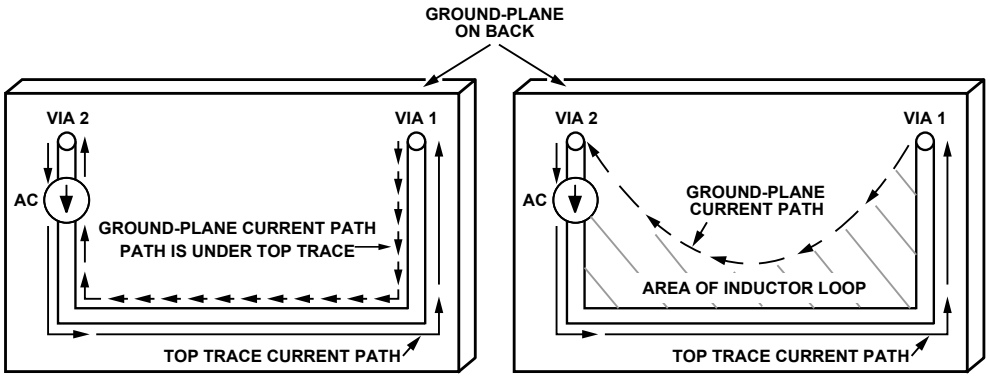


***Figure 12.63:*** *AC Current Path Without (left) and with (right) Resistance in the Ground Plane*

Which path will the current choose in the ground plane? Naturally the lower impedance path. Considering the loop formed by the U-shaped surface lead and the ground plane and neglecting resistance, high frequency ac current will follow the path with the least inductance, hence the least area.

In the example shown, the loop with the least area is quite evidently formed by the U-shaped top trace and the portion of the ground plane directly underneath it. So while Figure 12.61 shows the dc current path, Figure 12.63 shows the path that most of the ac current takes in the ground plane, where it finds minimum area, directly under the U-shaped top trace. In practice, the resistance in the ground plane causes the current to flow at low- and mid-frequencies to somewhere between straight back and directly under the top conductor. However, the return path is nearly under the top trace as low as 1 MHz or 2 MHz.

## Be Careful with Ground Plane Breaks

Wherever there is a break in the ground plane beneath a conductor, the ground plane return current must by necessity flow *around* the break. As a result, both the inductance and the vulnerability of the circuit to external fields are increased. This situation is diagrammed in Figure 12.64, where conductors A and B must cross one another.

Where such a break is made to allow a crossover of two perpendicular conductors, it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

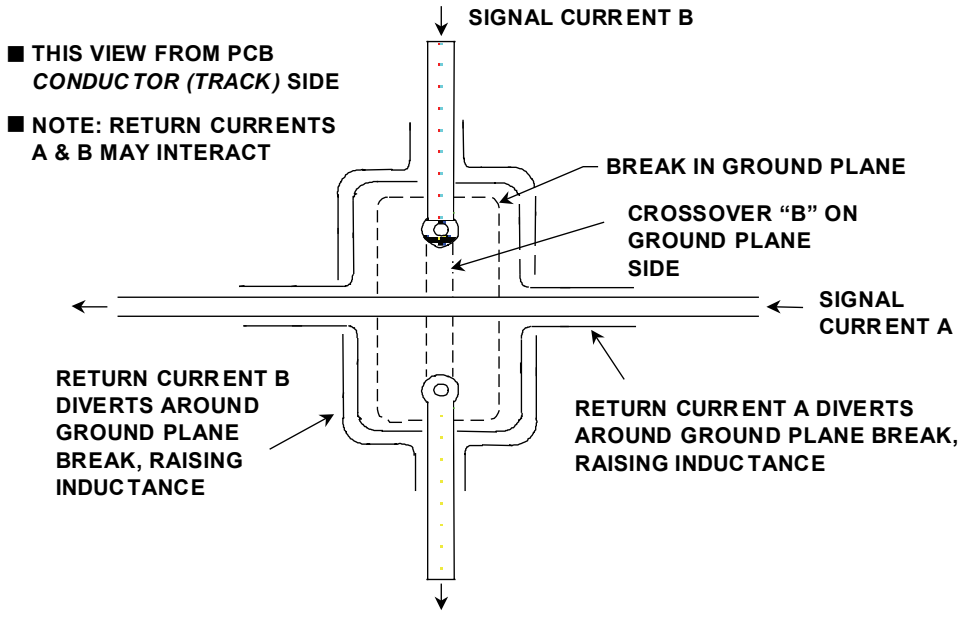


***Figure 12.64:*** *A Ground Plane Break Raises Circuit Inductance, and Increases Vulnerability to External Fields*

With a multilayer board, both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multilayer PCBs are expensive and

harder to trouble-shoot than more simple double-sided boards, but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

The use of double-sided or multilayer PCBs with at least one continuous ground plane is undoubtedly one of the most successful design approaches for high performance mixed signal circuitry. Often the impedance of such a ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system. However, whether or not this is possible does depend upon the resolution and bandwidth required, and the amount of digital noise present in the system.

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24. Alan Rich, "Shielding and Guarding," **Analog Dialogue,** Vol. 17 N0. 1, 1983, pp. 8.

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28. Paul Brokaw and Jeff Barrow, "Grounding for Low- and High-Frequency Circuits," **Analog Devices AN345.**

29. Jeff Barrow, "Avoiding Ground Problems in High Speed Circuits," **RF Design**, July 1989.

30. B. I. & B. Bleaney, **Electricity & Magnetism**, Oxford at the Clarendon Press, 1957, pp 23, 24, & 52.

31. William C. Rempfer, *Get All the Fast ADC Bits You Pay For*, **Electronic Design, Special Analog Issue**, June 24, 1996, p.44.

32. Mark Sauerwald, *Keeping Analog Signals Pure in a Hostile Digital World*, **Electronic Design, Special Analog Issue**, June 24, 1996, p.57.

33. Walt Kester and James Bryant, *Grounding in High Speed Systems*, **High Speed Design Techniques**, Analog Devices, 1996, Chapter 7, p. 7-27.

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## Notes:

# SECTION 4: DECOUPLING

It is imperative to properly decouple ALL ICs in a high speed and/or high precision application. This decoupling should include a small (typically 0.01 μF to 0.1μF) capacitor. This capacitor should have good high frequency characteristics. Surface mount multilayer ceramics are ideal; the purpose of this capacitor is to shunt any high frequency noise away for the IC. This is because the power supply rejection ratio drops with frequency, as shown in Figure 12.65. While this plot is for an op amp, all linear circuits and converters have the same general shape, rejection falling with increasing frequency. Keeping the high frequency noise out of the IC helps keep it from getting to the output (of a linear circuit) or affecting the noise (of a converter)

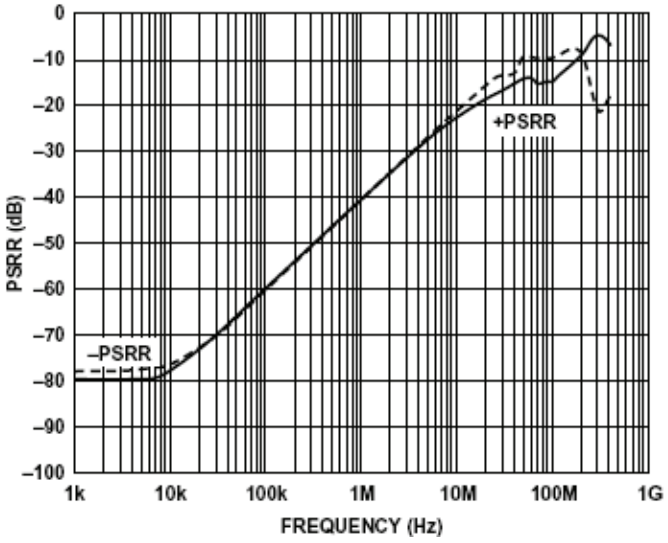


***Figure 12.65:*** *Power Supply Rejection Ratio (PSRR) of an AD8029*

In addition to the high frequency cap there should be liberal use of larger electrolytic capacitors (10 μF to 100 μF). These capacitors are not required at every chip. The purpose of these capacitors is to provide a local reservoir of charge so that instantaneous current demands can be provided from a local source, instead of having to come from a power supply which may be relatively far away and subject to the inductance and resistance of the PCB traces.

## Local high frequency bypass/decoupling

As we have stated, each individual analog stage requires local, high frequency decoupling. *These stages are provided directly at the power pins, of* all *individual analog stages*. Figure 12.66 shows the preferred technique, in both correct (left) as well as incorrect example implementations (right). In the left example, a typical 0.1 μF chip ceramic capacitor goes directly to the opposite PCB side ground plane, by virtue of the via, and on to the IC's GND pin by a second via. In contrast, the less desirable

arrangement at the right adds additional PCB trace inductance in the ground path of the decoupling cap, reducing effectiveness.

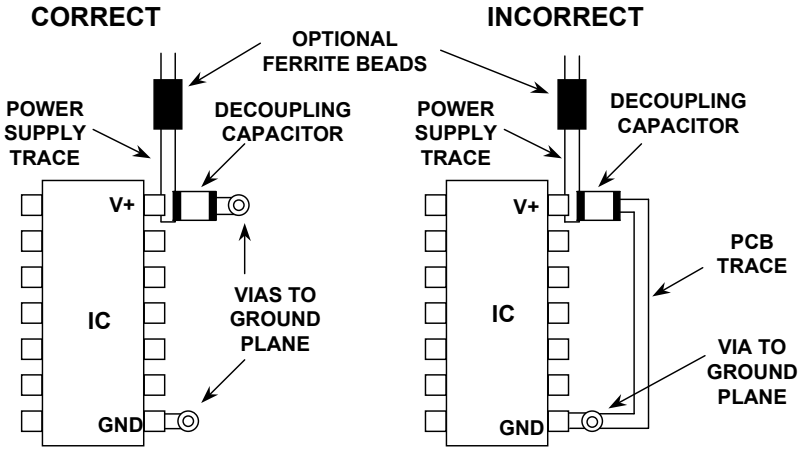


***Figure 12.66:*** *Localized High Frequency Supply Filter(s) Provides Optimum Filtering and Decoupling via Short Low-Inductance Path (Ground Plane)*

The general technique shown here as suitable for single-rail power supply, but the concept obviously extends to dual rail systems. Note—if the decoupled IC in question is an op amp, the GND pin shown is the $-V_S$ pin. For dual supply op amp uses, there is no op amp GND pin per se, so the dual decoupling networks should go directly to the ground plane when used, or other local ground.

*All* high frequency (i.e., ≥10 MHz) ICs should use a bypassing scheme similar to Figure 12.66 for best performance. Trying to operate op amps and other high performance ICs without local bypassing is almost always folly. It *may* be possible in a few circumstances, *if* the circuitry is strictly micropower in nature, and the gain-bandwidth in the kHz range. To put things into an overall perspective however, note that a pair of 0.1 μF ceramic bypass caps cost less than 25 cents. Hardly a worthy saving compared to the potential grief and lost time of troubleshooting a system without bypassing!

In contrast, the ferrite beads aren't 100% necessary, but they will add extra HF noise isolation and decoupling, which is often desirable. Possible caveats here would be to verify that the beads never saturate, when the op amps are handling high currents.

Note that with some ferrites, even before full saturation occurs, some beads can be nonlinear, so if a power stage is required to operate with a low distortion output, this should also be lab checked.

The effects of inadequate decoupling on harmonic distortion performance are dramatically illustrated in Figure 12.67. The left photo shows the spectral output of the AD9631 op amp driving a 100 Ω load with proper decoupling (output signal is 20 MHz,

2 V p-p). Notice that the second harmonic distortion at 40 MHz is approximately –70 dBc. If the decoupling is removed, the distortion is increased, as shown in the right photo of the same figure. Figure 12.67A also shows stray RF pickup in the wiring connecting the power supply to the op amp test fixture. Unlike lower frequency amplifiers, the power supply rejection ratio of many high frequency amplifiers is generally fairly poor at high frequencies. For example, at 20 MHz, the power supply rejection ratio of the AD9631 is less than 25 dB. This is the primary reason for the degradation in performance with inadequate decoupling. The change in output signal

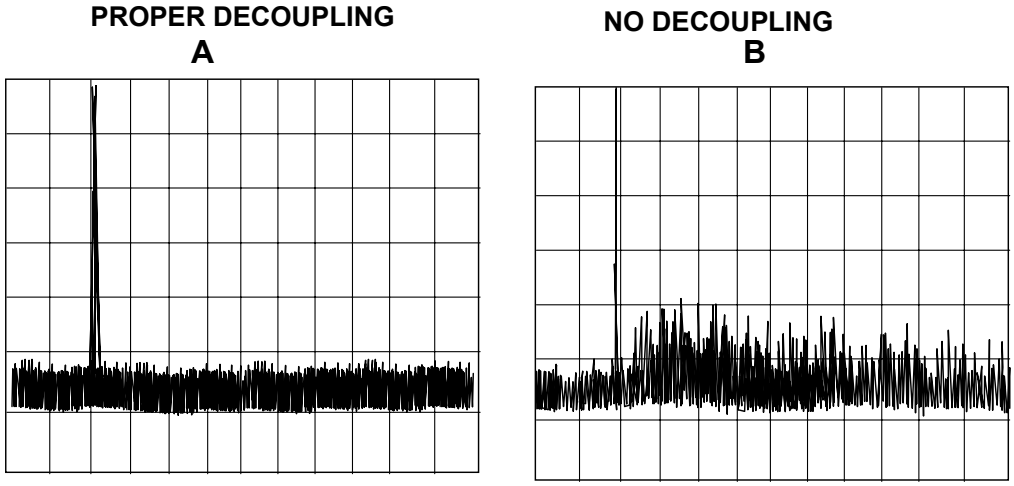


***Figure 12.67:*** *Effects of Inadequate Decoupling on Harmonic Distortion Performance of the AD9611 Op Amp*

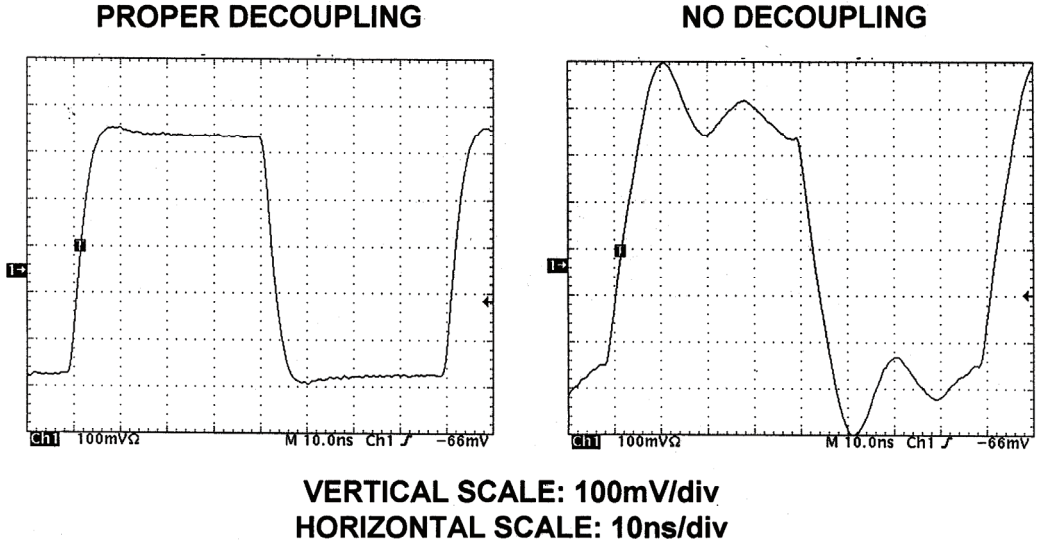


***Figure 12.68:*** *Effects of Inadequate Decoupling on the Phase Response of the AD9631 Op Amp*

produces a corresponding signal dependent load current change. The corresponding change in power supply voltage due to inadequate decoupling produces a signal dependent error in the output which manifests itself as an increase in distortion.

Inadequate decoupling can also severely affect the pulse response of high speed amplifiers such as the AD9631. Figures 12.67 and 12.68 shows normal operation and the effects of removing all decoupling capacitors on the AD9631 in its evaluation board. Notice the severe ringing on the pulse response for the poorly decoupled condition.

## Ringing

An inductor in series or parallel with a capacitor forms a resonant, or "tuned," circuit, whose key feature is that it shows marked change in impedance over a small range of frequency. Just how sharp the effect is depends on the relative Q of the tuned circuit. The effect is widely used to define the frequency response of narrow-band circuitry, but can also be a potential problem source.

If stray inductance and capacitance (which may or may not be stray) in a circuit should form a tuned circuit, then that tuned circuit may be excited by signals in the circuit, and ring at its resonant frequency.

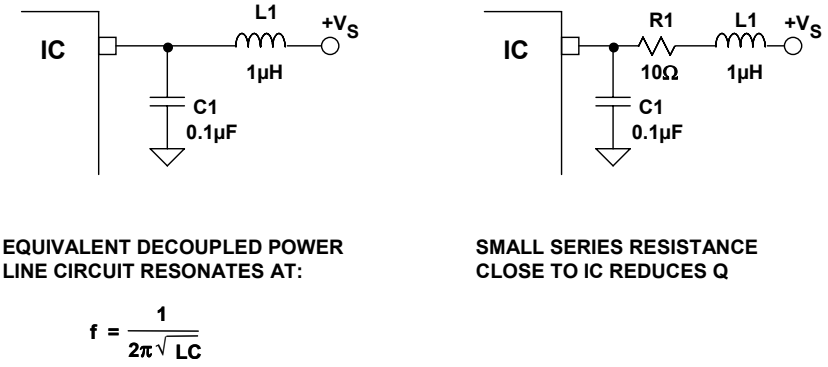


***Figure 12.69:*** *Resonant Circuit Formed by Power Line Decoupling*

An example is shown in Figure 12.69, where the resonant circuit formed by an inductive power line and its decoupling capacitor may possibly be excited by fast pulse currents drawn by the powered IC.

While normal trace inductance and typical decoupling capacitances of 0.01 µF to 0.1 µF will resonate well above a few MHz, an example 0.1 µF capacitor and 1 µH of inductance resonates at 500 kHz. Left unchecked, this could present a resonance problem, as shown in the left case. Should an undesired power line resonance be present, the effect may be minimized by lowering the Q of the inductance. This is most easily done by inserting a small resistance (~10 Ω) in the power line close to the IC, as shown in the right case.

# References:

1. Paul Brokaw, "An IC Amplifier User's Guide to Decoupling, Grounding and Making Things Go Right for a Change," **Analog Devices AN202**.

2. Henry W. Ott, **Noise Reduction Techniques in Electronic Systems, 2nd Edition**, John Wiley, Inc., 1988, ISBN: 0-471-85068-3.

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4. Jerald Grame and Bonnie Baker, "Design Equations Help Optimize Supply Bypassing for Op Amps," **Electronic Design, Special Analog Issue**, June 24, 1996, p.9.

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# SECTION 5: THERMAL MANAGEMENT

For reliability reasons, systems with appreciable power dissipation are increasingly called upon to observe *thermal management*. All semiconductors have some specified safe upper limit for junction temperature ($T_J$), usually on the order of 150°C (sometimes 175°C). Like maximum power supply voltages, maximum junction temperature is a worst case limitation which shouldn't be exceeded. In conservative designs an ample safety margin should be included. Note that this is critical, since semiconductor lifetime is inversely related to operating junction temperature. Simply put, the cooler ICs are, the longer their lifetimes will be.

This limitation of power and temperature is basic, and is illustrated by a typical data sheet statement as in Figure 12.70. In this case it is for the AD8017AR, an 8-pin SOIC device.

> ***The maximum power that can be safely dissipated by the AD8017 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately +150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.***

***Figure 12.70:*** *Maximum Power Dissipation Data Sheet Statement for the AD8017AR, an ADI Thermally Enhanced SOIC Packaged Device*

Tied to these statements are certain conditions of operation, such as the power dissipated by the device, and the package mounting to the printed circuit board (PCB). In the case of the AD8017AR, the part is rated for 1.3 W of power at an ambient of 25°C. This assumes operation of the 8-lead SOIC package on a two-layer PCB with about 4 $in^2$ (~2500 $mm^2$) of 2 oz. copper for heat sinking purposes. Predicting safe operation for the device under other conditions is covered below.

## Thermal Basics

The symbol θ is generally used to denote *thermal resistance*. Thermal resistance is in units of °C/watt (°C/W). Unless otherwise specified, it defines the resistance heat encounters transferring from a hot IC junction to the ambient air. It might also be expressed more specifically as $\theta_{JA}$, for *thermal resistance, junction-to-ambient*. $\theta_{JC}$ and $\theta_{CA}$ are two additional θ forms used, and are further explained below.

In general, a device with a thermal resistance θ equal to 100°C/W will exhibit a temperature differential of 100°C for a power dissipation of 1 W, as measured between

two reference points. Note that this is a linear relationship, so 1 W of dissipation in this part will produce a 100°C differential (and so on, for other powers). For the AD8017AR example, θ is about 95°C/W, so 1.3 W of dissipation produces about a 124°C junction-to-ambient temperature differential. It is of course this rise in temperature that is used to predict the internal temperature, in order to judge the thermal reliability of a design. With the ambient at 25°C, this allows an internal junction temperature of about 150°C. In practice most ambient temperatures are above 25°C, so less power can then be handled.

For any power dissipation P (in watts), one can calculate the effective temperature differential (ΔT) in °C as:

$$\Delta T = P \times \theta \qquad \text{Eq. 12-16}$$

where $\theta$ is the total applicable thermal resistance.

Figure 12.71 summarizes a number of basic thermal relationships.

- **θ = Thermal Resistance (°C/W)**
- **P = Total Device Power Dissipation (W)**
- **T = Temperature (°C)**
- **ΔT = Temperature Differential = P × θ**
- **$\theta_{JA}$ = Junction-Ambient Thermal Resistance**
- **$\theta_{JC}$ = Junction-Case Thermal Resistance**
- **$\theta_{CA}$ = Case-Ambient Thermal Resistance**
- **$\theta_{JA} = \theta_{JC} + \theta_{CA}$**
- **$T_J = T_A + (P \times \theta_{JA})$**
- ***Note: $T_{J(Max)}$ = 150°C (Sometimes 175°C)***

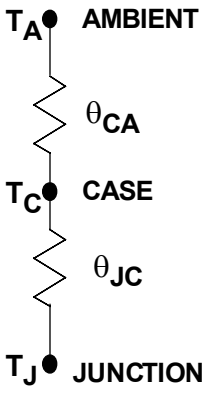


***Figure 12.71:*** *Basic Thermal Relationships*

Note that series thermal resistances, such as the two shown at the right, model the total thermal resistance path a device may see. Therefore the total θ for calculation purposes is the sum, i.e., $\theta_{JA} = \theta_{JC}$ and $\theta_{CA}$. Given the ambient temperature $T_A$, P, and θ, then $T_J$ can be calculated. As the relationships signify, to maintain a low $T_J$, either θ or the power being dissipated (or both) must be kept low. A low ΔT is the key to extending semiconductor lifetimes, as it leads to lower maximum junction temperatures.

In ICs, one temperature reference point is always the device junction, taken to mean the hottest spot inside the chip operating within a given package. The other relevant reference point will be either $T_C$, the case of the device, or $T_A$, that of the surrounding air. This then leads in turn to the above mentioned individual thermal resistances, $\theta_{JC}$ and $\theta_{JA}$.

Taking the simplest case first, $\theta_{JA}$ is the thermal resistance of a given device measured between its *junction* and the *ambient* air. This thermal resistance is most often used with small, relatively low power ICs such as op amps, which often dissipate 1 W or less. Generally, $\theta_{JA}$ figures typical of op amps and other small devices are on the order of 90°C/W to 100°C/W for a plastic 8-pin DIP package, as well as the better SOIC packages.

It should be clearly understood that these thermal resistances are *highly* package dependent, as different materials have different degrees of thermal conductivity. As a general guideline, thermal resistance of conductors is analogous to electrical resistances, that is copper is the best, followed by aluminum, steel, and so on. Thus copper lead frame packages offer the highest performance, i.e., the lowest θ.

## Heat Sinking

By definition, a *heat sink* is an added low thermal resistance device attached to an IC to aid heat removal. A heat sink has additional thermal resistance of its own, $\theta_{CA}$, rated in °C/W. However, most current IC packages don't easily lend themselves to heat sink attachment (exceptions are older TO-99 metal can types). Devices meant for heat sink attachment will often be noted by a $\theta_{JC}$ dramatically lower than the $\theta_{JA}$. In this case θ will be composed of more than one component. Thermal impedances add, making a net calculation relatively simple. For example, to compute a net $\theta_{JA}$ given a relevant $\theta_{JC}$, the thermal resistance of the heat sink, $\theta_{CA}$, or *case* to *ambient* is added to the $\theta_{JC}$ as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad \text{Eq. 12-17}$$

and the result is the $\theta_{JA}$ for that specific circumstance.

More generally, however, modern op amps *don't* use commercially available heat sinks. Instead, when significant power needs to be dissipated, such as ≥1 W, low thermal resistance copper PCB traces are used as the heat sink. In such cases, the most useful form of manufacturer data for this heat sinking are the boundary conditions of a sample PCB layout, and the resulting $\theta_{JA}$ for those conditions. This is in fact the type of specific information supplied for the AD8017AR, as mentioned earlier. Applying this approach, example data illustrating thermal relationships for such conditions is shown by Figure 12.72. These data apply for an AD8017AR mounted to a heat sink with an area of about 4 square inches on a 2 layer, 2 ounce copper PCB.

These curves indicate the maximum power dissipation vs. temperature characteristic for the AD8017, for maximum junction temperatures of both 150°C and 125°C. Such curves are often referred to as *derating* curves, since allowable power decreases with ambient temperature.

With the AD8017AR, the proprietary ADI *Thermal Coastline* IC package is used, which allows additional power to be dissipated with no increase in the SO-8 package size. For a $T_{J(max)}$ of 150°C, the upper curve shows the allowable power in this package, which is

1.3 W at an ambient of 25°C. If a more conservative $T_{J(max)}$ of 125°C is used, the lower of the two curves applies.

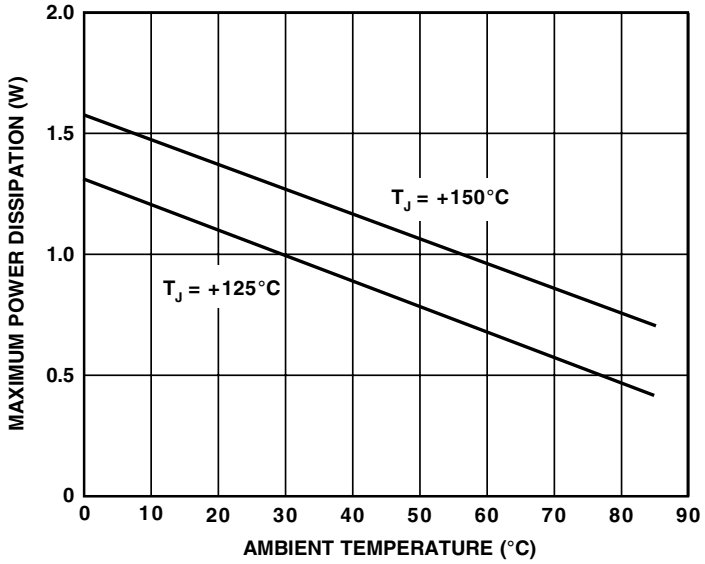


***Figure 12.72:*** *Thermal Rating Curves for AD8017AR Op Amp*

A performance comparison for an 8-pin standard SOIC and the ADI Thermal Coastline version is shown in Figure 12.73. Note that the Thermal Coastline provides an allowable dissipation at 25°C of 1.3 W, whereas a standard package allows only 0.8 W. In the Thermal Coastline heat transferal is increased, accounting for the package's lower $\theta_{JA}$.

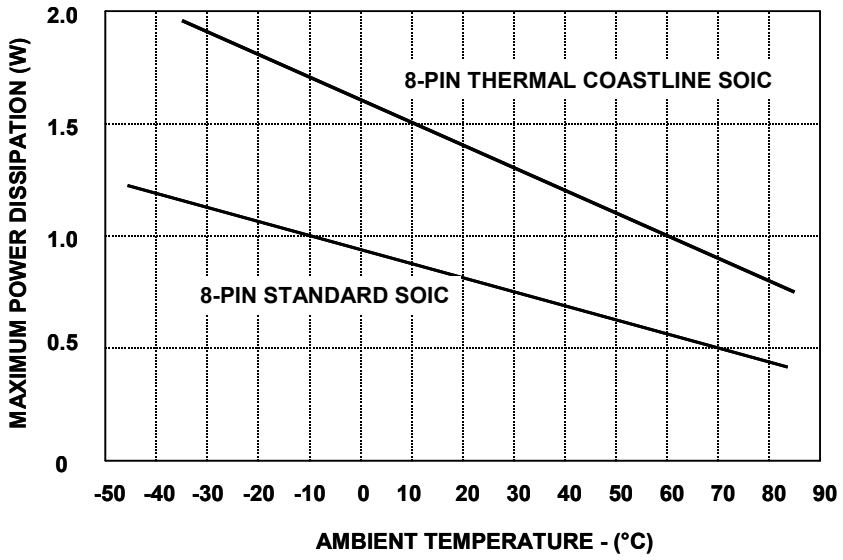


***Figure 12.73:*** *Thermal Rating Curves for Standard (Lower) and ADI Thermal Coastline (Upper) 8-Pin SOIC Packages*

Even higher power dissipation is possible, with the use of IC packages better able to transfer heat from chip to PCB. An example is the AD8016 device, available with two package options rated for 5.5 W and 3.5 W at 25°C, respectively, as shown in Figure 12.73.

Taking the higher rated power option, the AD8016ARP PSOP3 package, when used with a 10 inch$^2$ of 1 oz. heat sink plane, the combination is able to handle up to 3 W of power at an ambient of 70°C, as noted by the upper curve. This corresponds to a $\theta_{JA}$ of 18°C/W, which in this case applies for a maximum junction temperature of 125°C.

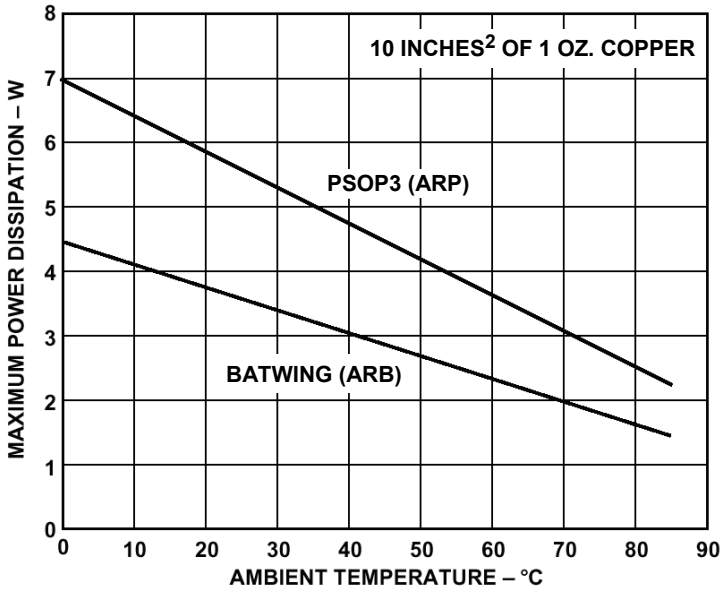


***Figure 12.74:*** *Thermal Characteristic Curves for the AD8016 BATWING (Lower) and PSOP3 (Upper) Packages, for $T_{J(Max)}$ Equal to 125°C*

The reason the PSOP3 version of the AD8016 is so better able to handle power lies with the use of a large area copper slug. Internally, the IC die rest directly on this slug, with the bottom surface exposed as shown in Figure 12.75. The intent is that this surface be soldered directly to a copper plane of the PCB, thereby extending the heat sinking.

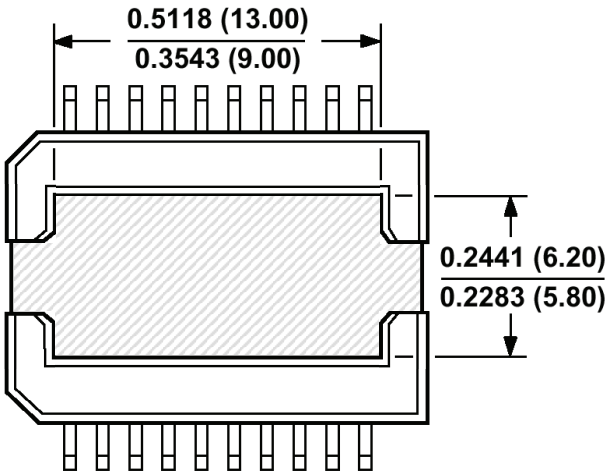


***Figure 12.75:*** *Bottom View of AD8016 20-Lead PSOP3 Package Showing Copper Slug for Aid in Heat Transfer (Central Grayed Area)*

For reliable, low thermal resistance designs with op amps, several design *Do's and Don'ts* are listed below. Consider all of these points, as may be practical.

1) *Do use as large an area of copper as possible for a PCB heat sink, up to the point of diminishing returns.*

2) *In conjunction with 1), do use multiple (outside) PCB layers, connected together with multiple vias.*

3) *Do use as heavy copper as is practical (2 oz. or more preferred).*

4) *Do provide sufficient natural ventilation inlets and outlets within the system, to allow heat to freely move away from hot PCB surfaces.*

5) *Do orient power-dissipating PCB planes vertically, for convection aided airflow across heat sink areas.*

6) *Do consider the use of external* power buffer *stages, for precision op amp applications.*

7) *Do consider the use of* forced air, *for situations where several watts must be dissipated in a confined space.*

8) *Don't use solder mask planes over heat dissipating traces.*

9) *Don't use excessive supply voltages on ICs delivering power.*

Both of the AD8016 package options are characterized for both still and moving air, but the thermal information given above applies *without* the use of directed airflow. Therefore, adding additional airflow lowers thermal resistance further (see Reference 2).

For the most part, these points are obvious. However, one that could use some elaboration is number 9. Whenever an application requires only modest *voltage* swings (such as for example standard video, 2 V p-p) a wide supply voltage range can often be used. But operation of an op amp driver on higher supply voltages produces a large IC dissipation, even though the load power is constant.

In such cases, as long as the distortion performance of the application doesn't suffer, it can be advantageous to operate the IC on lower supplies, say ±5 V, as opposed to ±15 V. The above example data was calculated on a dc basis, which will generally tax the driver more in terms of power than a sine wave or a noise-like waveform, such as a DMT signal (see Reference 2). The general principles still hold for these ac waveforms, i.e., the op amp power dissipation is high when load current is high and the voltage low.

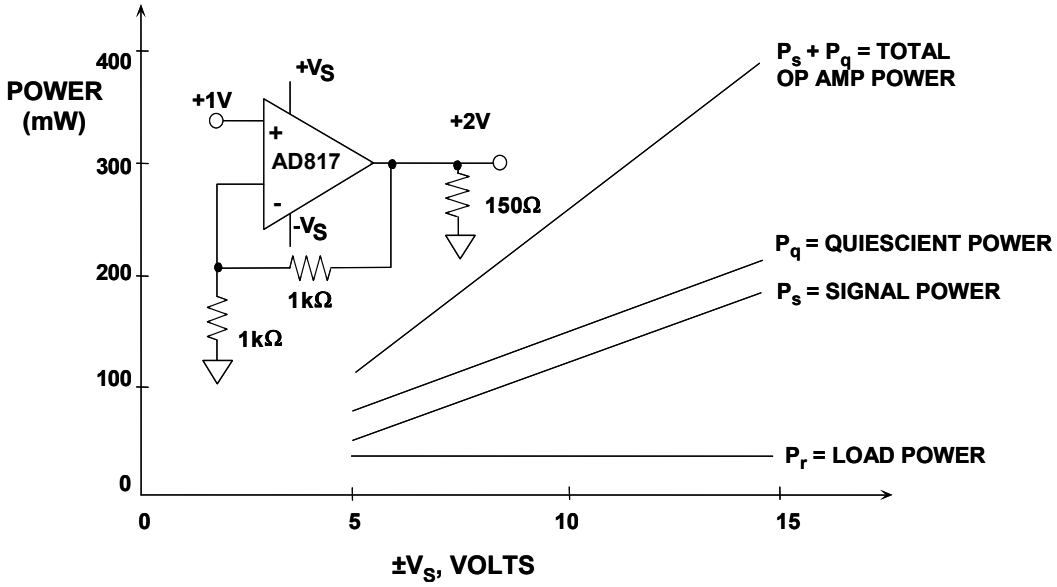


***Figure 12.76:*** *Power Dissipated in Video Op Amp Driver for Various Supply Voltages with Low Voltage Output Swing*

While there is ample opportunity for high power handling with the thermally enhanced packages described above for the AD8016 and AD8107, the increasingly popular smaller IC packages actually move in an opposite direction. Without question, it is true that today's smaller packages do noticeably sacrifice thermal performance. But, it must be

understood that this is done in the interest of realizing a smaller size for the packaged op amp, and, ultimately, a much greater final PCB density for the overall system.

These points are illustrated by the thermal ratings for the AD8057 and AD8058 family of single and dual op amp devices, as is shown in Figure 12.77. The AD8057 and AD8058 op amps are available in three different packages. These are the SOT-23-5, and the 8-pin MSOP, along with standard SOIC.

As the data shows, as the package size becomes smaller and smaller, much less power is capable of being removed. Since the lead frame is the only heat sinking possible with such tiny packages, their thermal performance is thus reduced. The $\theta_{JA}$ for the packages mentioned is 240°C/W, 200°C/W, and 160°C/W, respectively. Note this is more of a *package* than *device* limitation. Other ICs with the same packages have similar characteristics.

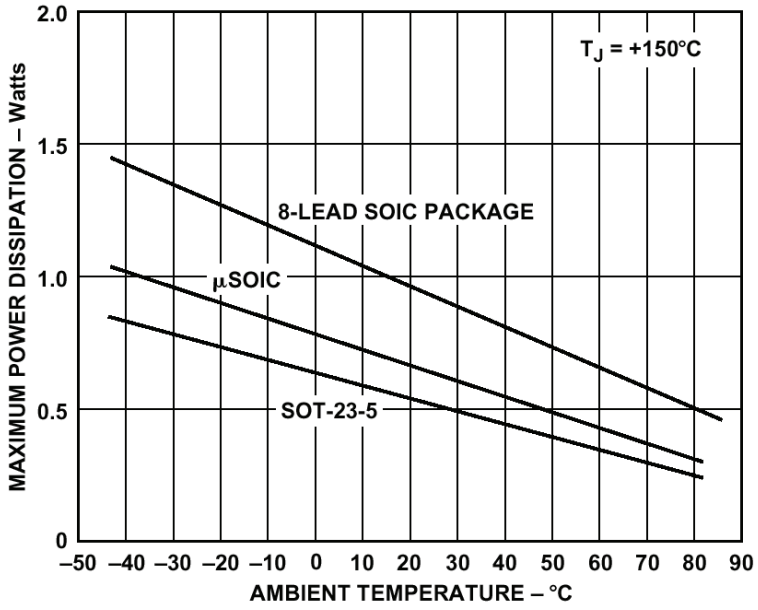


***Figure 12.77:*** *Comparative Thermal Performance for Several AD8057/AD8058 Op Amp Package Options*

## Data Converter Thermal Considerations

At first glance, one might assume that the power dissipation of an ADC or a DAC will remain constant for a given power supply voltage. However, many data converters, especially CMOS ones, have power dissipations that are highly dependent upon not only output data loading but also the sampling clock frequency. Since many of the newer high-speed converters can dissipate between 1.5 W and 2 W maximum power under the worst-case operating conditions, this point must be well understood in order to ensure that the

package is mounted in such a way as to maintain the junction temperature within acceptable limits at the highest expected operating temperature.

The previous discussion in this chapter on grounding emphasized that the digital outputs of high performance ADCs, especially those with parallel outputs, should be lightly loaded (5 pF to10 pF) in order to prevent digital transient currents from corrupting the SNR and SFDR. Even under light output loading, however, most CMOS and BiCMOS ADCs have power dissipations which are a function of sampling clock frequency and in some cases, the analog input frequency and amplitude.

For example, Figure 12.78 shows the AD9245 14-bit, 80-MSPS, 3-V CMOS ADC power dissipation versus frequency for a 2.5 MHz analog input and 5 pF output loading of the data lines. The graphs show the digital and analog power supply currents separately as well as the total power dissipation. Note that total power dissipation can vary between approximately 310 mW and 380 mW as the sampling frequency is varied between 10 MSPS and 80 MSPS.

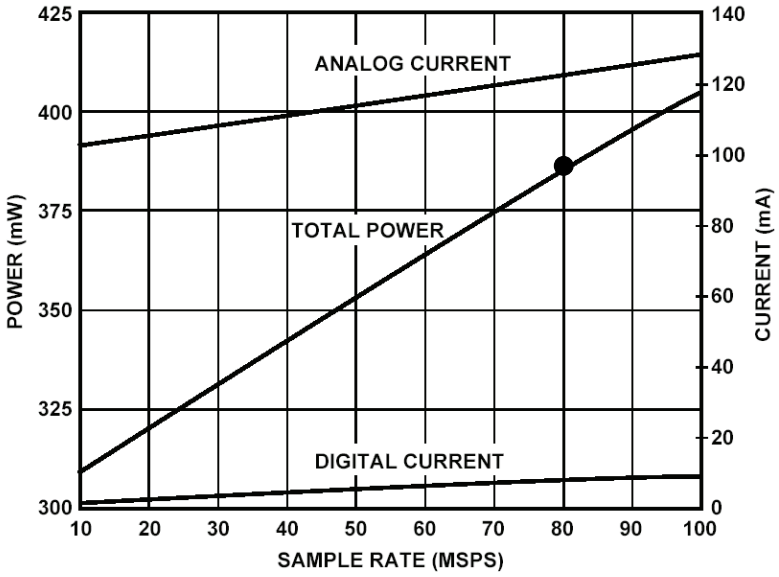


***Figure 12.78:*** *AD9245 14-Bit, 80-MSPS, 3 V CMOS ADC Power Dissipation vs. Sample Rate for 2.5 MHz Input, 5 pF Output Loads*

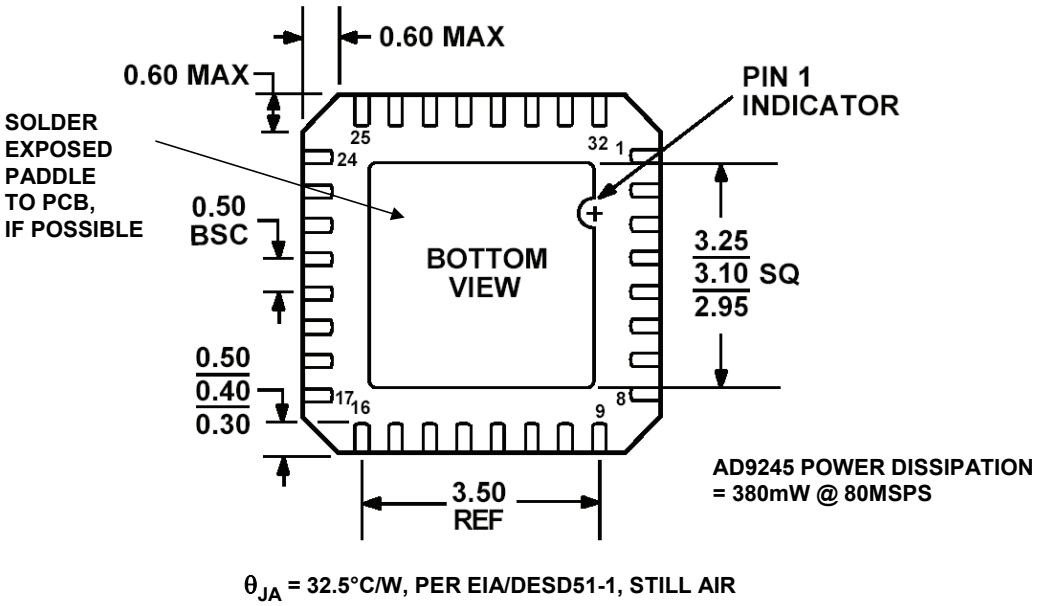


***Figure 12.79:*** *AD9245 CP-32 Lead-Frame Chip-Scale Package (LFCSP), Bottom View*

The AD9245 is packaged in a 32-pin leadless chip scale package as shown in Figure 12.79. The bottom view of the package shows the exposed paddle which should be soldered to the PC board ground plane for best thermal transfer. The worst-case package junction-to-ambient resistance, $\theta_{JA}$, is specified as 32.5°C/W, which places the junction 32.5°C × 0.38°C = 12.3°C above the ambient for a power dissipation of 380 mW. For a maximum operating temperature of +85°C, this places the junction at a modest 85°C + 12.3°C = 97.3°C.

The AD9430 is a high performance 12-bit, 170 MSPS /210 MSPS, 3.3 V BiCMOS ADC. Two output modes are available: dual 105-MSPS demultiplexed CMOS outputs, or 210 MSPS LVDS outputs. Power dissipation as a function of sampling frequency is shown in Figure 12.56. Analog and digital supply currents are shown for CMOS and LVDS modes for an analog input frequency of 10.3 MHz. Note that in the LVDS mode and a sampling frequency of 210 MSPS, total supply current is approximately 455 mA—yielding a total power dissipation of 1.5 W.

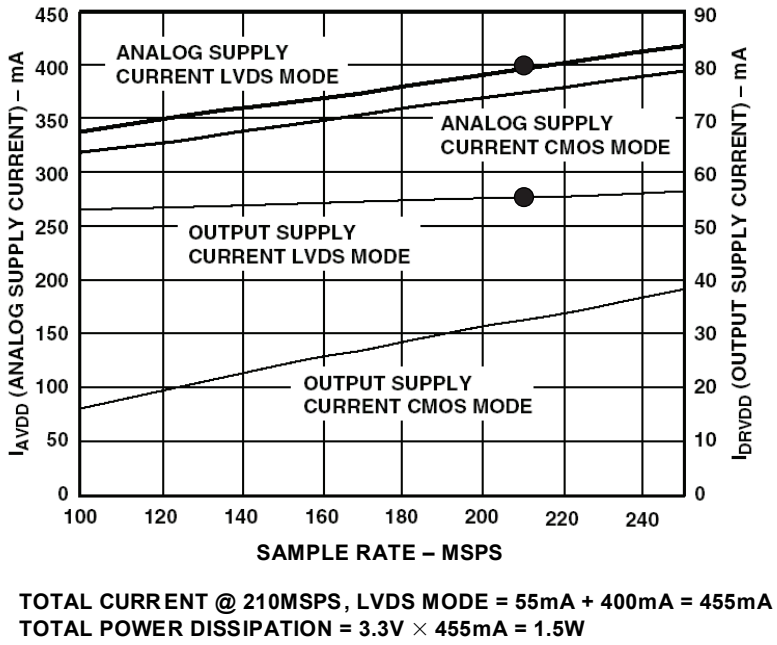


***Figure 12.80:*** *AD9430 12-Bit 170 MSPS/210 MSPS ADC Supply Current vs. Sample Rate for a 10.3 MHz Input*

The AD9430 is available in a 100-lead thin plastic quad flat package with an exposed pad (TQFP/EP) as shown in Figure 12.81. The conducive pad is connected to chip ground and should be soldered to the PC board ground plane. The $\theta_{JA}$ of the package when soldered to the ground plane is 25°C/W in still air. This places the junction 25°C × 1.5°C = 37.5°C above the ambient temperature for 1.5 W of power dissipation. For a maximum operating temperature of +85°C, this places the junction at 85°C + 37.5°C = 122.5°C.

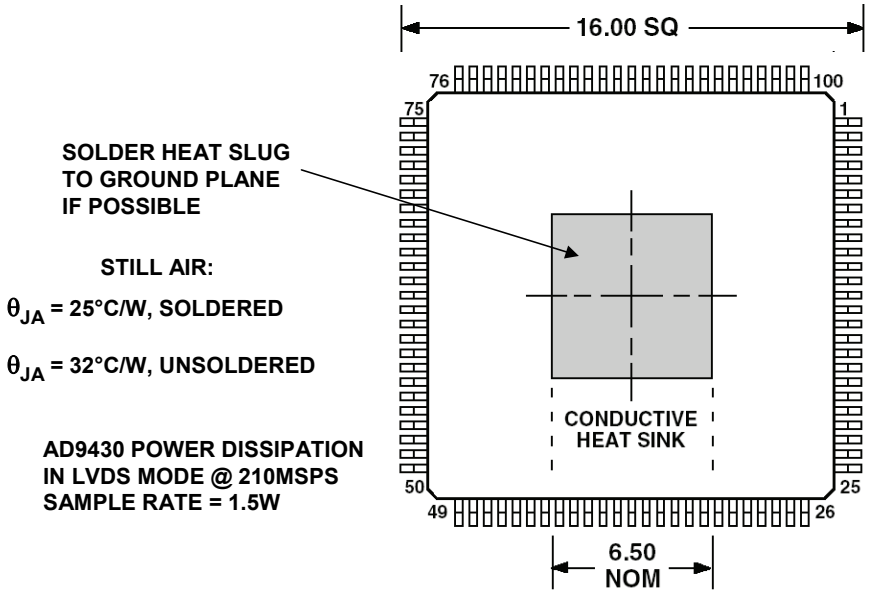


***Figure 12.81:*** *AD9430 100-Lead e-PAD TQFP*

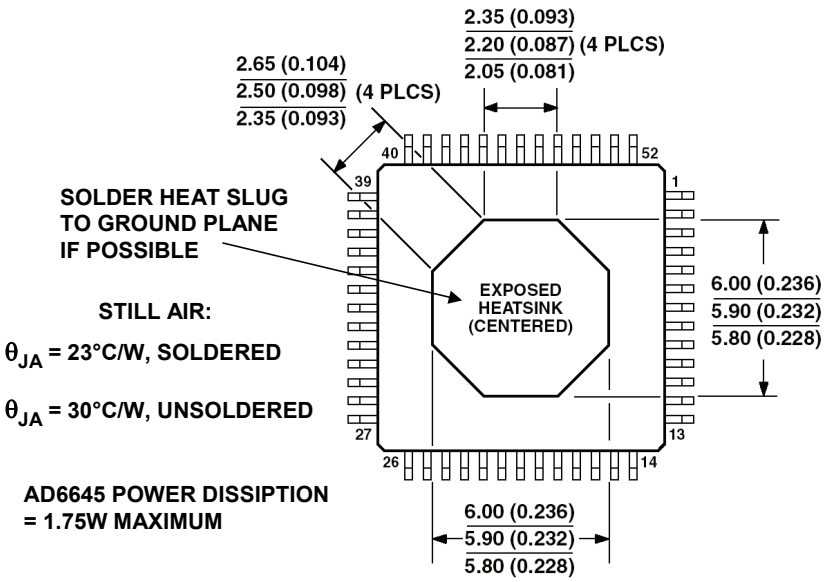


***Figure 12.82:*** *AD6645 52-Lead Power-Quad 4 (LQFP_ED) (SQ-52) Thermally Enhanced Package, Bottom View*

The AD6645 is a high performance 14-bit, 80 MSPS/105 MSPS ADC fabricated on a high speed complementary bipolar process (XFCB, and offers the highest SFDR (89 dBc) and SNR (75 dB). Although there is little variation in power as a function of sampling frequency, the maximum power dissipation of the device is 1.75 W. The package is a thermally enhanced 52-lead PowerQuad 4® with an exposed pad as shown in Figure 12.82.

It is recommended that the exposed center heat sink be soldered to the PC board ground plane to reduce the package $\theta_{JA}$ to 23°C/W in still air. For 1.75 W of power dissipation, this places the junction temperature 23°C × 1.75°C = 40.3°C above the ambient temperature. For a maximum operating temperature of +85°C, this places the junction at 85°C + 40.3°C = 125.3°C. The thermal resistance of the package can be reduced to 17°C/W with 200 LFPM airflow, thereby reducing the junction temperature to 30°C above the ambient, or 115°C for an operating ambient temperature of +85°C.

High speed CMOS DACs (such as the TxDAC® series) and DDS ICs (such as the AD985x series) also have clock-rate dependent power dissipation. For example, in the case of the AD9777 16-bit, 160-MSPS dual interpolating DAC, power dissipation is a function of clock rate, output frequency, and the enabling of the PLL and the modulation functions. Power dissipation on 3.3 V supplies can range from 380 mW ($f_{DAC}$ = 100 MSPS, $f_{OUT}$ = 1 MHz, no interpolation, no modulation) to 1.75 W ($f_{DAC}$ = 400 MSPS, $f_{DATA}$ = 50 MHz, $f_s/2$ modulation, PLL enabled). These and similar parts in the family are also offered in thermally enhanced packages with exposed pads for soldering to the PC board ground plane.

These discussions on the thermal application issues of op amps and data converters haven't dealt with the classic techniques of using clip-on (or bolt-on) type heat sinks. They also have not addressed the use of forced air cooling, generally considered only when tens of watts must be handled. These omissions are mainly because these approaches are seldom possible or practical with today's op amp and data converter packages.

The more general discussions within References 4-7 can be consulted for this and other supplementary information.

# REFERENCES: THERMAL MANAGEMENT

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2. Data sheet for **AD8016 Low Power, High Output Current, xDSL Line Driver**, Analog Devices, Inc., http://www.analog.com/.

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