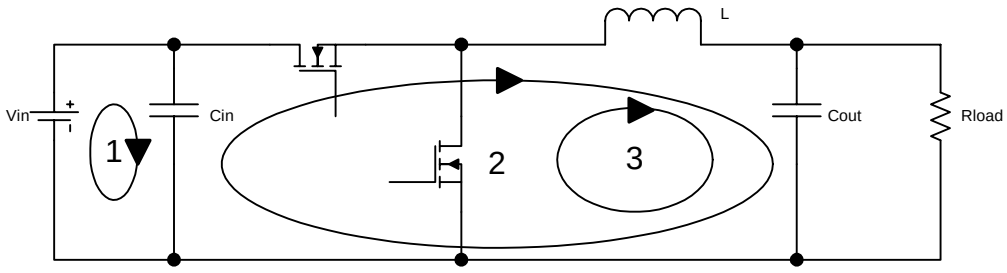
ENPIRION

Application Note

Printed Circuit Board Layout Considerations for the EN5310D, EN5330D, and EN5360D

With any switch mode power supply, proper layout of the printed circuit board is essential to prevent switching noise generated by the power supply from contaminating the rest of the circuit. Switching noise in the form of dI/dt, dV/dt and magnetic coupling can disturb sensitive analog or digital circuitry, especially circuits operating at RF frequencies. A poor layout can even cause the power supply itself to be inoperable.

Since the switching noise is generated primarily by the power stage of the supply, careful layout of the power components should take place before the small signal components are placed and routed. The basic strategy is to minimize the area of the loops created by the power components and their associated traces. In the synchronous buck converter shown below the input (source) loop #1 ideally consists of a DC current with a negligible AC ripple. Loop numbers 2 and 3 are the power switch loops. The current in these loops is composed of trapezoidal pulses with large peaks and fast edges (dI/dt and dV/dt). The area of these loops will be determined primarily by how close together the power components, the inductor, and the capacitors Cin and Cout can be placed. The closer the components, the shorter the PCB traces connecting them, and therefore the smaller loop area.



The Enpirion family of devices greatly simplifies the board layout because of the self-contained power switches and inductor. This means that the only external power components that need to be placed are the input and output filter caps, and the pinout of the part ensures that the area of the critical current loops is kept to a minimum.

Due to the high frequency of operation of the Enpirion power converters, circuit board layout is important to minimize input/output ripple and noise and radiated EMI. Proper layout requires attention primarily to two areas: (1) maintaining tight, well disciplined ac current loops on the input and output through the respective filter capacitors, and (2) creation of a “quiet” ground for referencing the dc input and output voltages, and properly bypassing of the I/O terminals to the quiet ground.

The first area of consideration requires that the input and output filter capacitors, which conduct sizable ac currents, be situated as close to the converter package as possible. Ideally, the input filter capacitors should connect the +Input with the Input Ground leads immediately adjacent to the package. Similarly, output filter capacitors should connect the +Output with the Output Ground leads where these leads exit the package. These “loops” should lie entirely on the same layer of metal on the PCB as the power converter.

The second area of consideration, a “quiet” ground, is probably best implemented by creating a ground layer in a multi-layer board. The converter package should be connected to this layer at a single “point”-- through the matrix of vias directly under the package. To minimize ac ripple voltage, noise and EMI on the input and output, bypass capacitors are placed between the respective input and output terminals and the “quiet” ground using vias as necessary to the appropriate layers of the PCB. These vias should be placed as close to the capacitor terminals as possible.

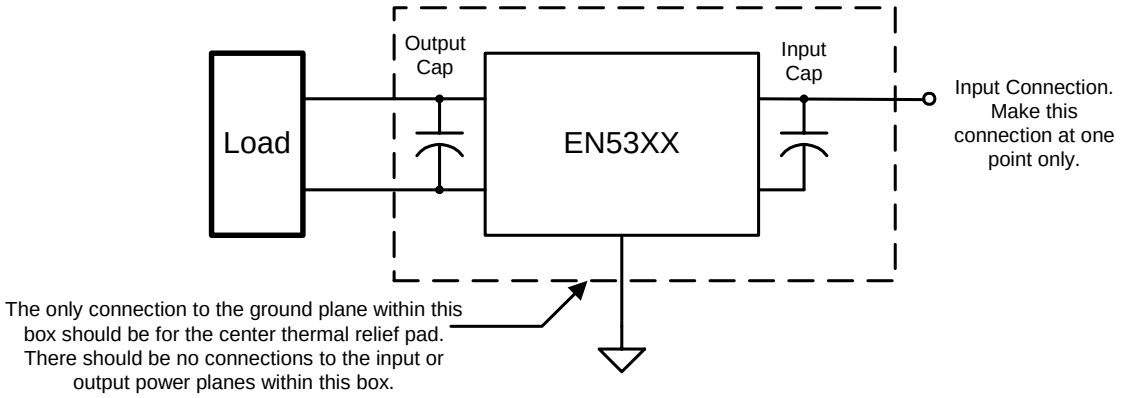
One of the most important performance parameters of a switching regulator is the output voltage ripple. The output voltage ripple has two main components: one at the fundamental switching frequency of the converter, and another caused by the fast switching edges resulting in voltage spikes at hundreds of megahertz. The large output filter capacitors right next to the output pins of the package keep the switching frequency component under control while providing energy storage for reasonable transient response. The larger the number of capacitors, the lower will be the fundamental ripple component. To control the high frequency spikes, additional smaller capacitors are also sometimes needed in parallel to the output filter capacitors. If the load is some distance away from the converter, additional capacitors will be needed at the load to bring down the fundamental and the switching spike components of the ripple. Usually these capacitors are the output terminal bypass capacitors to the quiet ground discussed above. The value and size of the capacitors needed at the load will depend a lot on the board layout and parasitic elements.

Capacitor choice for ripple and noise bypassing between the I/O terminals and the quiet ground should seek to minimize the overall capacitor impedance at the frequencies of interest. Using capacitors that are self-resonant at these frequencies can mean the difference between effective and ineffective bypassing. Many times different values of bypass capacitors are needed in parallel to bypass multiple ranges of noise frequencies. We recommend only ceramic multi-layer chip capacitors with the C0G (NP0), X7R, or X5R dielectric to be used with the Enpirion regulators.

Turn off the Auto-router and Do It Manually

Ideally, the power supply section of any circuit should be physically isolated from the rest of the circuit. Imagine if you will a small “island” of power supply circuitry that connects to the rest of the circuit through a single “land bridge”. Schematically, the power and ground nets are typically distributed throughout an entire design, including the power section. It is often difficult to prevent layout problems with the power section because the electrical rules check performed by the PCB design software cannot differentiate between the power/ground nets used by the power supply and those used by the rest of the circuitry because they are the same net.

As the figure below shows, the input and output filter capacitors should be placed on the same side of the PCB as the power IC and right next to the input and output pins of the package with no vias between the capacitors and the power IC. This will ensure that the high frequency current loops are minimized.



Since the power IC has fast switching signals, it is advisable to keep all sensitive signals as far away as possible from the device. If possible, try not to route any traces underneath the device. Ideally, only thermal ground planes should be underneath the power IC package. The thermal copper on top layer of the PCB should be the same size as the thermal pad on the device, and it should be filled with as many vias as possible. The size of the vias should be less than 0.3mm.

Analog vs. Power Ground

The Enpirion POL devices have two grounds: a single quiet AGND pin for the control section, and several PGND connections for the power section. The PGND connections consist of pins on the input side, on the output side, and a thermal pad underneath the package. All the PGND points are connected to each other inside the Enpirion package, and they need to be connected to AGND. This connection is made at only a single point on the PCB in order to prevent ground loops. AGND should go to the quiet ground on the PCB, usually one or more of the ground planes. The connection should be made using a via right next to the AGND pin. This via can also serve as a test point in case any signals needs to measured with respect to AGND. The ground plane on the PCB is then considered the quiet AGND plane for the power converter circuits. Any small-signal component that needs to be connected to AGND pin of the regulator only needs to be connected to the ground plane of the PCB in the vicinity of the Enpirion package.

The input PGND set of pins is very noisy due to high-frequency, trapezoidal AC currents with very fast rise and fall times, and these currents should be kept away from the quiet ground plane of the PCB as much as possible. For this reason, these pins should only go to the input filter capacitors, and no other point. Input dc power comes to these pins and the input capacitors from the ground plane to the thermal PGND pad and through internal Enpirion module connections.

The output PGND pins are also quite noisy due to the high-frequency triangular inductor ripple current going through them. There should be a direct connection from these pins to the output capacitors. If the application allows, the ground connection from the output capacitors should then continue directly to the load ground without going to any other point in the PCB. This type of a direct connection minimizes the parasitic inductance between the output capacitors and the load.

The input PGND pins should not be connected to the output PGND pins on the PCB. None of the PGND pins should also be connected to the thermal PGND pad on the PCB. These connections are all made inside the Enpirion module. The thermal PGND is then to be connected to the quiet ground plane through the thermal vias

underneath it. This connection establishes the single point connection between PGND and AGND, and minimizes the amount of switching noise induced on the quiet ground.

Remote Sensing Capability

Remote sensing gives the system designer the ability to achieve the best possible regulation at the load. In order to avoid any stability problems, the inductance between the last output capacitor and the load should be minimized. This can be achieved by making the positive and ground connections between the converter and the load with very wide copper pours. The connection from the load to the VSENSE pins should also be made as thick as possible. It should also be kept away from any noisy circuits that could contaminate it.

Loop Compensation

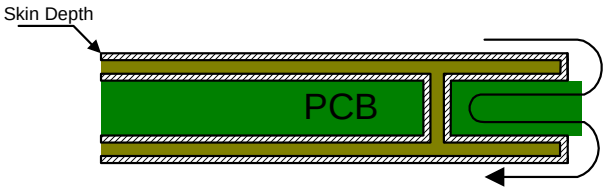
The Enpirion devices are all internally compensated to achieve stable operation through all operating conditions. Since the control loop includes the output capacitors and any connections up to and including the load, some applications may require adjustments to the compensation circuit. For this reason, three pins (COMP, EAIN, and EAOUT) are made available. Most applications will not require adjustments to the compensation. We do, however, recommend adding through-hole test points next to each of these pins. These test points can be used to observe the control loop behavior and perform any troubleshooting on the hardware if needed. The control signals should be measured with respect to the AGND test point.

Radiated EMI Requirements

One of the most prevalent radiated EMI requirements is the EN55022. Most electronic systems need to pass the level B specification of this requirement. The test is done using a calibrated antenna at 3 or 10 meters away from the equipment. The frequency range of the test is from 30MHz to 1GHz. Following the guidelines mentioned above will help an electronic system consisting of a POL switching regulator meet the radiated EMI specifications. For the Enpirion POL converters, small 0603 C0G (NP0) ceramic capacitors with values in the range 100-1000pF should be used in parallel with the larger input filter capacitors between the PVIN and PGND pins of the package. In order to add further suppression of the switching signals causing the radiated EMI, the 100-1000pF capacitors can also be used as bypass caps at the input terminal of any PCB which has the Enpirion POL converters assembled on it.

Some Notes on the Use of Vias

As the switching frequency of power converters increases, it is necessary to consider skin effect when laying out the power path. High frequency AC currents do not flow through a conductor evenly as does DC current. The depth of penetration of the conductor is a function of the frequency and conductor material. The use of through hole vias to carry high frequency currents can increase the length of the current path, and can also cause noise contamination of power planes even though the component placement and layout appear optimized from a DC standpoint. It is also important to use enough vias, both to carry high currents and to provide redundancy to the power connection. An absolute minimum of two vias is recommended for the input power, input ground, output power and output ground connections.



AC current can only penetrate the conductor to the skin depth, forcing high frequency currents to flow around the edge of the trace instead of through a via filled with solder. This causes an increase in the length of the current path.

In order to determine the skin depth in a PCB trace, use the following calculation:

Skin Depth: $\Delta = \frac{k}{\sqrt{f}}$

Where: $k = 6.58 \frac{cm}{\sqrt{Hz}}$ Copper at 20ºC

$\Delta = skindepth(cm)$

$f = frequency(Hz)$

In a flat copper conductor, the skin depth at 5MHz is 0.029mm at 20ºC. A PCB trace made of 1 ounce copper is 0.034mm thick.

Vias are also necessary to carry heat out of the package to other PCB layers where it can be dissipated. As shown in the sample layout, an array of vias under the center pad of the part connects to the solder side ground plane. This ground plane then acts as a heat sink for the part.

Layout Recommendations

The recommendations shown in this section are for the Enpirion DFN, laminate package, POL converters. These products consist of the EN5310, EN5330, and EN5360. Since all these packages are very similar to each other, the layout guidelines below can be applied to all of them. The recommendations only show the critical input and output filter capacitors. The table below shows the values of these capacitors for the three POL products:

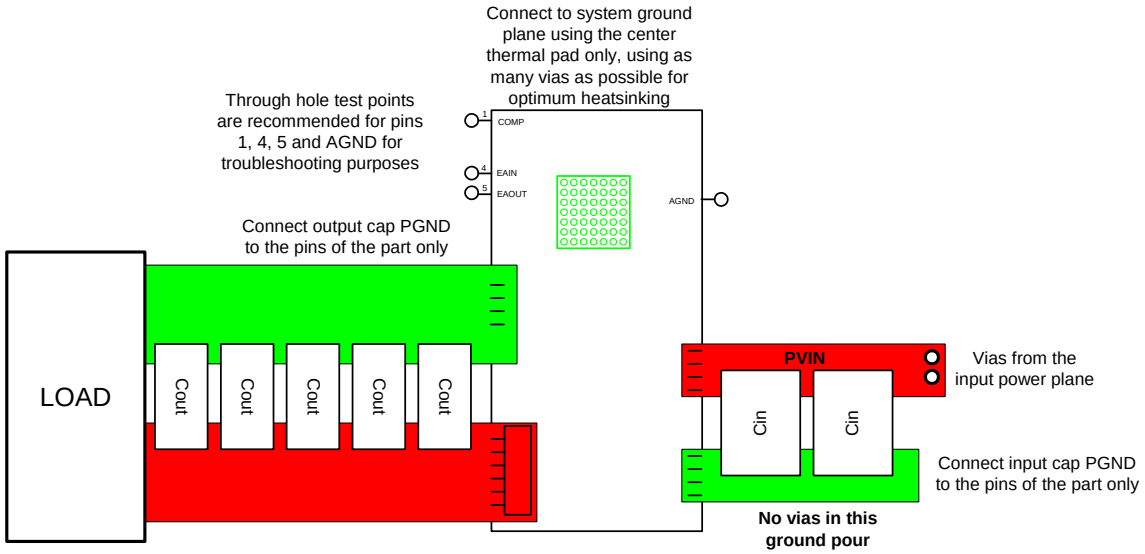
Product	Input Capacitor		Output Capacitor	
	Total Capacitance	Optimum Solution	Total Capacitance	Optimum Solution
EN5310	10uF, 10V	Single 10uF, 1206	20uF, 6.3V	2x10uF, 1206
EN5330	22uF, 10V	Single 22uF, 1210	50uF, 6.3V	5x10uF, 1206
EN5360	44uF, 10V	2x22uF, 1210	50uF, 6.3V	5x10uF, 1206

Table 1: Input and output capacitor configuration for the Enpirion POL switching regulators

In all the recommendations below the load has been shown adjacent to the output filter capacitors. We realize this represents a best-case scenario that may not always be achievable. Nevertheless, the recommendations below present a relative comparison among different options.

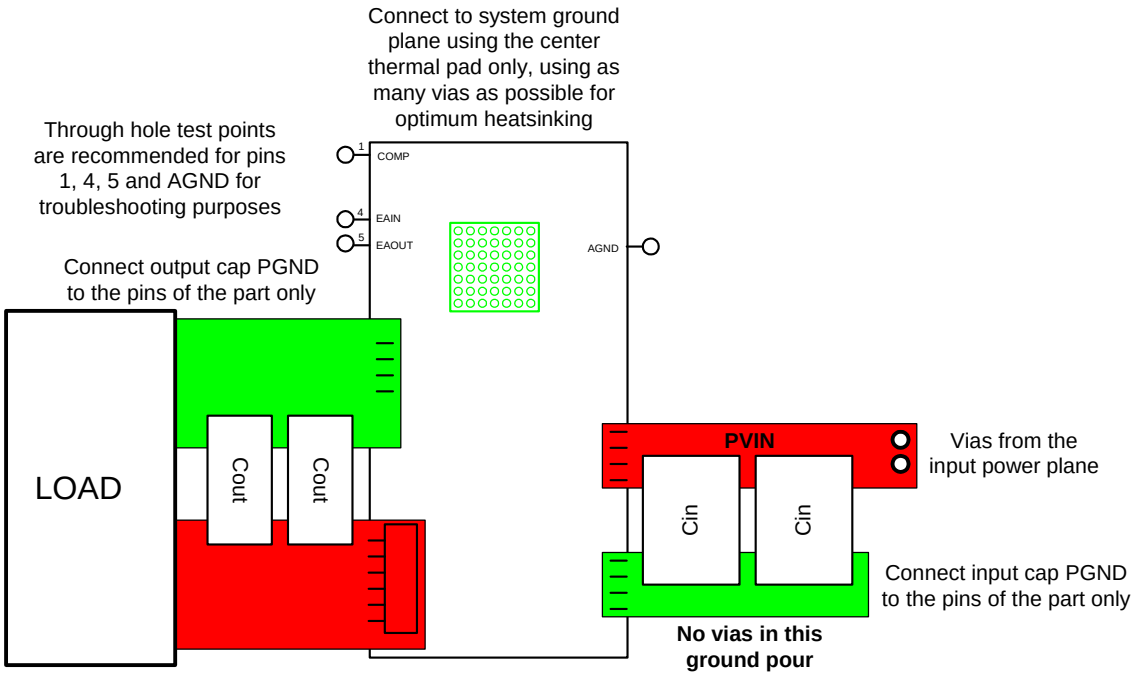
Optimum Performance Layout

This layout results in the best output ripple with the least amount of parasitic inductance in the output. However, it takes up the most footprint on the PCB. For the EN5310, assume only two output capacitors for all the layout recommendations. For both the EN5310 and EN5330 assume only one input capacitor for all cases.



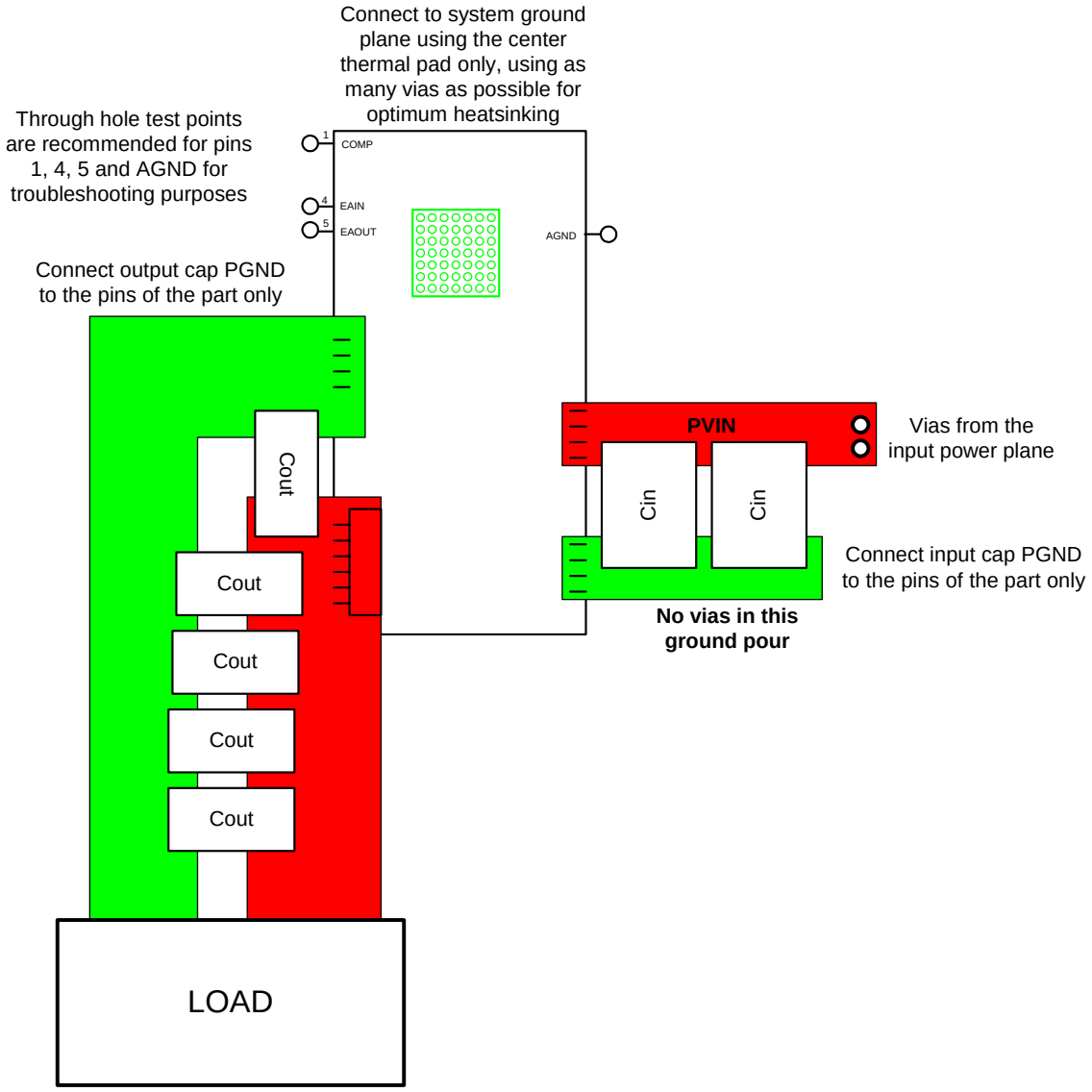
Minimum Footprint Layout

This layout cuts down on the number of output capacitors for EN5330 and EN5360. It takes up less footprint, but the output ripple voltage will be higher. Some smaller filter capacitors could be used to further reduce the ripple if needed.



Vertical Output Capacitor Placement

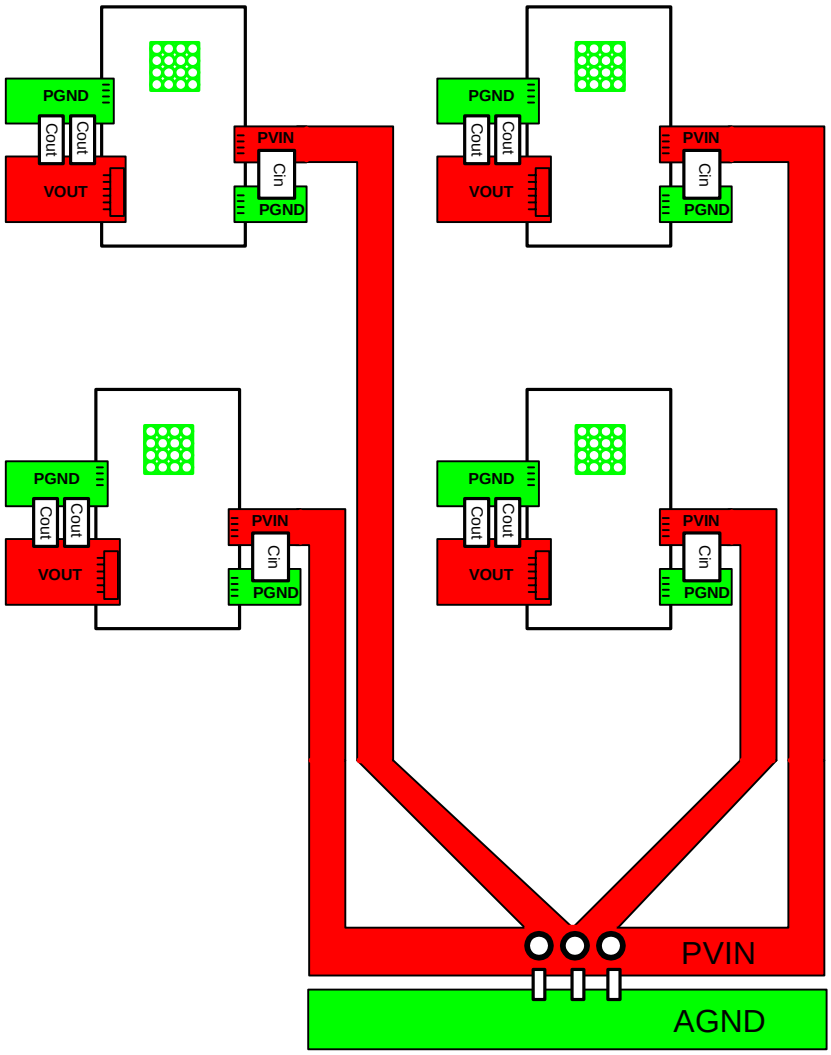
This layout still employs 5 output capacitors, but arranged to use the PCB footprint more efficiently. The parasitic inductance in the output is slightly higher than the previous layout.



Notes on Laying Out Multiple Converters (see picture on next page)

When laying out multiple converters in close proximity to each other, care must be taken to avoid crosstalk between the converters. Crosstalk between multiple converters operating at slightly different switching frequencies will result in low frequency noise appearing on the output, effectively increasing the output voltage ripple amplitude.

In order to isolate the converters from each other, it is necessary to separate the input voltage connections going to each converter and connecting them together in a star configuration right at the point where the input comes into the circuit, usually this is a connector of some sort. It is also helpful to bypass high frequency noise generated by the switching converters to ground using one or more high quality ceramic capacitors from Vin to AGND at the star connection point. A 1µF 0603 size capacitor has a resonant frequency close to the 5MHz switching frequency of the EN53X series converters, and thus provides optimum bypassing. The ground connection at the star point is considered AGND because it removed from the switching grounds of the input capacitors of the converters. All the high-frequency AC current is in the PGND copper of each converter, and only the dc current flows through the AGND.



One or more 1uF 0603 size capacitors from PVIN to AGND right at the star connection point will help eliminate crosstalk

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