BY EDISON FONG • NATIONAL SEMICONDUCTOR

PCB-layout techniques for gigasample ADCs

WHEN A MULTILAYER BOARD OPERATES AT SPEEDS GREATER THAN A FEW HUNDRED MEGAHERTZ, IT'S A CHALLENGE TO MAINTAIN SIGNALS WITHOUT MISMATCHES, LOSSES, DISTORTION, OR EMI. FOLLOW THESE GUIDELINES FOR PCB LAYOUT TO PRESERVE SIGNAL INTEGRITY AND ACHIEVE HIGH-SPEED PERFORMANCE.

As a general rule, when a design's speed rises to more than a few hundred megahertz, it requires a PCB (printed-circuit board) with four or more layers. The only exception occurs when the design uses small boards; in that case, a two-layer board may be acceptable. Developers typically perform these designs on evaluation boards for baluns, chip capacitors, resistors, and other small components.

Any board using a BGA (ball-grid array) with hundreds of pins can use no fewer than eight layers and typically uses more than 10 layers. The number of pins on the package of the largest chip on the board often determines the number of layers on a board. For example, National Semiconductor's (www.national.com) ADC10D1000 reference board comes in a 300-pin BGA package; the Xilinx (www.xilinx.com) Virtex-4 FPGA on the board is a 668-pin BGA. This arrangement requires at least an eight-layer board for a designer to gain access to all the pins. Given this constraint, you must also explore what other advantages the situation brings to the board design. It is no accident that you can achieve 10-bit performance with a 3-GHz sample rate on a board having multiple microwave signals, high-speed FPGAs, switching power supplies, and low-noise analog lines.

Nelco NP4000-6 epoxy from Park Electrochemical Corp (www.parkelectro.com) is a good material choice for designs requiring low loss and high durability. This material has a similar dielectric constant to that of conventional FR (fire-retardant)-4 board material, but Nelco 4000 provides better high-frequency performance. Another advantage of Nelco 4000 material is that you can use it for all layers, not just the top and bottom layers as with other microwave-PCB dielectrics, such as Teflon. The ADC10D1000 uses a 10-layer board. National Semiconductor also fabricated an identical board in FR-4 material, and, in some ways, this approach is better if the application can tolerate signal losses. Because of the higher loss tangent of FR-4, matching is less critical, providing for a better S_{11} reflection coefficient because FR-4 absorbs much of the signal that would cause reflections in the transmission line. However, lines in these designs should be no longer than 3 in. The difference between Nelco and FR-4 is negligible for the digital interface to the FPGA because the frequencies are lower than 2 GHz.

DDi Silicon Valley Division — **Pre-Release Stackup Report** — Pre-Release #: P22798A

Cust: DDI - Milpitas — Total Layers: 10

Part #: NATIONAL SEMI 10 LAYERS — Rev -

Finished Thickness: 0.0620 +/- 0.0060 — Finished Over: All

Lam Thickness: 0.0580 +/- 0.0030 — Material Type: NP 4000-6

Impedance Requirements:

L#	Impedance Type	Orig Line	Fin. Line	Ref Pln	2nd Ref Pln	Targeted Desired Impedance	Impedance Tolerance	Actual Calculated Impedance	Diff Line Centers	Diff Line Space	Original Coplanar Spacing	Finished Coplanar Spacing
1	DIF-Coated Microstrip Edg Cpld		.00325	2		100.00 Ω	+/- 10%	101.23 Ω	.01000	.00675		
1	SE-Coated Microstrip		.00425	2		50.00 Ω	+/- 10%	49.64 Ω				
3	DIF-Stripline Edg Cpld		.00400	2	4	100.00 Ω	+/- 10%	100.87 Ω	.00800	.00400		
3	SE-Stripline		.00600	2	4	52.00 Ω	+/- 10%	51.30 Ω				
6	DIF-Stripline Edg Cpld		.00400	7	5	100.00 Ω	+/- 10%	100.87 Ω	.00800	.00400		
6	SE-Stripline		.00600	7	5	52.00 Ω	+/- 10%	51.30 Ω				
8	DIF-Stripline Edg Cpld		.00400	9	7	100.00 Ω	+/- 10%	100.87 Ω	.00800	.00400		
8	SE-Stripline		.00600	9	7	52.00 Ω	+/- 10%	51.30 Ω				
10	DIF-Coated Microstrip Edg Cpld		.00325	9		100.00 Ω	+/- 10%	101.23 Ω	.01000	.00675		
10	SE-Coated Microstrip		.00425	9		50.00 Ω	+/- 10%	49.64 Ω				

Controlled Impedance Notes:

Lamination Stackup:

L#/Type	Description:	Thickness and Tolerances: Cu+:	Laminate/PrePreg:		Base Material Rqmts: Type: Description:	Dk @ 1Ghz
1 Sig	Foil (H oz)	.00060				
	Pre-Preg (1 x 1080)		.0027	+/- 0.0003	NP 4000-6	3.9
2 Pln	Core 0.0060 1/H	.00120	.0060		NP 4000-6	
3 Sig		.00060				4.1
	Pre-Preg (1 x 2113)		.0080	+/- 0.0008	NP 4000-6	4.18
	Pre-Preg (1 x 2116)					
4 Pln	Core 0.0030 1/1	.00120	.0030		NP 4000-6	
5 Pln		.00120				4.35
	Pre-Preg (1 x 2116)		.0080	+/- 0.0008	NP 4000-6	4.18
	Pre-Preg (1 x 2113)					
6 Sig	Core 0.0060 H/1	.00060	.0060		NP 4000-6	
7 Pln		.00120				4.1
	Pre-Preg (1 x 2116)		.0080	+/- 0.0008	NP 4000-6	4.18
	Pre-Preg (1 x 2113)					
8 Sig	Core 0.0060 H/1	.00060	.0060		NP 4000-6	
9 Pln		.00120				4.1
	Pre-Preg (1 x 1080)		.0027	+/- 0.0003	NP 4000-6	3.9
10 Sig	Foil (H oz)	.00060				

Target Post-Lam Thickness: 0.0580 +/- 0.0030

Copper Oz Legend: H=1/2oz T=3/8oz Q=1/4oz E=1/8oz S=1/16oz

Stackup Notes:

***Laser drilled microvias 1-2

PLEASE RETURN APPROVED STACK-UP TO DDI WITH DATA SET PRIOR TO MANUFACTURING

Figure 1 This stackup report gives the dimensions for matched impedance for both surface (microstrip) and embedded (stripline) transmission lines (courtesy DDI).

Before beginning any layout, you must obtain the stackup data from the PCB manufacturer because the data gives the dimensions for matched impedance for both surface (microstrip) and embedded (stripline) transmission lines. **Figure 1** shows stackup data from DDI (www.ddiglobal.com). Other manufacturers offer similar data. Matched lines are critical for high-frequency signals. Ideally, you want coaxial cable, but this choice is not economical except for the most critical applications, such as military, high-end commercial, or aerospace equipment. The cost is typically prohibitive in consumer applications, so with multilayer PCBs, stripline or microstrip rather than expensive miniature coaxial cable is your best option.

Impedance is constant in coaxial cable because the surrounding ground shield is at a constant distance from the center conductor. This situation translates to a constant velocity factor and thus uniform speed of the wave traveling inside the coaxial cable. The coaxial cable presents the best impedance match to a signal. If multiple signal lines are close together on a PCB with limited space, you should use ultrathin coaxial cables, such as 50Ω SRC023, with an outside diameter of 23 mils, for high-performance transmission and isolation. You layer this coaxial cable on the surface of the PCB. Again, using this cable for consumer applications is cost-prohibitive, and this technique finds use primarily in satellite and military applications in which dozens of high-frequency signals must transmit in a small space.

If using coaxial cable is impractical, one possible choice is the use of a microstrip (**Reference 1**). The basic principle of this technique is that you use the horizontal trace contributing to the inductance and the trace above the ground plane to calculate the square root of the inductance divided by the capacitance. A given width for a given thickness yields an impedance. In coaxial cable, the wave travels with 100% uniform surroundings; the outer-shield conductor is at a constant distance from the center conductor. You cannot duplicate this topology on a PCB microstrip.

Microstrip improves on using just a "random" trace but is far from ideal. Even if you precisely calculate the trace width and precisely consider the trace's height from the ground plane, it does not even approach a perfect match. The intuitive explanation, without introducing Maxwell's field equations, is that the dielectric below the trace is thicker than air. The dielectric above the trace is air. Take, for example, FR-4, with a dielectric constant of approximately four. The wave traveling in the dielectric travels at approximately half the speed of that in air. Thus, microstrips cannot work over long distances. The signal above the trace travels at twice the speed of that in the dielectric. However, sometimes you have no other choice; for runs of less than a quarter-wavelength, using microstrip is a viable alternative. For long runs, the mismatch dominates, so you cannot use microstrip. There are times when you cannot avoid using microstrip, such as when you must connect an SMA connector, when your design requires surface test points, or when the design has only a two-layer PCB.

Another improvement is the use of balanced differential lines over the ground plane. Two lines have equal and opposite currents, ideally canceling the external field. This cancellation makes this type of transmission line less dependent on the ground planes than a single-conductor microstrip would be. However, the differential lines lack the enclosure of coaxial cable. In a differential microstrip, the ground plane is only partially responsible for the matching (**Figure 2**). Most of the matching depends on the conjugate line. This technique is still vulnerable to both radiating and receiving interference

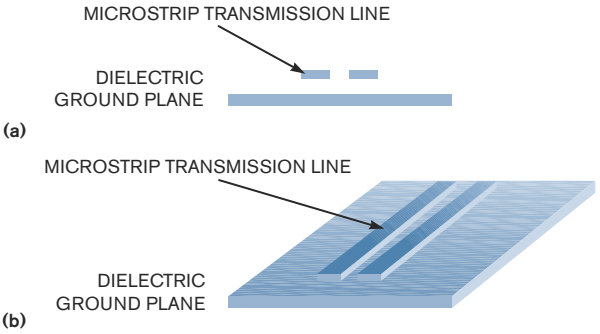


Figure 2 In a side view (a) and a perspective view (b) of the differential microstrip line, the ground plane is only partially responsible for the matching. Most of the matching depends on the conjugate line.

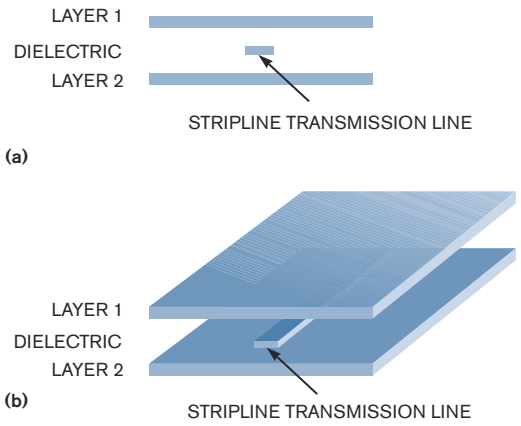


Figure 3 Conventional single-ended stripline in a side view (a) and a perspective view (b), although an improvement over microstrip, is still not ideal.

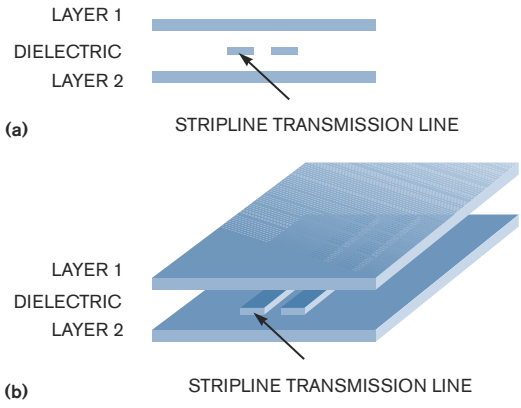


Figure 4 Differential stripline offers good matching and excellent EMI shielding in both a side view (a) and a perspective view (b).

signals. On a two-layer PCB, it is the best choice other than using rigid coaxial cable. It does require almost twice as much area, however.

The solution to the microstrip issue is to use striplines sandwiched between two planes (**Figure 3**). This approach allows for a uniform dielectric around the transmission line. However, it still does not provide uniform return ground for the conductor. It does not have coaxial cable's major advantage—that the ground shield surrounds the signal line by 360°. In the case of the stripline, only the top and bottom provide for the ground return. Another advantage of using striplines is that they have shielding from the outside world, preventing not only interference but also unnecessary radiating signals. The match, although better, does not rival the performance of coaxial cable. As in the case of microstrip, differential lines improve performance at the expense of occupying more space (**Figure 4**).

The ADC10D1000 uses impedance-matched differential stripline with equal and opposite currents on each line. The matching depends on the thickness of the dielectric, the dielectric constant of the material, and the spacing and thickness of the balanced line. You obtain all of this information from the PCB manufacturer. Using this approach and embedding the stripline between two power-supply or ground planes makes the EMI (electromagnetic interference) too small to measure.

The entire system on the ADC-10D1000 reference board is fully differential, taking advantage of not only the chip's CMR (common-mode rejection) but also the matching of impedances from the outside world to the input of the chip. The drawback of this approach is that it almost doubles complexity. The thermal noise increases in quadrature due to the increase in total active components, and power consumption increases accordingly. You would be lucky to retrieve even 6 bits in a 1G-sample, single-ended architecture.

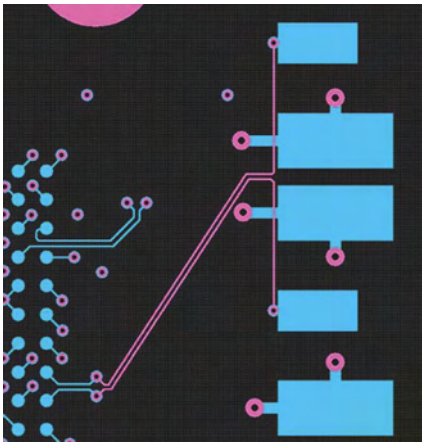


Figure 5 You must immediately bring together the positive and negative input-voltage signals to conform to the 100Ω balanced transmission line.

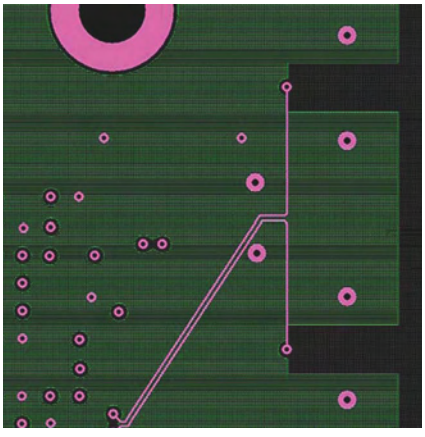


Figure 6 The general rule is to keep the balanced transmission line intact as long as possible to maintain matching. You must remove the green ground layer underneath the SMA landing pad, Layer 2, because it would form a large capacitor with the landing pad. This board has no conducting material under the SMA landing pad until Layer 7. Layer 7 must be an ac ground for proper impedance matching.

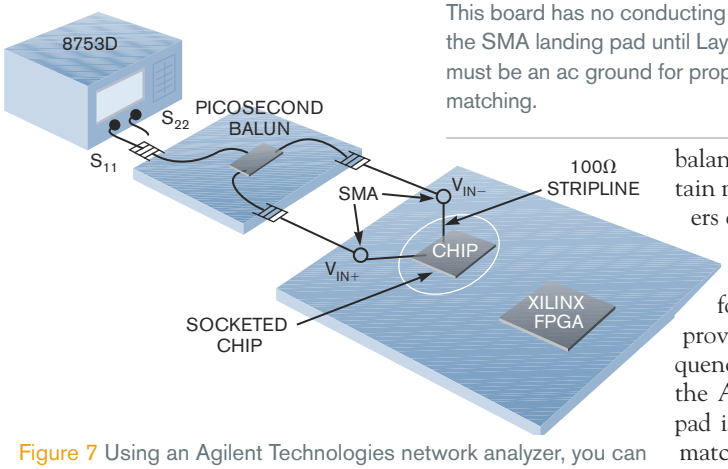
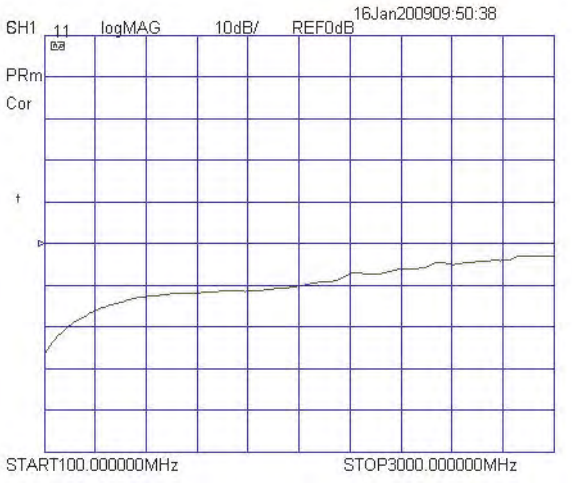


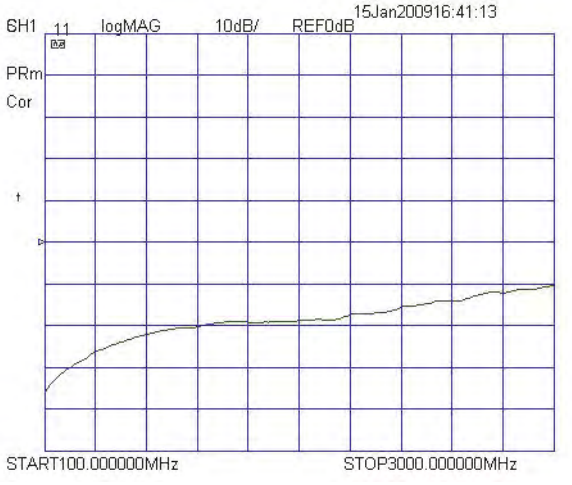
Figure 7 Using an Agilent Technologies network analyzer, you can achieve better than −10-dB return loss at frequencies as high as 3 GHz.

Early in the design cycle of the ADC-10D1000, its designers determined that the input interface would be as simple as possible, placing any baluns, amplifiers, and relays outside the board. They also used no relays or unnecessary traces because all these components would degrade the performance of the board. The following general approach achieves good matching and provides for the broadest bandwidth with minimal EMI. From the input pins of the ADC, immediately place vias and move down at least one layer for the transmission line. In the case of the ADC10D1000, designers chose Layer 3 as the transmission line. This layer forms the heart of the stripline transmission line, with layers 2 and 4 as the ac ground, shielding the signal from outside interference. Because it is a balanced stripline, it maintains its impedance for longer distances than does an open, single-trace, unbalanced surface transmission line.

You must immediately bring together the positive and negative input-voltage signals to conform to the 100Ω balanced transmission line (**Figure 5**). This step is critical for good performance. At the SMA-connector end, the via comes back up to the surface layer. The general rule is to keep the balanced transmission line intact as long as possible to maintain matching (**Figure 6**). Another major rule, which designers often overlook, is the impedance matching of the SMA connector to the PCB. Although the SMA connector itself is matched to 50Ω, the landing pad on the PCB for the SMA connector is not. Unless you make special provisions, the performance of the board deteriorates at frequencies greater than 1 GHz. With the SMA connectors that the ADC10D1000 reference design uses, the SMA landing pad is about four times wider than a 50Ω trace. For a 50Ω match, the associated ground plane is Layer 7. You must remove the metal on layers 2 through 6.

Using these layout rules, you can achieve superb broadband matching. Using an Agilent Technologies (www.agilent.com)





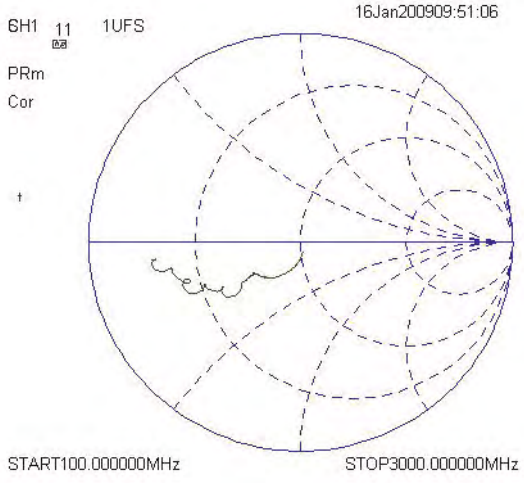


Figure 8 The S_{11} of the input match with a 100Ω termination resistor without removing layers 2 through 6 works at frequencies as high as 1.5 GHz.

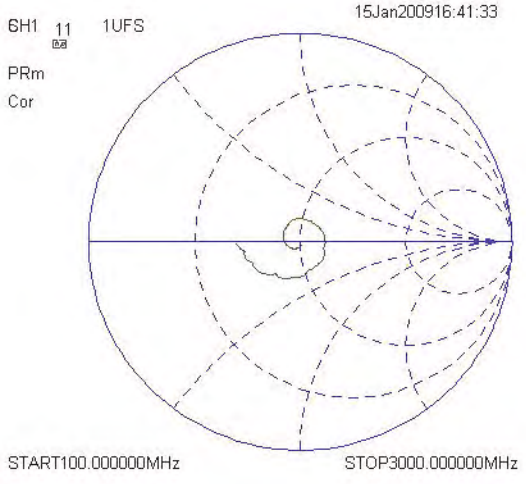


Figure 9 With layers 2 through 6 blank under the SMA landing pad, this layout is a dramatic improvement and is usable at frequencies as high as 3 GHz.

8753D network analyzer, you can achieve better than −10-dB return loss at frequencies as high as 3 GHz (**Figure 7**). **Figure 8** shows the S_{11} of the input match with a 100Ω termination resistor without removing layers 2 through 6. The matching works at frequencies as high as 1.5 GHz. **Figure 9** shows the same layout with the removal of layers 2 through 6. It is a dramatic improvement and is usable at frequencies as high as 3 GHz. **Figure 10** shows the input match with the ADC10D1000 in place. The worst-case return loss is better than −12 dB at 100 MHz to 3 GHz.

The exact amount of ground plane to remove from layers 2 through 6 is a subject of debate. Layers 2 through 6 contribute to the impedance of the landing pad even if you remove them. Not all of the fields from the SMA landing pad terminate on Layer 7; some terminate on layers 2 through 6. A 2-D field-solver program can solve many of the details and determine clearance. If a field-solver program is unavailable, you can get this data for SMA landing pads from any reputable PCB vendor. The vendor should be able to provide this information for the exact dimensions for its process. If neither of these options is available, clear each layer—layers 2 through 6, for example—by three to five widths of the stripline conductor (**Figure 11**).EDN

REFERENCE

1 Wheeler, HA, "Transmission-line properties of parallel strips separated by a dielectric sheet," *IEEE Transactions on Microwave Theory and Techniques*, Volume 13, Issue 2, March 1965, pg 172, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?tp=&arnumber=1125962&isnumber=24900.

AUTHOR'S BIOGRAPHY

Edison Fong is an instructor at the University of California—Berkeley Extension School, where he teaches courses in radio frequency and acts as a consultant on chip design and board-level design. Previously, he worked at National Semiconductor. He holds nine patents and has published more than 30 papers. Fong received bachelor's and master's degrees in electrical engineering from the University of California—Berkeley, a degree in engineering science from the University of Santa Clara (Santa Clara, CA), and a doctorate from the University of San Francisco. His personal interests include ham radio, photography, bicycling, and jogging.

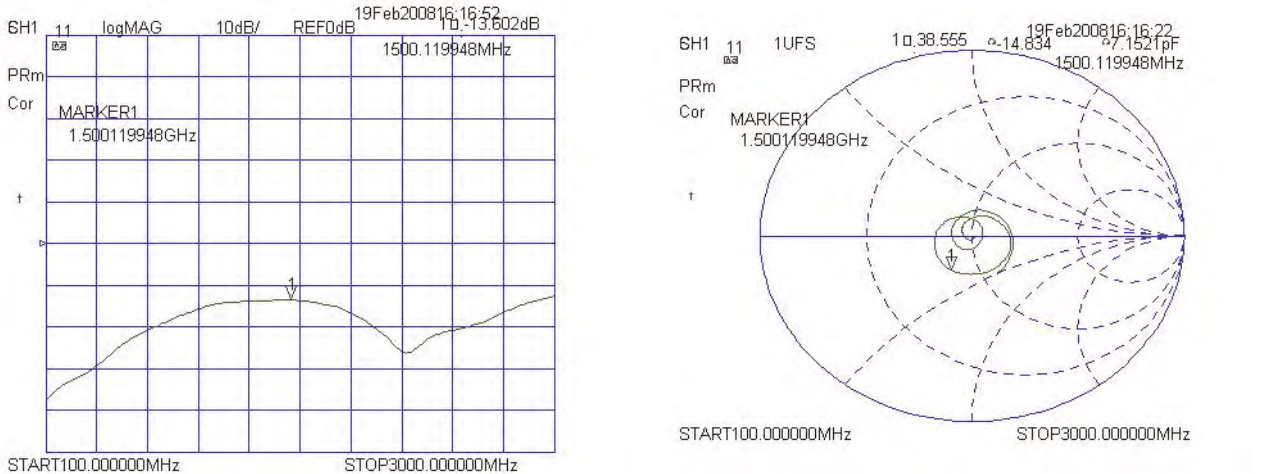


Figure 10 With the ADC10D1000 in place, the worst-case return loss is better than −12 dB at 100 MHz to 3 GHz.

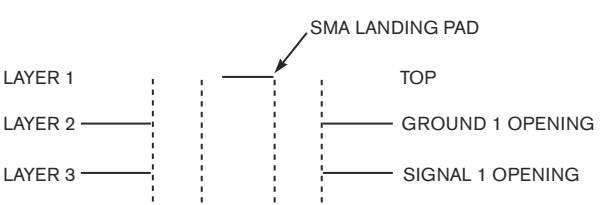


Figure 11 The exact amount of ground plane to remove from layers 2 through 6 is a subject of debate. If a field-solver program or data from the PCB vendor is unavailable, clear each layer with three to five widths of the stripline conductor.