BY HENRY J ZHANG • LINEAR TECHNOLOGY CORP

PCB-layout considerations for nonisolated switching power supplies

A GOOD LAYOUT DESIGN OPTIMIZES EFFICIENCY, ALLEVIATES THERMAL STRESS, AND MINIMIZES THE NOISE AND INTERACTIONS AMONG TRACES AND COMPONENTS. IT ALL STARTS WITH THE DESIGNER'S UNDERSTANDING OF THE CURRENT-CONDUCTION PATHS AND SIGNAL FLOWS IN THE SUPPLY.

The best news when you power up a prototype supply board for the very first time is that it not only works, but also runs quiet and cool. Unfortunately, that is not always the case.

A common problem with switching power supplies is "unstable" switching waveforms. Sometimes, waveform jitter is so pronounced that the magnetic components generate audible noise. If the problem is related to the printed-circuit-board layout, identifying the cause can be difficult. That is why proper PCB layout at the early stage of a switching-power-supply design is critical.

The power-supply designer best understands the technical details and functional requirements of the supply in the final product. Thus, from the outset of the board-design project, the power-supply designer should work closely with the PCB layout designer on the critical supply layout.

A good layout design optimizes supply efficiency and alleviates thermal stress; most important, it minimizes the noise and interactions among traces and components. To achieve those goals, the designer must understand the current-conduction paths and signal flows in the switching power supply. Keep the following design considerations in mind to achieve a proper layout design for nonisolated switching power supplies.

THE LAYOUT PLAN

To achieve the best voltage regulation, load transient response, and system efficiency for an embedded dc/dc supply on a large board, locate the supply output near the load devices to minimize the interconnection impedance and the conduction voltage drop across the PCB traces. Ensure good airflow to limit the thermal stress; if forced-air cooling is available, locate the supply close to the cooling fan.

In addition, the large passive components, such as inductors and electrolytic capacitors, should not block the airflow to low-profile, surface-mount semiconductor components such as power MOSFETs or PWM controllers. To prevent the switching noise from upsetting other analog signals in the system, avoid routing sensitive signal traces underneath the supply if possible; otherwise, you will need an internal ground plane between the power-supply layer and the small-signal layer for shielding.

It's important to plan out your power-supply location and board real-estate requirements during the system's early design and planning phase. Designers sometimes ignore that advice and focus first on more "important" or "exciting" circuits on the big system board. Treating power management as an afterthought and relegating the supply to whatever space is left on the board are contrary to achieving an efficient and reliable power-supply design.

For multilayer boards, it is highly desirable to place the dc ground or dc input- or output-voltage layers between the high-current, power-component layer and the sensitive, small-signal trace layer. The ground or dc voltage layers provide ac grounds to shield the small-signal traces from noisy power traces and power components.

As a general rule, the ground or dc voltage planes of a multilayer PCB should not be segmented. If you find that such segmentation is unavoidable, minimize the number and

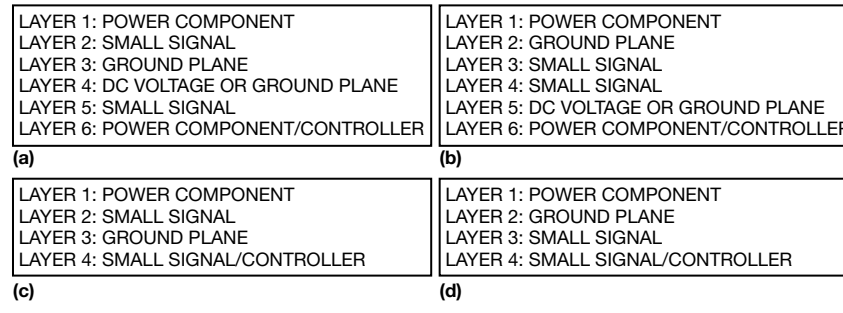


Figure 1 Undesirable layer arrangements for six- (a) and four-layer (c) switching-power-supply PCBs sandwich the small-signal layer between the high-current power layer and the ground layer. In desirable arrangements for six- (b) and four-layer (d) designs, the ground layers shield the small-signal layers.

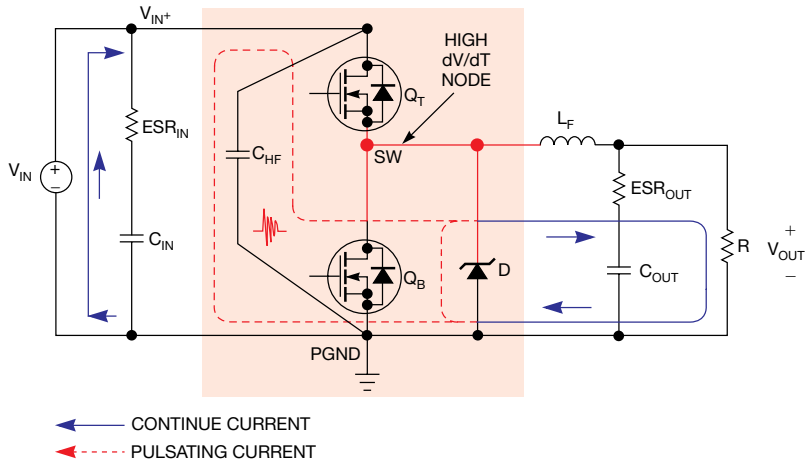


Figure 2 The solid line represents the continuous-current paths in a synchronous buck converter; the dashed line represents the pulsating (switching)-current paths.

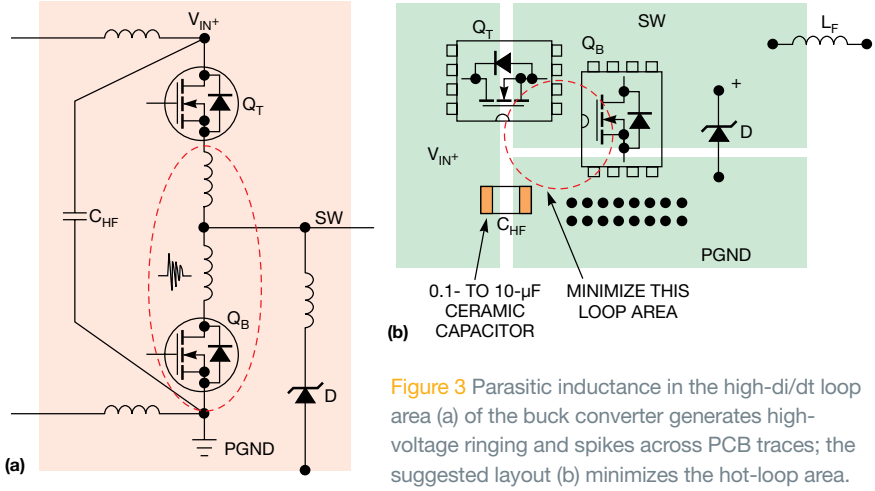


Figure 3 Parasitic inductance in the high-di/dt loop area (a) of the buck converter generates high-voltage ringing and spikes across PCB traces; the suggested layout (b) minimizes the hot-loop area.

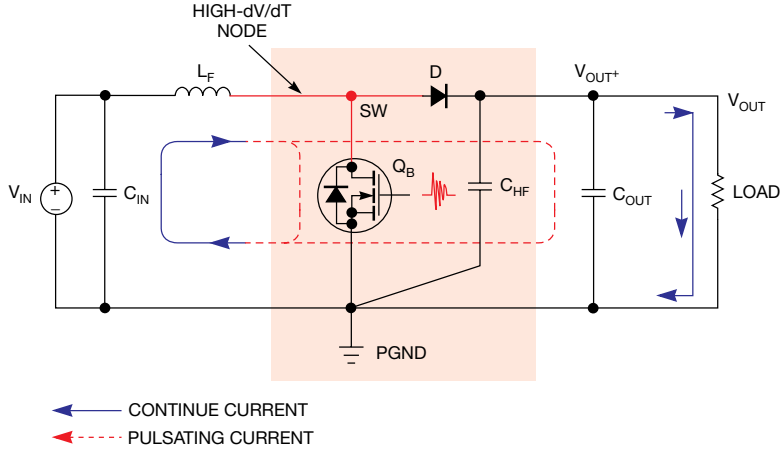


Figure 4 The continuous- and pulsating-current paths in the boost converter are shown. The high-frequency ceramic capacitor, C_{HF}, should be placed on the output side close to the MOSFET, Q_B, and boost diode, D.

length of traces in those planes, and route the traces in the same direction as the high-current-flow direction to minimize the impact.

Figures 1a and **1c** illustrate undesirable layer arrangements for six- and four-layer switching-power-supply PCBs, respectively. The configurations sandwich the small-signal layer between the high-current power layer and the ground layer, thereby increasing capacitive-noise coupling between the high-current/voltage power layer and the analog small-signal layer.

In **figures 1b** and **1d**, respectively illustrating desirable layer arrangements for minimizing noise coupling in six- and four-layer PCB designs, the ground layers shield the small-signal layers. It is important always to have a ground layer next to the outside power-stage layer, and it is desirable to use thick copper for the external high-current power layers to minimize PCB conduction loss and thermal impedance.

POWER-STAGE LAYOUT

A switching-power-supply circuit can be divided into the power-stage circuit and the small-signal control circuit. The power-stage circuit includes the components that conduct high current; in general, you would place those components first and then place the small-signal control circuitry in specific spots in the layout.

The large current traces should be short and wide to minimize PCB inductance, resistance, and voltage drop. This setup is especially critical for the traces with high-di/dt pulsating-current flow.

Figure 2 identifies the continuous- and pulsating-current paths in a synchronous buck converter; the solid line represents the continuous-current paths, and the dashed line represents the pulsating (switching)-current paths. The pulsating-current paths include the traces connected to the input decoupling ceramic capacitor, C_{HF}; the top control FET, Q_T; and the bottom synchronous FET, Q_B, with its optional, paralleled Schottky diode.

Figure 3a shows the parasitic PCB inductors in the high-di/dt current paths. Because of the parasitic inductance, the pulsating-current paths not only radiate magnetic fields but also generate high-voltage ringing and

spikes across the PCB traces and MOSFETs. To minimize PCB inductance, lay out the pulsating-current loop (hot loop) so that it has a minimum circumference and comprises traces that are short and wide.

The high-frequency decoupling capacitor, C_{HF}, should be a 0.1- to 10-µF, X5R- or X7R-dielectric ceramic capacitor with very low ESL (effective series inductance) and ESR (equivalent series resistance). Higher-capacitance dielectrics (such as Y5V) can allow a large reduction in capacitance over voltage and temperature and thus are not preferred materials for C_{HF} use.

HIGHER-CAPACITANCE DIELECTRICS CAN ALLOW A LARGE REDUCTION IN CAPACITANCE OVER VOLTAGE AND TEMPERATURE AND THUS ARE NOT PREFERRED MATERIALS FOR C_{HF} USE.

Figure 3b provides a layout example for the critical pulsating-current loop in the buck converter. To limit resistive voltage drops and the number of vias, place power components on the same side of the board, with power traces routed on the same layer. When it is necessary to route a power trace to another layer, choose a trace in the continuous-current paths. When using vias to connect PCB layers in the high-current loop, deploy multiple vias to minimize via impedance.

Figure 4 shows the continuous- and pulsating-current loops in the boost converter. In this case, you should place the high-frequency ceramic capacitor, C_{HF}, on the output side close to the MOSFET, Q_B, and boost diode, D.

Figure 5 provides a layout example for the pulsating-current loop in the boost converter. It is critical to minimize the loop formed by the switch, Q_B, rectifier diode, D, and high-frequency output capacitor, C_{HF}.

To emphasize the importance of the decoupling capacitor, **figures 6** and **7** provide an example of a synchronous buck circuit. **Figure 6a** shows the layout of a dual-phase, $12V_{IN}$ to $2.5V_{OUT}$/30A max, synchronous buck supply using the LTC3729 two-phase, single-V_{OUT} controller IC. The waveforms for switching nodes SW1 and SW2 and output inductor current I_{LF1} are stable at no load (**Figure 6b**). If the load current exceeds 13A, however, the SW1 node waveform starts missing cycles. The problem becomes even worse with higher load current (**Figure 6c**).

Adding two 1-µF high-frequency ceramic capacitors—one on each channel's input side—solves the problem by separating and minimizing the hot-loop area of each channel. The switching waveform is stable even with maximum load current up to 30A.

HIGH-DV/DT SWITCHING AREA

In **figures 2** and **4**, the SW voltage swings with a high dv/dt rate between V_{IN} (or V_{OUT}) and ground. This node is rich in high-frequency noise components and is a strong source of EMI noise. To minimize the coupling capacitance between

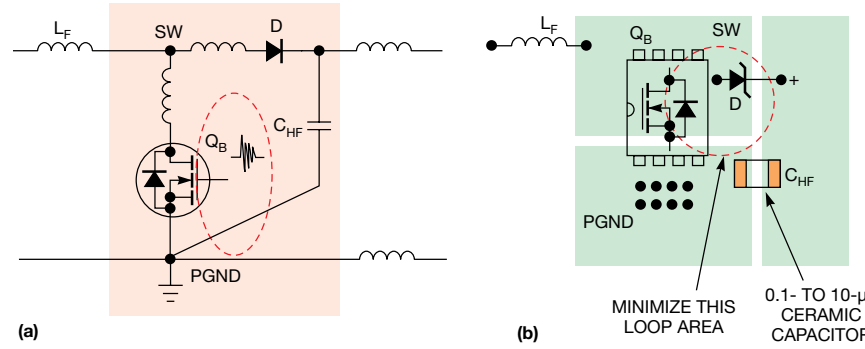
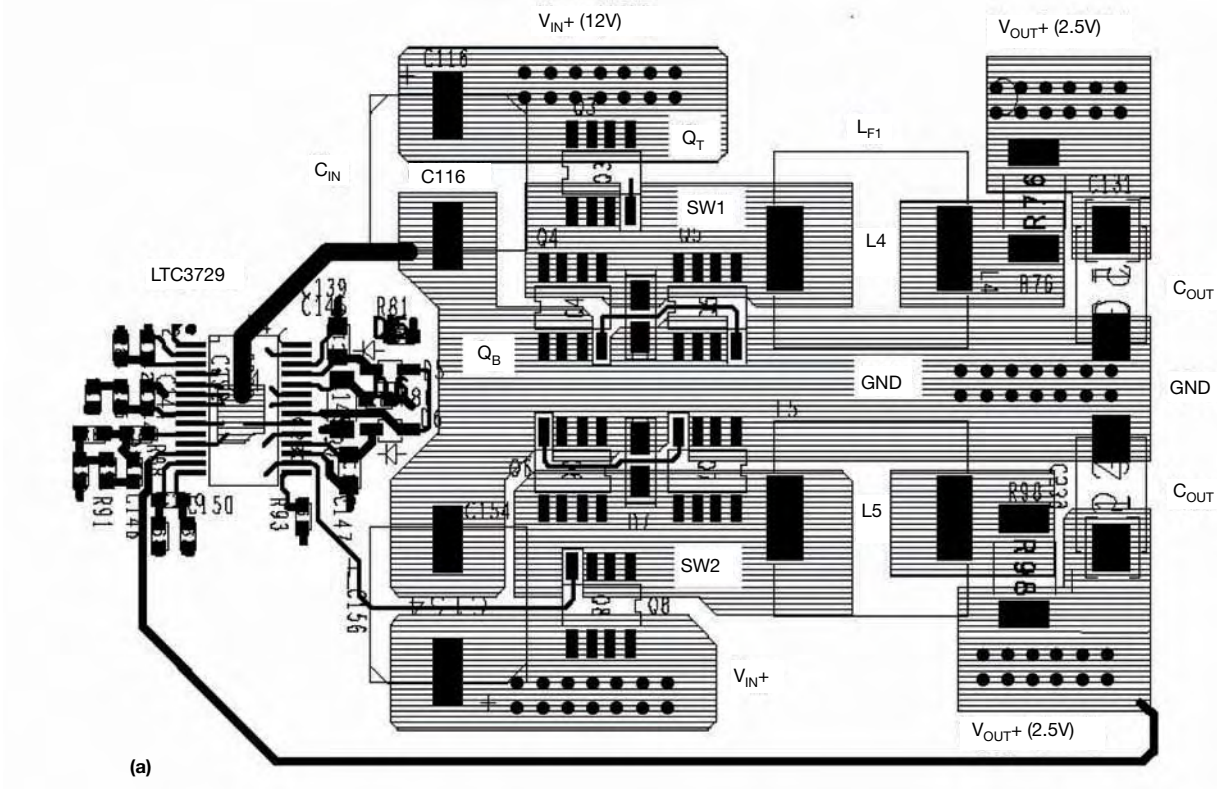
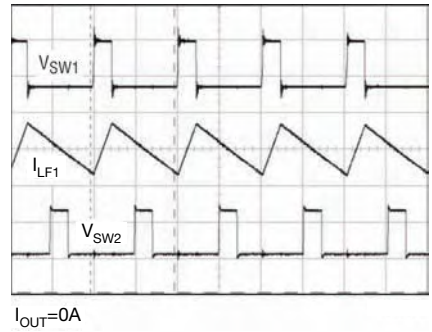


Figure 5 The hot-loop and parasitic PCB inductors in the boost converter are shown (a); the suggested layout (b) minimizes the hot-loop area.





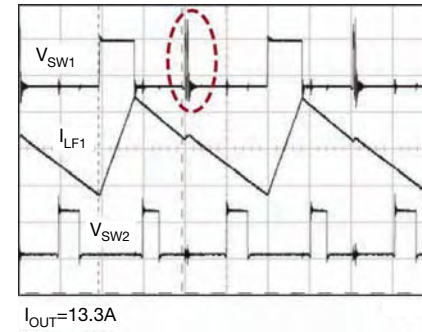


Figure 6 This two-phase, 2.5V/30A output buck converter (a) has a noise problem: Switching waveforms are stable at no load (b), but the SW1 waveform misses cycles when load current exceeds 13A (c).

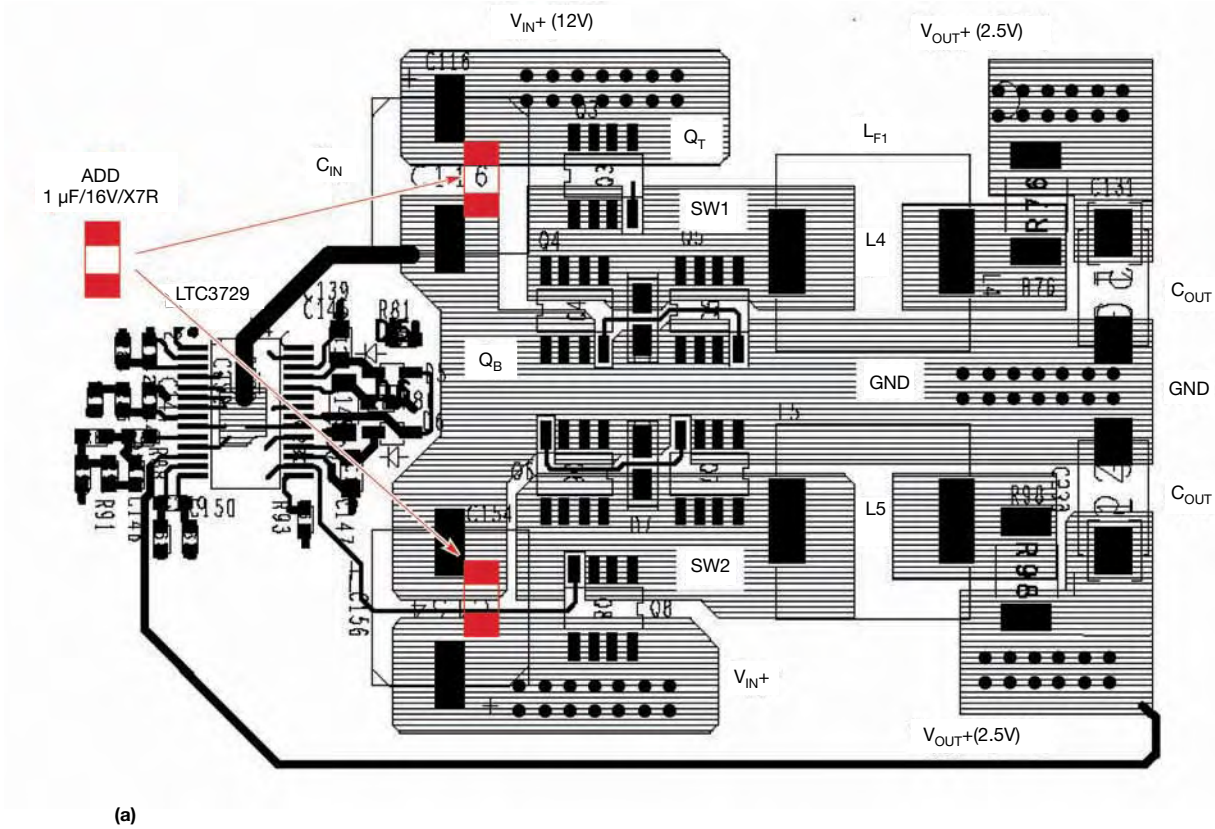


Figure 7 Adding two 1-µF, high-frequency input capacitors (a) solves the noise problem, as the switching waveforms at zero load (b) and 30A load (c) show.

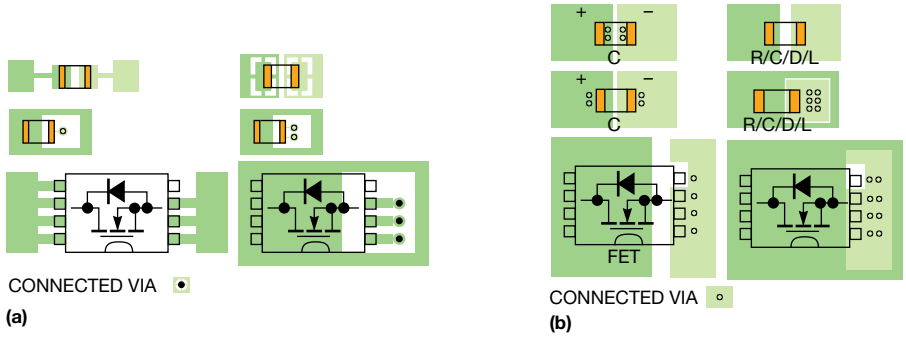
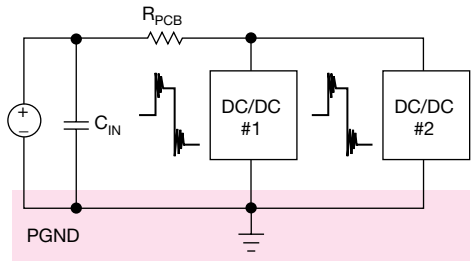
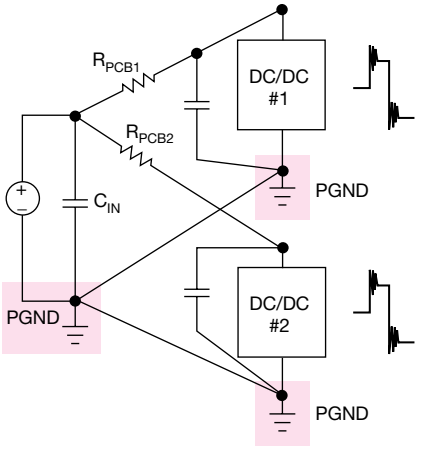


Figure 8 Unnecessary use of thermal-relief land patterns (a) increases the interconnection impedance of power components; in the recommended land pattern (b), the positive and negative vias are kept as close to each other as possible to minimize ESL.



(a)



(b)

Figure 9 When multiple onboard switching supplies share the same input-voltage rail (a), separate the input-current paths among the supplies for a more desirable setup (b).

the switching node and other noise-sensitive traces, you would minimize the SW copper; however, to conduct high inductor current and provide a heat sink to the power MOSFET, the SW-node PCB area cannot be made too small. It is usually preferable to place a ground copper area underneath the switching node to provide additional shielding.

In a design without external heat sinks for surface-mounted power MOSFETs and inductors, the copper area must be sufficient for heat sinking. For a dc voltage node, such as input/output voltage and power ground, it is desirable to make the copper area as large as possible.

Multiple vias are helpful in further reducing thermal stress. For high-dv/dt switching nodes, determining the proper size for the switching-node copper area involves a design trade-off between minimizing dv/dt-related noise and

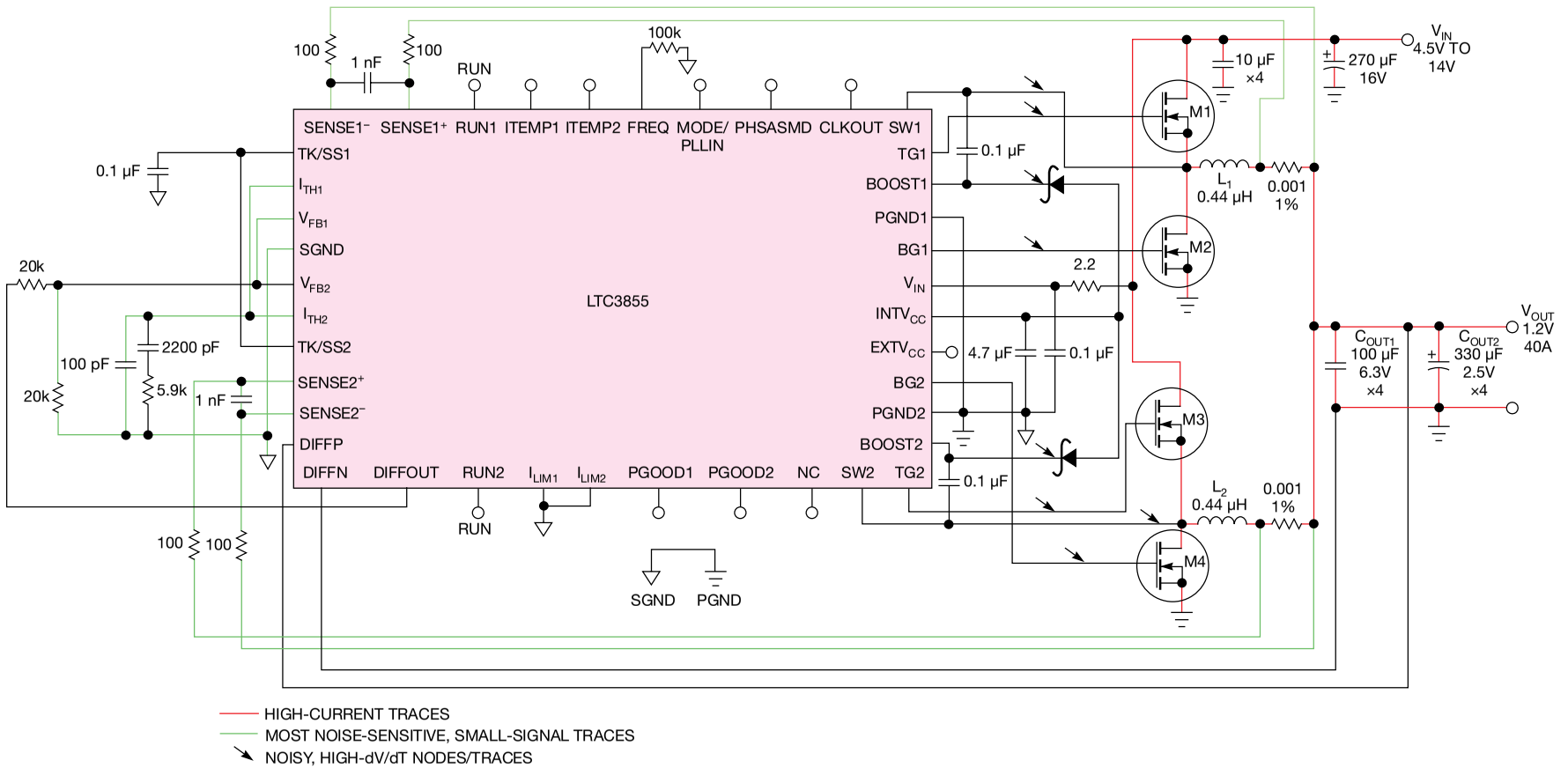


Figure 10 Using different colors in the schematic to indicate the different types of traces, as was done here for the LTC3855 buck converter, will help the PCB designer distinguish among them.

providing good heat-sinking capability for the MOSFETs.

POWER LAND PATTERNS

It is important to pay attention to the land (or pad) pattern of power components, such as low-ESR capacitors, MOSFETs, diodes, and inductors. **Figures 8a** and **8b** show examples of undesirable and desirable power-component land patterns, respectively.

For a decoupling capacitor, the positive and negative vias should be as close to each other as possible to minimize PCB ESL (**Figure 8b**). This is especially effective for capacitors with low ESL. Large-valued, low-ESR capacitors are usually more expensive; improper land patterning and poor routing can degrade their performance and thus increase overall cost. In general, the desired land patterns reduce PCB noise, reduce thermal impedance, and minimize trace impedance and voltage drops for the high-current components.

One common mistake in high-current power-component layout is the improper use of thermal-relief land patterns, as **Figure 8a** shows. Unnecessary use of thermal-relief land patterns increases the interconnection impedance of power components, resulting in higher power losses and decreasing the decoupling effect of low-ESR capacitors. If you use vias to conduct high current in your layout, be sure to use them in sufficient numbers to minimize via impedance. Further, do not use thermal relief for those vias.

Figure 9 shows an application with several onboard switching supplies sharing the same input-voltage rail. When

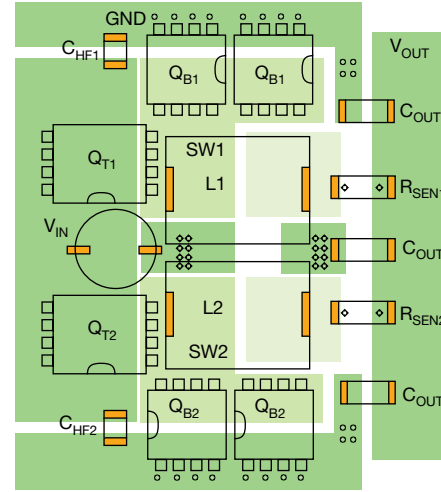


Figure 11 In this power-stage layout of a dual-phase, single-V_{OUT} buck converter, a solid power-ground-plane layer is placed just underneath the power-component layer.

those supplies are not synchronized to each other, it is necessary to separate the input current traces to avoid common-impedance noise coupling between different power supplies. It is less critical to have a local input-decoupling capacitor for each power supply.

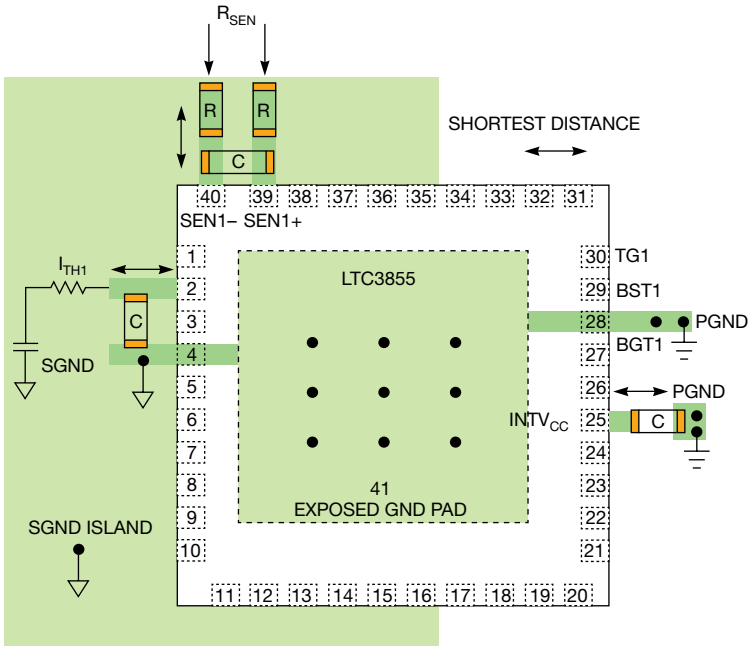


Figure 12 In the preferred ground-separation scheme for the LTC3855 supply, the IC has an exposed GND pad, which should be soldered down to the PCB to minimize electrical and thermal impedance. Several critical decoupling capacitors should be next to the IC pins.

components with ground planes or traces.

The control circuitry should have a separate signal (analog)-ground island from the power-stage ground. If there are separate SGND (signal ground) and PGND (power ground) pins on the controller IC, you should route them separately. For controller ICs that have integrated MOSFET drivers, the small-signal section of the IC pins should use the SGND (**Figure 12**).

Only one connection point is required between the signal and power grounds. It is desirable to return the signal ground to a clean point of the power-ground plane. Connecting both ground traces just under the controller IC can accomplish the two grounds. **Figure 12** shows the preferred ground separation of the LTC3855 supply. In this example, the IC has an exposed ground pad. It should be soldered down to the PCB to minimize electrical and thermal impedance. Multiple vias should be placed on the ground-pad area.

The decoupling capacitors for the controller IC should be physically close to their pins. To minimize connection impedance, it is preferable to connect the decoupling capacitors directly to the pins without using vias. As shown in **Figure 12**, the LTC3855 pins that should have their decoupling capacitors closely located are the current-sensing pins, $Sense^+/Sense^-$; compensation pin, I_{TH}; signal-ground pin, SGND; feedback-voltage divider pin, FB; IC V_{CC} voltage pin, $INTV_{CC}$; and power-ground pin, PGND.

For a PolyPhase single-output converter, having a symmetric layout for each phase helps to balance thermal stresses.

LAYOUT DESIGN EXAMPLE

Figure 10 provides a design example of a 4.5V to 14V_{IN} to 1.2V/40A max dual-phase synchronous buck converter using the LTC3855 PolyPhase current-mode step-down controller. Before starting your PCB layout, one good practice is to use different colors in the schematic to highlight the high-current traces; the noisy, high-dv/dt traces; and the sensitive, small-signal traces. Such delineation will help PCB designers distinguish among the traces.

Figure 11 shows a power-stage layout example for the power-component layer of this 1.2V/40A supply. In this figure, Q_T is the top-side control MOSFET and Q_B the bottom-side synchronous FET. An optional Q_B footprint is added for even more output current. A solid power-ground-plane layer is placed just underneath the power-component layer.

CONTROL-CIRCUITRY LAYOUT

Keep the control circuitry away from the noisy, switching copper areas. It is preferable to locate the control circuitry close to the V_{OUT}+ side for the buck converter and close to the V_{IN}+ side for the boost converter, where the power traces carry continuous current.

If space allows, locate the control IC a small distance (0.5 to 1 in.) from the power MOSFETs and inductors, which are noisy and hot. If space constraints force you to locate the controller close to power MOSFETs and inductors, take special care to isolate the control circuitry from the power

LOOP AREA AND CROSSTALK

Two or more adjacent conductors can be coupled capacitively. High dv/dt on one conductor will couple currents to another through the parasitic capacitor. To reduce the noise coupling from the power stage to the control circuitry, keep the noisy switching traces far from the sensitive small-signal traces. If possible, route the noisy traces and sensitive traces on different layers, using an internal ground layer for noise shielding.

IF SPACE ALLOWS, LOCATE THE CONTROL IC A SMALL DISTANCE (0.5 TO 1 IN.) FROM THE POWER MOSFETS AND INDUCTORS, WHICH ARE NOISY AND HOT.

The FET-driver TG, BG, SW, and BOOST pins on the LTC3855 controller have high-dv/dt switching voltages. The LTC3855 pins connected to the most sensitive small-signal nodes are $Sense^+/Sense^-$, FB, I_{TH}, and SGND. If the layout routes sensitive signal traces close to high-dv/dt nodes, you must insert ground traces or a ground layer between the signal traces and high-dv/dt traces to shield the noise.

Using short and wide traces to route gate-drive signals helps minimize impedance in gate-drive paths. In **Figure 13**,

you should route top FET-driver traces TG and SW together with a minimum loop area to minimize inductance and high-dv/dt noise. Similarly, route bottom FET-driver trace BG close to a PGND trace.

If you place a PGND layer under the BG trace, the ac-ground return current of the bottom FET will automatically be coupled in a path close to the BG trace. Alternating current will flow to where it finds the minimum loop/impedance. In this case, a separate PGND return trace for the bottom gate driver is not required. It is best to minimize the number of layers on which the gate-driver traces are routed; doing so prevents gate noise from propagating to other layers.

Of all the small-signal traces, current-sensing traces are the most sensitive to noise. The current-sensing signal amplitude is usually less than 100 mV, which is comparable to the noise amplitude. In the LTC3855 example, the Sense$^+$/Sense$^-$ traces should be routed in parallel with minimum spacing (Kelvin sense) to minimize the chance of picking up di/dt-related noise, as **Figure 14** shows.

In addition, the filter resistors and capacitor for current-sensing traces should be placed as close to the IC pins as possible. This setup provides the most effective filtering in the event that noise is injected into the long sense lines. If inductor DCR current sensing is used with an R/C network, the DCR sensing resistor, R, should be close to the inductor, while the DCR sensing capacitor, C, should be close to the IC.

If you use a via in the return path of the trace to Sense$^-$, the via should not contact another internal V_{OUT}+ layer. Otherwise, the via may conduct large V_{OUT}+ current, and the resulting voltage drop may distort the current-sensing signal. Avoid routing the current-sensing traces near the noisy switching nodes (TG, BG, SW, and BOOST traces). If possible, place the ground layer between the current-sensing traces and the layer with power-stage traces.

If the controller IC has differential-voltage remote-sensing pins, use separated traces for the positive and negative remote-sensing traces, with Kelvin sense connection as well.

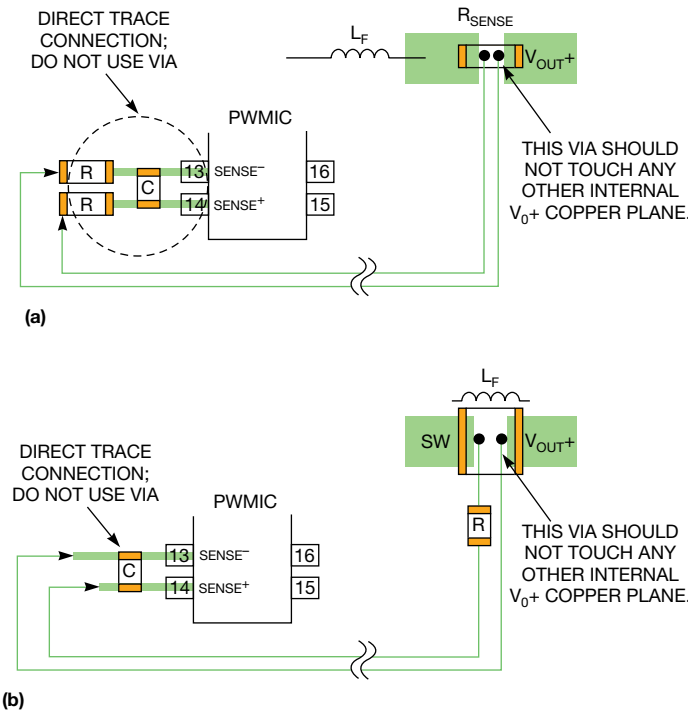


Figure 14 Kelvin sensing is shown for current sensing, R_{SENSE} (a) and inductor DCR sensing (b).

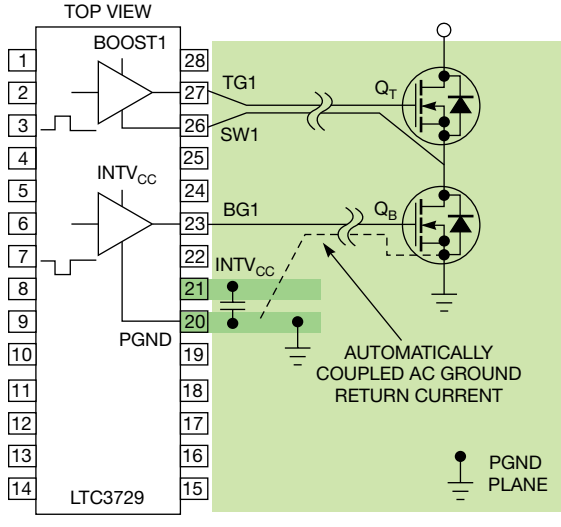


Figure 13 When routing MOSFET gate-driver traces, using short and wide traces helps minimize impedance in gate-drive paths. The gate-driver current paths should have minimum loop areas.

TRACE-WIDTH SELECTION

Current level and noise sensitivity are unique to specific controller pins; therefore, you must select specific trace widths for different signals. In general, the small-signal nets can be narrow and routed with 10- to 15-mil-wide traces. The high-current nets (gate driving, V_{CC}, and PGND) should be routed with short and wide traces. At least a 20-mil width is recommended for these nets.

LAYOUT CHECKLIST

Table 1, available online at http://bit.ly/Ruxanc, provides a sample checklist of the dual-phase LTC3855 supply shown in **Figure 10**. Using such a checklist will help ensure a well-laid-out power-supply design. EDN

AUTHOR'S BIOGRAPHY

Henry Zhang is an applications engineering manager for power products at Linear Technology Corp. He received his bachelor of science degree in electrical engineering from Zhejiang University in China in 1994 and his master's and doctoral degrees in electrical engineering from Virginia Polytechnic Institute and State University (Blacksburg, VA) in 1998 and 2001, respectively.