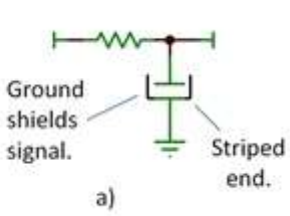
Bruce Trump *Dec 11, 2012*

I posed a question a couple of weeks ago regarding film capacitors—what's the meaning of the stripe on one end? Check the picture below.

These are non-polarized capacitors so it's not a polarity marking. A reader, Richard, answered correctly—it identifies the outside conductive foil of the spiral wrapped innards. I'm finding that few engineers these days know this, and proper orientation can make a difference. Even if you never use one of these caps, it may cause you to design your PCB layouts differently. Let's think about it.

The outside foil of a spiral-wrapped film capacitor shields the inner conductor. In a simple low-pass R-C circuit, figure 1a, one side of the capacitor is grounded so it makes good sense to connect the striped end to ground to shield the signal side from electrostatically coupled interference.



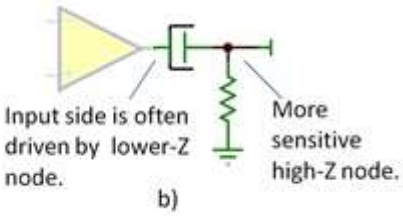


Figure 1.

What about the high-pass case, figure 1b? Neither side of the capacitor is grounded. But generally, the previous stage driving this circuit (perhaps the output of an op amp) is a low impedance that would be less susceptible to induced noise. So connect the stripe to the low-Z side.

- Now, what to do with the integrator circuit, figure 2a? The output side of the integrator capacitor is driven by the low impedance of the op amp and is not easily perturbed by external interference. The inverting input is clearly the more sensitive node. The stripe should go on the output side of the op amp.

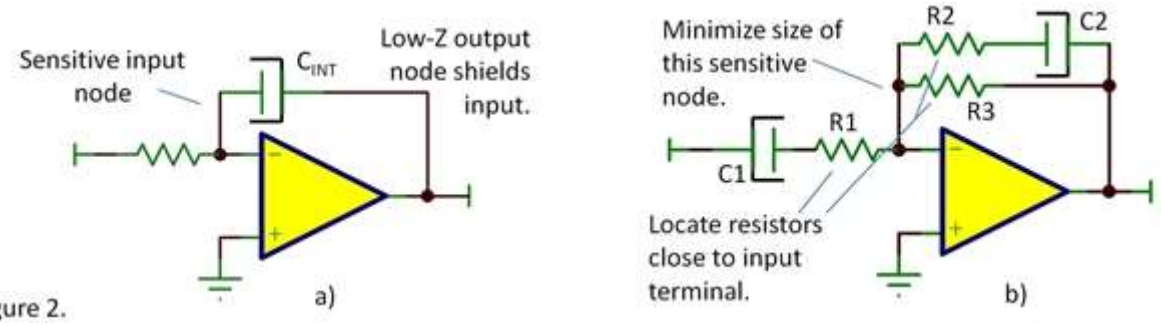


Figure 2.

There's more to consider in figure 2b. The order in which C1 and R1 are connected could make a difference. Same with R2 and C2. In theory, the order is irrelevant and SPICE simulations would show identical results. But R1 and R2 are physically smaller and can be located close to the inverting input terminal. This reduces the "antenna" area and capacitance on this sensitive node (which can affect stability). The physically larger film capacitor, C2, is located on the output side of the op amp with the stripe connected to the low impedance output terminal.

I mostly think about sensitive analog circuitry that could be *susceptible* to interference but you may have noisy circuitry that might be a *source* of potential interference. Again, careful placement and orientation may yield improvement. And this is not just about striped capacitors. There may be other large components in your system that can be a source of noise pickup or radiation. With awakened awareness you may find other opportunities for tweaks and improvements to your PCB layouts.

Striped capacitors are but a quirky reminder that there's a lot to know about good circuit board layout—grounding, signal routing, component selection and placement. Many of our data sheets have very specific information that can help optimize performance. And here are a few links to general ideas for improved layouts:

- Reducing PCB design costs: From schematic capture to PCB layout
- PCB Layout Tips for High Resolution—Section 9
- High Speed Amplifier Layout Tip—general tips also applicable to precision analog circuits
- PCB Design Guidelines for Reduced EMI—Reduction of EMI in microcontroller circuitry

Thank for reading, and comments are welcome!

Bruce email: thesignal@list.ti.com (Email for direct communications. Comments for all, below.)

Table of Contents for all *The Signal* blogs

Jens-Michael Gross *over 12 years ago*

An interesting article about PCB design.

But where it comes to the striped capacitor, I think the critical thing is not the marking of the outside (surface) foil that is responsible for the proposed shielding effect. After all, the outside foild becomes an inside foil after one loop. And the whole thing is a capacitor, intended to let AC signals pass.

The important thing is that the wires are usually connected one at the outer and one at the inner end of the wrapped foil. So between the two ends of one foil layer is the resistance of the foils full length. IMHO the main difference of the two pins of a striped capacitor is that the pin connected to the outer end of one foil has a much smaller ESR between pin and capacitor surface than the pin that is connected to the inner end of the other foil. Independent of whether it is the 'outer' or 'inner' side it is connected to.

If both pins were conneted to the outer end of their foils, I don't think it would make a difference at all which one is outer or inner side. But that is mechanically much more difficult to handle during production.

Well, It was just an analytical thought and I may be wrong :)

Bruce Trump *over 12 years ago*

Jens-Michael— Not all capacitors are used as a low-impedance AC coupling device intended to pass all AC. Their varying impedance with frequency is intended and useful in the circuit, as in a filter. The AC impedance on the two sides of a capacitor can be very different. If you were to touch each side of a capacitor in the type of circuits I described you would see a pronounced difference in the induced noise.

You may be correct that one lead has a greater contribution to ESR but I don’t see that it matters. Unlike the situation described in figure 2b, it is the case of a theoretical series circuit—the order of the components (ESR-Cap or Cap-ESR) does not matter.

Jens-Michael Gross *over 12 years ago*

Well, yes, of course not to let 'all' AC pass, depending on capacitance and frequency. But capacitance and frequency are relative. A Dirac pulse (e.g. an isolated beta particle ionic charge) will go through any capacitor unattenuated.

What I meant was that only the first outer winding will act as 'shield', but the next windings will transport the 'shielded' signal into the capacitor.

So the difference is IMHO not whether the inner or outer foil layer is used as shield, but rather whether the pin that is intended to channel off the shielded signal is connected to the outermost winding (with no ESR between pin and "shield") or the innermost winding (with maximum ESR between pin and shield). And mostly independent of whether it is the inner or outer foil layer of the film.

Of course, if there were only one winding, then inner or outer would be the only thing of importance. But since the outer foil is also the 2nd and 4th inner foil and any signal that hits one foil is also passed ot the inside as well with not much attenuation (because that's what a capacitor does: passing changes while saturating on states), I still think that the important factor is which pin is closer to the outermsot winding, and not whether it is the outer or inner foil. Even though usually the one pin is connected to the outermost winding of the outer foil while the other goes to the innermost winding of the inner foil. so it comes to the same result in practice.

Bruce Trump *over 12 years ago*

Jens-Michael-- I’ll try once more. If properly connected, the outside foil does not pick up electrostatic interference because it is connected to a low impedance, imperturbable circuit node. Thus there is no (or much less) noise on the outside conductor that could be transferred to the other side of the capacitor.

Low ESR to the outside conductor won't help unless the node to which it is connected is a lower impedance than the other side.

This link www.aikenamps.com/OutsideFoil.htm also describes the issue correctly if you would like to sample another information source.

It's interesting that the audio community working with vintage tube (valve) gear is attuned to this issue. The high electrostatic fields present in this equipment in conjunction with very high Z at grid inputs made these designs particularly vulnerable to unwanted coupling.

Dieter Teuchert *over 12 years ago*

Thanks for your reminder. I just tested a cap as described in the link, using a scope. The cap i used (ERO 1813-6 3u3 / 250V) showed a clear difference of the two orientations, but as a surprise appeared to be reverse, i mean the outer foil was NOT on the end marked with the stripe. I have eight of those and measured the other ones, too. Some are the wrong way, the others are as expected. With these capacitors it would require some extra work to use the proposed optimization for an industrial board. If needed i can provide a photo of the cap and a screen dump of a typical measurement.

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