SECTION 7-2

# PCB Design Issues

*James Bryant*

Printed circuit boards (PCBs) are by far the most common method of assembling modern electronic circuits. Comprised of a sandwich of insulating layer (or layers) and one or more copper conductor patterns, they can introduce various forms of errors into a circuit, particularly if the circuit is operating at either high precision or high speed. PCBs then, act as "unseen" components, wherever they are used in precision circuit designs. Since designers don't always consider the PCB electrical characteristics as additional components of their circuit, overall performance can easily end up worse than predicted. This general topic, manifested in many forms, is the focus of this section.

PCB effects that are harmful to precision circuit performance include leakage resistances, spurious voltage drops in trace foils, vias, and ground planes, the influence of stray capacitance, dielectric absorption (DA), and the related "hook." In addition, the tendency of PCBs to absorb atmospheric moisture, *hygroscopicity,* means that changes in humidity often cause the contributions of some parasitic effects to vary from day to day.

In general, PCB effects can be divided into two broad categories—those that most noticeably affect the static or dc operation of the circuit, and those that most noticeably affect dynamic or ac circuit operation.

Another very broad area of PCB design is the topic of grounding. Grounding is a problem area in itself for all analog designs, and it can be said that implementing a PCB based circuit doesn't change that fact. Fortunately, certain principles of quality grounding, namely the use of ground planes, are intrinsic to the PCB environment. This factor is one of the more significant advantages to PCB-based analog designs, and appreciable discussion of this section is focused on this issue.

Some other aspects of grounding that must be managed include the control of spurious ground and signal return voltages that can degrade performance. These voltages can be due to external signal coupling, common currents, or simply excessive IR drops in ground conductors. Proper conductor routing and sizing, as well as differential signal handling and ground isolation techniques enables control of such parasitic voltages.

One final area of grounding to be discussed is grounding appropriate for a mixed-signal, analog/digital environment. Although this isn't the specific overall focus of the book, it is certainly true that interfacing with ADCs (or DACs) is a major task category of op amps, and thus it shouldn't be overlooked. Indeed, the single issue of quality grounding can drive the entire layout philosophy of a high performance mixed signal PCB design—as it well should.

## Resistance of Conductors

Every engineer is familiar with resistors—little cylinders with wire or tab ends—although perhaps fewer are aware of their idiosyncrasies, as generally covered in section 7-1. But far too few engineers consider that all the wires and PCB traces with which their systems and circuits are assembled are also resistors. In higher precision systems, even these trace resistances and simple wire interconnections can have degrading effects. Copper is *not* a superconductor—and too many engineers appear to think it is.

SECTION 7-3

# *Op Amp Power Supply Systems*

*Walt Jung, Walt Kester*

Op amp circuits have traditionally been powered from well-regulated, low noise linear power supplies. This type of power system is typically characterized by medium-to-low power conversion efficiency. Such linear regulators usually excel in terms of self-generated and radiated noise components. If the designer's life were truly simple, it might continue with such familiar designs offering good performance and minimal side effects.

But, the designer's life is hardly so simple. Modern systems may allow using linear regulators, but multiple output levels and/or polarities are often required. There may also be some additional requirements set for efficiency, which may dictate the use of dc-dc conversion techniques, and, unfortunately, their higher associated noise output.

This section addresses power supply design issues for op amp systems, taking into account the regulator types most likely to be used. The primary dc power sources are assumed to be either rectified and smoothed ac sources (i.e., mains derived), a battery stack, or a switching regulator output. The latter example could be fed from either a battery or a mains-derived dc source.

As noted in Figure 7-46, linear mode regulation is generally recommended as an optimum starting point in all instances (first bullet). Nevertheless, in some cases, a degree of hybridization between fully linear and switching mode regulation may be required (second bullet). This could be either for efficiency or other diverse reasons.

- High performance analog power systems use linear regulators, with primary power derived from:
  - AC line power
  - Battery power systems
  - DC- DC power conversion systems
- Switching regulators should be avoided if at all possible, but if not…
  - Apply noise control techniques
  - Use quality layout and grounding
  - Be aware of EMI

**Figure 7-46: Regulation priorities for op amp power supply systems**

Whenever switching-type regulators are involved in powering precision analog circuits, noise control is very likely to be a design issue. Therefore some focus of this section is on minimizing noise when using switching regulators.

## Linear IC Regulation

Linear IC voltage regulators have long been standard power system building blocks. After an initial introduction in 5 V logic voltage regulator form, they have since expanded into other standard voltage levels spanning from 3 V to 24 V, handling output currents from as low as 100 mA (or less) to as high as 5 A (or more). For several good reasons, linear style IC voltage regulators have been valuable system components since the early days. As mentioned above, a basic reason is the relatively low noise characteristic vis-à-vis the switching type of regulator. Others are a low parts count and overall simplicity compared to discrete solutions. But, because of their power losses, these linear regulators have also been known for being relatively inefficient. Early generation devices (of which many are still available) required 2 V or more of unregulated input above the regulated output voltage, making them lossy in power terms.

More recently however, linear IC regulators have been developed with more liberal (i.e., lower) limits on minimum input-output voltage. This voltage, known more commonly as *dropout* voltage, has led to what is termed the *Low DropOut* regulator, or more simply, the LDO. Dropout voltage ($V_{MIN}$) is defined simply as that minimum input-output differential where the regulator undergoes a 2% reduction in output voltage. For example, if a nominal 5.0 V LDO output drops to 4.9 V (–2%) under conditions of an input-output differential of 0.5 V, by this definition the LDO's dropout voltage is 0.5 V.

Dropout voltage is extremely critical to a linear regulator's power efficiency. The lower the voltage allowable across a regulator while still maintaining a regulated output, the less power the regulator dissipates as a result. A low regulator dropout voltage is the key to this, as it takes a lower dropout to maintain regulation as the input voltage lowers. In performance terms, the bottom line for LDOs is simply that more useful power is delivered to the load and less heat is generated in the regulator. LDOs are key elements of power systems providing stable voltages from batteries, such as portable computers, cellular phones, and so forth. This is because they maintain a regulated output down to lower points on the battery's discharge curve. Or, within classic mains-powered raw dc supplies, LDOs allow lower transformer secondary voltages, reducing system shutdowns under brownout conditions, as well as allowing cooler operation.

## Some Linear Voltage Regulator Basics

A brief review of three terminal linear IC regulator fundamentals is necessary before understanding the LDO variety. Most (but not all) of the general three-terminal regulator types available today are *positive leg, series style* regulators. This simply means that they control the regulated voltage output by means of a pass element in series with the positive unregulated input. And, although they are fewer in number, there are also *negative leg* series style regulators, which operate in a fashion complementary to the positive units.

A basic hookup diagram of a three terminal regulator is shown in Figure 7-47. In terms of basic functionality, many standard voltage regulators operate in a series mode, three-terminal form, just as shown here. As can be noted from this figure, the three I/O terminals are $V_{IN}$, GND (or Common), and $V_{OUT}$. Note also that this regulator block, in the absence of any assigned voltage polarity, could in principle be a positive type regulator. Or, it might also be a negative style of voltage regulator—the principle is the same for both—a common terminal, as well as input and output terminals.

In operation, two power components become dissipated in the regulator, one a function of $V_{IN} - V_{OUT}$ and $I_L$, plus a second, which is a function of $V_{IN}$ and $I_{GROUND}$. The first of these is usually dominant. Analysis of the situation will reveal that as the dropout voltage $V_{MIN}$ is reduced, the regulator is able to deliver a higher percentage of the input power to the load, and is thus more efficient, running cooler and saving power. This is the core appeal of the modern LDO type of regulator (see Reference 1).

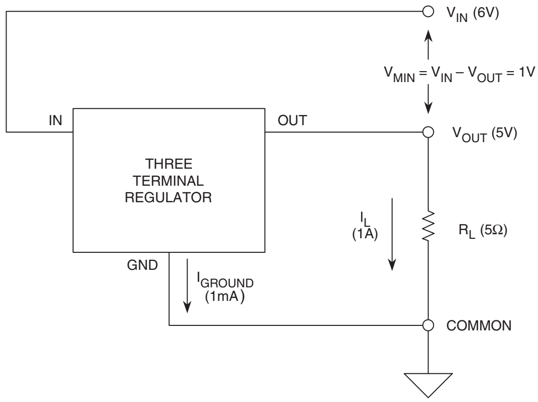


**Figure 7-47: A basic three-terminal regulator hookup (either positive or negative)**

A more detailed look within a typical regulator block diagram reveals a variety of elements, as is shown in Figure 7-48. Note that all regulators will contain those functional components connected via solid lines. The connections shown dotted indicate options, which might be available when more than three I/O pins are available.

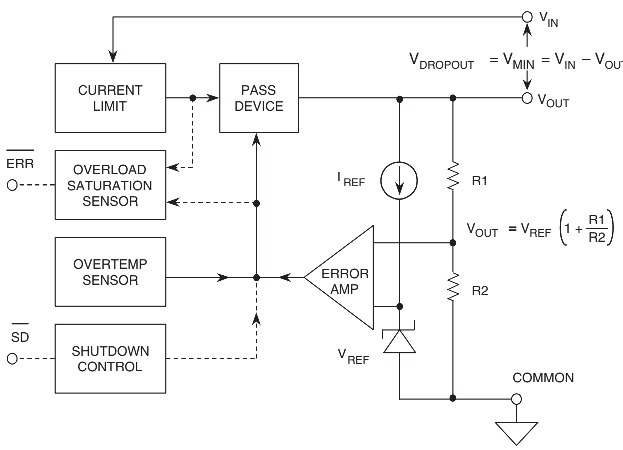


**Figure 7-48: Functional diagram of a typical voltage regulator**

In operation, a voltage reference block produces a stable voltage $V_{REF}$, which is almost always a voltage based on the bandgap voltage of silicon, typically ~1.2 V (see Reference 2). This allows output voltages of 3 V or more from supplies as low as 5 V. This voltage drives one input of an error amplifier, with the second input connected to the divider, R1-R2. The error amplifier drives the pass device, which in turn controls the output. The resulting regulated voltage is then simply:

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right) \qquad \text{Eq. 7-1}$$

## Pass Devices

The pass device is a foremost regulator part, and the type chosen here has a major influence on almost all regulator performance issues. Most notable among these is dropout voltage, $V_{MIN}$. Analysis shows that the use of an *inverting* mode pass transistor allows the pass device to be effectively saturated, thus minimizing the associated voltage losses. Therefore, this factor makes the two most desirable pass devices for LDO use a PNP bipolar, or a PMOS transistor. These device types achieve the lowest levels of $V_{IN}$–$V_{OUT}$ required for LDO operation. In contrast, NPN bipolars are poor as pass devices in terms of low dropout, particularly when they are Darlington connected.

Standard fixed-voltage IC regulator architectures illustrate this point regarding pass devices. For example, the fixed-voltage LM309 5 V regulators and family derivatives such as the 7805, 7815, et al, (and their various low and medium current alternates) are poor in terms of dropout voltage. These designs use a Darlington pass connection, not known for low dropout (~1.5 V typical), or for low quiescent current (~5 mA).

## ±15 V Regulator Using Adjustable Voltage ICs

Later developments in references and three-terminal regulation techniques led to the development of the *voltage-adjustable* regulator. The original IC to employ this concept was the LM317, a positive regulator. The device produces a fixed reference voltage of 1.25 V, appearing between the $V_{OUT}$ and ADJ pins of the IC. External scaling resistors set up the desired output voltage, adjustable in the range of 1.25 V–30 V. A complementary device, the LM337, operates in similar fashion, regulating negative voltages.

An application example using standard *adjustable* three terminal regulators to implement a ±15 V linear power supply is shown in Figure 7-49. This is a circuit that might be used for powering traditional op amp supply rails. It is capable of better line regulation performance than would an otherwise similar circuit, using standard fixed-voltage regulator devices, such as for example 7815 and 7915 ICs. However, in terms of power efficiency it isn't outstanding, due to the use of the chosen ICs, which require 2 V or more of headroom for operation.

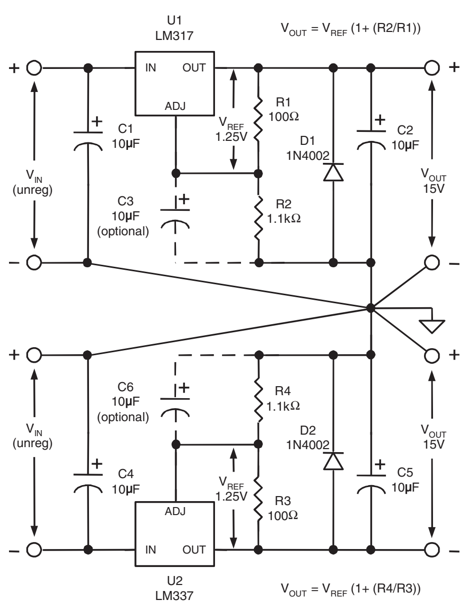


**Figure 7-49: A classic ±15 V, 1 A linear supply regulator using adjustable voltage regulator ICs**

In the upper portion of this circuit an LM317 adjustable regulator is used, with R2 and R1 chosen to provide a 15 V output at the upper output terminal. If desired, R2 can easily be adjusted for other output levels, according to the figure's $V_{OUT}$ expression. Resistor R1 should be left fixed, as it sets the minimum regulator drain of 10 mA or more.

In this circuit, capacitors C1 and C2 should be tantalum types, and R1-R2 metal films. C3 is optional, but is highly recommended if the lowest level of output noise is desired. The normally reverse biased diode D1 provides a protective output clamp, for system cases where the output voltage would tend to reverse, if one supply should fail. The circuit operates from a rectified and filtered ac supply at $V_{IN}$, polarized as shown. The output current is determined by choosing the regulator IC for appropriate current capability.

To implement the negative supply portion, the sister device to the LM317 is used, the LM337. The bottom circuit section thus mirrors the operation of the upper, delivering a negative 15 V at the lowest output terminal. Programming of the LM337 for output voltage is similar to that of the LM317, but uses resistors R4 and R3. R4 should be used to adjust the voltage, with R3 remaining fixed. C6 is again optional, but is recommended for reasons of lowest noise.

## Low Dropout Regulator Architectures

In contrast to traditional three terminal regulators with Darlington or single-NPN pass devices, low dropout regulators employ lower voltage threshold pass devices. This basic operational difference allows them to operate effectively down to a range of 100 mV–200 mV in terms of their specified $V_{MIN}$. In terms of use within a system, this factor can have fairly significant operational advantages.

An effective implementation of some key LDO features is contained in the Analog Devices series of anyCAP LDO regulators. Devices of this ADP330x series are so named for their relative insensitivity to the output capacitor, in terms of both its size and ESR. Available in power efficient packages such as the ADI Thermal Coastline (and other thermally-enhanced packages), they come in both stand-alone LDO and LDO controller forms (used with an external PMOS FET). They also offer a wide span of fixed output voltages from 1.8 V to 5 V, with rated current outputs up to 500 mA. User-adjustable output voltage versions are also available. A basic simplified diagram for the family is shown schematically in Figure 7-50.

One of the key differences in the ADP330x LDO series is the use of a high gain vertical PNP pass device, Q1, allowing typical dropout voltages for the series to be on the order of 1 mV/mA for currents of 200 mA or less.

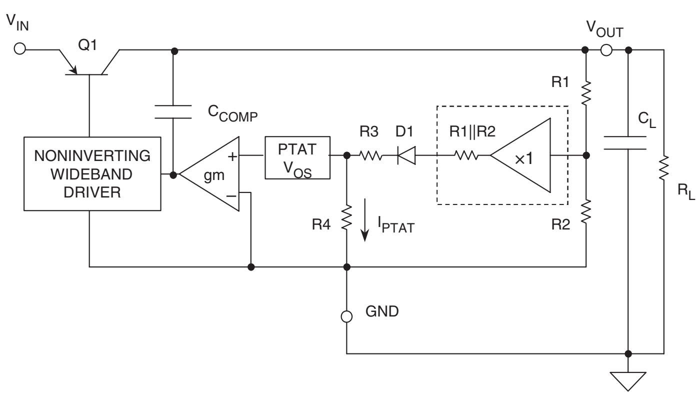


**Figure 7-50: The ADP330x anyCAP LDO architecture has both dc and ac performance advantages**

In circuit operation, $V_{REF}$ is defined as a reference voltage existing at the output of a zero impedance divider of ratio R1/R2. In Figure 7-50, this is depicted symbolically by the (dotted) unity gain buffer amplifier fed by R1/R2, which has an output of $V_{REF}$. This reference voltage feeds into a series connection of (dotted) R1||R2, then actual components D1, R3, R4, and so forth. The regulator output voltage is:

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right) \qquad \text{Eq. 7-2}$$

In the various devices of the ADP330X series, the R1-R2 divider is adjusted to produce standard output voltages of 1.8 V, 2.5 V, 2.7 V, 3.0 V, 3.2 V, 3.3 V, and 5.0 V. The regulator behaves as if the entire error amplifier has simply an offset voltage of $V_{REF}$ volts, as seen at the output of a conventional R1-R2 divider.

While the above described dc performance enhancements of the ADP330x series are worthwhile, more dramatic improvements come in areas of ac-related performance. Capacitive loading, and the potential instability it brings, is a major deterrent to easy LDO applications. One method of providing some measure of immunity to variation in an amplifier response pole is the use of a frequency compensation technique called *pole splitting*. In the Figure 7-50 circuit, $C_{COMP}$ functions as the pole splitting capacitor, and provides benefits of a buffered, $C_L$ independent single-pole response. As a result, frequency response is dominated by the regulator's internal compensation, and becomes relatively immune to the value and ESR of load capacitor $C_L$.

This feature makes the design tolerant of virtually any output capacitor type. $C_L$, the load capacitor, can be as low as 0.47 μF, and it can also be a multilayer ceramic capacitor (MLCC) type, allowing a very small physical size for the entire regulation function.

## Fixed Voltage, 50/100/200/500 mA LDO Regulators

A basic regulator application diagram common to various fixed voltage devices of the ADP330x device series is shown by Figure 7-51. Operation of the various pins and internal functions is discussed next. To adapt this general diagram to a specific current and voltage requirement, select a basic device for output current from the table in the diagram. Then select the output voltage by the part number suffix, consistent with the table.

OUTPUT TABLE

| DEVICE | $I_{OUT}$(mA) | $V_{OUT}$(V) |
|---|---|---|
| ADP3300 | 50 | 2.7, 3, 3.2, 3.3, 5 |
| ADP3301 | 100 | 2.7, 3, 3.2, 3.3, 5 |
| ADP3303 | 200 | 2.7, 3, 3.2, 3.3, 5 |
| ADP3335 | 500 | 1.8, 2.5, 2.85, 3.3, 5 |

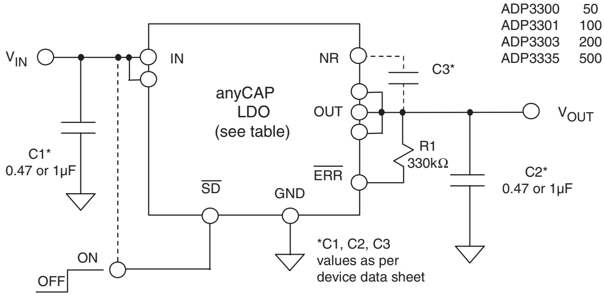


**Figure 7-51: A basic LDO regulator hookup useful by device selection from 50 mA to 500 mA, at fixed voltages per table**

This circuit is a general one, illustrating common points. For example, the ADP3300 is a 50 mA basic LDO regulator device, designed for those fixed output voltages as noted. An actual ADP3300 device ordered would be ADP3300ART-YY, where the "YY" is a voltage designator suffix such as 2.7, 3, 3.2, 3.3, or 5, for the respective table voltages. The "ART" portion of the part number designates the package (SOT23 6-lead). To produce 5 V from the circuit, use the ADP3300ART-5. Similar comments apply to the other devices, insofar as part numbering. For example, an ADP3301AR-5 depicts an SO-8 packaged 100 mA device, producing 5 V output.

In operation, the circuit produces rated output voltage for loads under the max current limit, for input voltages above $V_{OUT} + V_{MIN}$ (where $V_{MIN}$ is the dropout voltage for the specific device used, at rated current). The circuit is ON when the shutdown input is in a HIGH state, either by a logic HIGH control input to the $\overline{SD}$ pin, or by simply tying this pin to $V_{IN}$ (shown dotted). When $\overline{SD}$ is LOW or grounded, the regulator shuts down, and draws a minimum quiescent current.

The anyCAP regulator devices maintain regulation over a wide range of load, input voltage and temperature conditions. Most devices have a combined error band of ±1.4% (or less). When an overload condition is detected, the open collector $\overline{ERR}$ goes to a LOW state. R1 is a pullup resistor for the $\overline{ERR}$ output. This resistor can be eliminated if the load provides a pullup current.

C3, connected between the OUT and NR pins, can be used for an optional noise reduction (NR) feature. This is accomplished by bypassing a portion of the internal resistive divider, which reduces output noise ~10 dB. When exercised, only the recommended low leakage capacitors as specific to a particular part should be used.

The C1 input and C2 output capacitors should be selected as either 0.47 µF or 1 µF values respectively, again, as per the particular device used. For most devices of the series 0.47 µF suffices, but the ADP3335 uses the 1 µF values. Larger capacitors can also be used, and will provide better transient performance.

Heat sinking of device packages with more than five pins is enhanced, by use of multiple IN and OUT pins. All of the pins available should therefore be used in the PCB design, to minimize layout thermal resistance.

## Adjustable Voltage, 200 mA LDO Regulator

In addition to the fixed output voltage LDO devices discussed above, adjustable versions are also available, to realize nonstandard voltages. The ADP3331 is one such device, and shown in Figure 7-52, configured as a 2.8 V output, 200 mA LDO application.

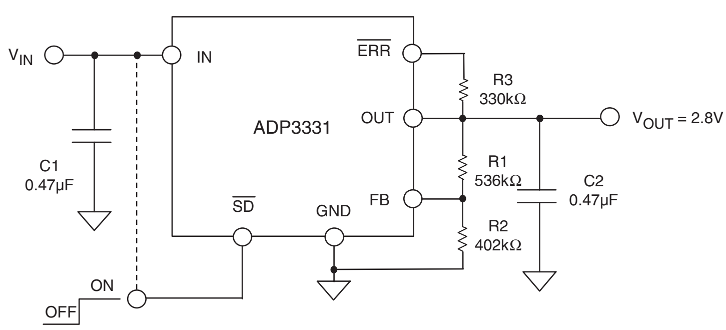


**Figure 7-52: An adjustable 200 mA LDO regulator set up for a 2.8 V output**

The ADP3331 is generally similar to other anyCAP LDO parts, with two notable exceptions. It has a lower quiescent current (~34 µA when lightly loaded) and most importantly, the output voltage is user-adjustable. As noted in the circuit, R1 and R2 are external precision resistors used to define the regulator operating voltage.

The output of this regulator is $V_{OUT}$, which is related to feedback pin FB voltage $V_{FB}$ as:

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right) \qquad \text{Eq. 7-3}$$

where $V_{FB}$ is 1.204 V. Resistors R1 and R2 program $V_{OUT}$, and their parallel equivalent should be kept close to 230 kΩ for best stability.

To select R1 and R2, first calculate their ideal values, according to the following two expressions:

$$R1 = 230\left(\frac{V_{OUT}}{V_{FB}}\right)k\Omega \qquad \text{Eq. 7-4}$$

$$R2 = \frac{230}{\left(1+\frac{V_{FB}}{V_{OUT}}\right)}k\Omega \qquad \text{Eq. 7-5}$$

In the example circuit, $V_{OUT}$ is 2.8 V, which yields R1 = 534.9 kΩ, and R2 = 403.5 kΩ. As noted in the figure, closest standard 1% values are used, which provides an output of 2.8093 V (perfect resistors assumed). In practice, the resistor tolerances should be added to the ±1.4% tolerance of the ADP3331 for an estimation of overall error.

To complement the above-discussed anyCAP series of standalone LDO regulators, there is the LDO *regulator controller*. The regulator controller IC picks up where the standalone regulator stops for either load current or power dissipation, using an external PMOS FET pass device. As such, the current capability of the LDO can be extended to several amps. An LDO regulator controller application is shown later in this discussion. The application examples above illustrate a subset of the entire anyCAP family of LDOs. Further information on this series of standalone and regulator controller LDO devices can be found in the references at the end of the section.

## Charge-Pump Voltage Converters

Another method for developing supply voltage for op amp systems employs what is known as a *charge-pump* circuit (also called switched capacitor voltage conversion). Charge-pump voltage converters accomplish energy transfer and voltage conversion using charges stored on capacitors, thus the name, charge-pump.

Using switching techniques, charge pumps convert supply voltage of one polarity to a higher or lower voltage, or to an alternate polarity (at either higher or lower voltage). This is accomplished with only an array of low resistance switches, a clock for timing, and a few external storage capacitors to hold the charges being transferred in the voltage conversion process. No inductive components are used, thus EMI generation is kept to a minimum. Although relatively high currents are switched internally, the high current switching is localized, and therefore the generated noise is not as great as in inductive type switchers. With due consideration towards component selection, charge-pump converters can be implemented with reasonable noise performance.

The two common charge-pump voltage converters are the *voltage inverter* and the *voltage doubler* circuits. In a voltage inverter, a charge pump capacitor is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle the input voltage stored on the charge pump capacitor is inverted and applied to an output capacitor and the load. Thus the output voltage is essentially the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle—defined as the ratio of charge pump charging time to the entire switching cycle time—is usually 50%, which yields optimal transfer efficiency.

A voltage doubler works similarly to the inverter. In this case the pump capacitor accomplishes a voltage doubling function. In the first phase it is charged from the input, but in the second phase of the cycle it appears in series with the output capacitor. Over time, this has the effect of doubling the magnitude of the input voltage across the output capacitor and load. Both the inverter and voltage doubler circuits provide no voltage regulation in basic form. However, techniques exist to add regulation (discussed below).

There are advantages and disadvantages to using charge-pump techniques, compared to inductor-based switching regulators. An obvious key advantage is the elimination of the inductor and the related magnetic design issues. In addition, charge-pump converters typically have relatively low noise and minimal radiated EMI. Application circuits are simple, and usually only two or three external capacitors are required. Because there are no inductors, the final PCB height can generally be made smaller than a comparable inductance-based switching regulator. Charge-pump inverters are also low in cost, compact, and capable of efficiencies greater than 90%. Obviously, current output is limited by the capacitor size and the switch capacity. Typical IC charge-pump inverters have 150 mA maximum outputs.

On their downside, charge-pump converters don't maintain high efficiency for a wide voltage range of input to output, unlike inductive switching regulators. Nevertheless, they are still often suitable for lower current loads where any efficiency disadvantages are a small portion of a larger system power budget. A summary of general charge-pump operating characteristics is shown in Figure 7-53.

An example of charge-pump applicability is the voltage inverter function. Inverters are often useful where a relatively low current negative voltage (i.e., –3 V) is required, in addition to a primary positive voltage (such as 5 V). This may occur in a single supply system, where only a few high performance parts require the negative voltage. Similarly, voltage doublers are useful in low current applications, where a voltage greater than a primary supply voltage is required.

- No Inductors
- Minimal Radiated EMI
- Simple Implementation: Two External Capacitors (Plus an Input Capacitor)
- Efficiency > 90% Achievable
- Low Cost, Compact, Low Profile (Height)
- Optimized for Doubling or Inverting Supply Voltage:
  – ADM660 or ADM8660
- Voltage Regulated Output Devices Available:
  – ADP3603/ADP3604/ADP3605/ADP3607

**Figure 7-53: Some general charge-pump characteristics**

## Unregulated Inverter and Doubler Charge Pumps

Illustrating these principles are a pair of basic charge-pump ICs from Analog Devices, shown in Figure 7-54. The ADM660 is a popular charge-pump IC, and is shown here operating as both a voltage inverter (left) and the doubler (right). Switching frequency of this IC is selectable between 25 kHz and 120 kHz using the FC input pin. With the FC input is open as shown, the switching frequency is 25 kHz; with it connected to the V+ pin, frequency increases to 120 kHz. Generally, efficiency is greater when operating at the higher frequency. Only two external electrolytic capacitors are required for operation, C1 and C2 (ESR should be <200 mΩ). The value of these capacitors is flexible. For a 25 kHz switching frequency 10 µF tantalum types are recommended; for 120 kHz operation 2.2 µF provides comparable performance. Larger values can also be used, and will provide lower output ripple (at the expense of greater size and cost).

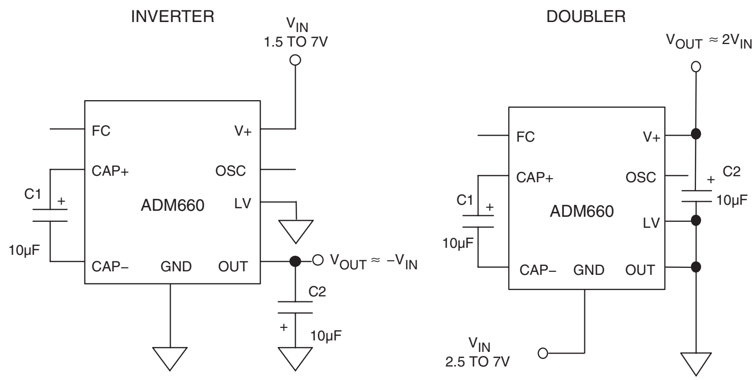


**Figure 7-54: ADM660 IC functions as a supply inverter (left) or doubler (right)**

These circuits accept $V_{IN}$ inputs over the ranges noted, and deliver a nominal voltage output tracking the input voltage in magnitude, as noted in the output expressions. Although the output voltage is not regulated in these basic designs, it is still relatively low in impedance, due to the nominal 9 Ω resistance of the IC switches.

Efficiency of these circuits using the ADM660/ADM8660 can be 90% or more, for output currents up to 50 mA at a 120 kHz frequency. The ADM8660 is a device similar to the ADM660, however it is optimized for inverter operation, and includes a shutdown feature which reduces the quiescent current to 5 µA.

## Regulated Output Charge-Pump Voltage Converters

Adding regulation to a simple charge-pump voltage converter function greatly enhances its usefulness for most applications. There are several techniques for adding regulation to a charge-pump converter. The most straightforward is to follow the charge-pump inverter/doubler with an LDO regulator. The LDO provides the regulated output, and can also reduce the charge-pump converter's ripple. This approach, however, adds complexity and reduces the available output voltage by the dropout voltage of the LDO (~200 mV). These factors may or may not be a disadvantage.

By far the simplest and most effective method for achieving regulation in a charge-pump voltage converter is simply to use a charge-pump design with an internal error amplifier, to control the on-resistance of one of the switches.

This method is used in the ADP3603/ADP3604/ADP3605 voltage inverters, devices offering regulated outputs for positive input voltage ranges. The output is sensed and fed back into the device via a sensing pin, $V_{SENSE}$. Key features of the series are good output regulation, 3% in the ADP3605, and a high switching frequency of 250 kHz, good for both high efficiency and small component size.

An example circuit for the ADP3605 IC from this series is shown in Figure 7-55. The application is a 5 V to –3 V inverter, with the output regulated ±3% for currents up to 60 mA. In normal operation, the SHUTDOWN pin is connected to ground (as shown dotted). Alternately, a logic HIGH at this pin shuts the device down to a standby current of 2 µA.

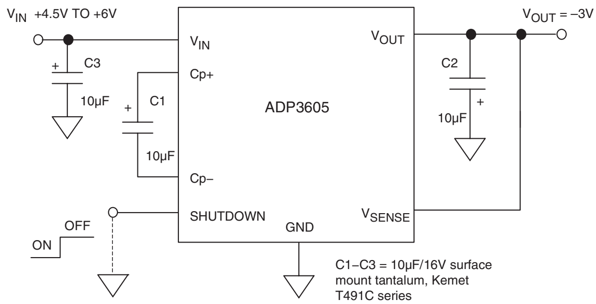


**Figure 7-55: ADP3605 5 V to –3 V, 60 mA regulated supply inverter**

The 10 µF capacitors for C1–C3 should have ESRs of less than 150 mΩ (4.7 µF can be used at the expense of slightly higher output ripple voltage). C1 is the most critical of the three, because of its higher current flow. The tantalum type listed is recommended for lowest output ripple.

With values as shown, typical output ripple voltage ranges up to approximately 60 mV as the output current varies over the 60 mA range. Although output is regulated for currents up to 60 mA, higher currents of up to 100 mA are also possible with further voltage deviation, and proportionally greater ripple.

These application examples illustrate a subset of the entire charge-pump IC family. Further information on these devices can be found in the end-of-section references.

## *Linear Post Regulator for Switching Supplies*

Another powerful noise reduction option that can be utilized in conjunction with a switching type supply is the option of a *linear post regulator* stage. This is at best an LDO type of regulator, chosen for the desired clean analog voltage level and current. It is preceded by a switching stage, which might be a buck or boost type inductor-based design, or it may also be a charge-pump. The switching converter allows the overall design to be more power-efficient, and the linear post regulator provides clean regulation at the load, reducing the noise of the switcher. This type of regulator can also be termed *hybrid regulation*, since it combines both switching and linear regulation concepts.

An example circuit is shown in Figure 7-56, which features a 3.3 V/1 A low noise, analog-compatible regulator. It operates from a nominal 9 V supply, using a buck or step-down type of switching regulator, as the first stage at the left. The switcher output is set for a few hundred mV above the desired final voltage output, minimizing power in the LDO stage at the right. This feature can eliminate need for a heat sink on the LDO pass device.

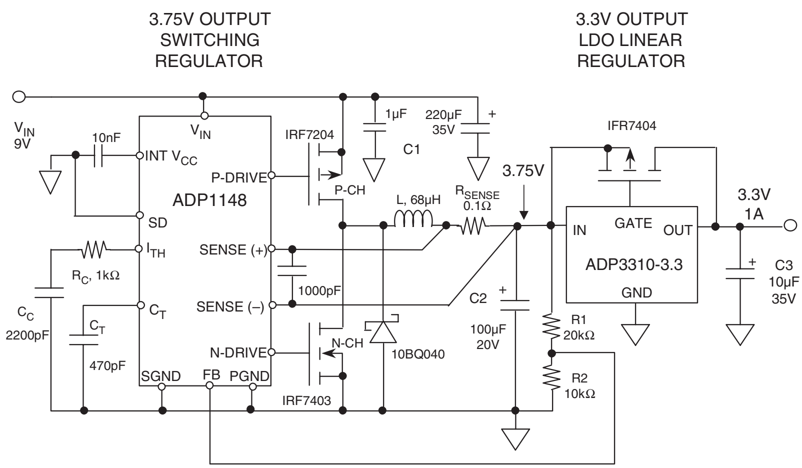


**Figure 7-56: A linear post-regulator operating after a switching/ linear regulator is capable of low noise, as well as good dc efficiency**

In this example the ADP1148 IC switcher is set up for a 3.75 V output by R1-R2 but, in principle, this voltage can be anything suitable to match the headroom of the companion LDO (within specification limits, of course). In addition, the principle extends to any LDO devices and other current levels, and other switching regulators. The ADP3310-3.3 is a fixed-voltage LDO controller, driving a PMOS FET pass device, with a 3.3 V output.

The linear post regulation stage provides both noise-reduction (in this case about 14 dB), as well as good dc regulation. To realize best results, good grounding practices must be followed. In tests, noise at the 3.3 V output was about 5mV p-p at the 150 kHz switcher frequency. Note that the LDO noise rejection for such relatively high frequencies is much less than at 100 Hz/120 Hz. Note also that C2's ESR will indirectly control the final noise output. The ripple figures given are for a general-purpose C2 part, and can be improved.

## Power Supply Noise Reduction and Filtering

During the last decade or so, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20 kHz to 1 MHz, the spikes can contain frequency components extending to 100 MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, with the output loading of your system.

This section discusses filter techniques for rendering a switching regulator output *analog ready*, that is sufficiently quiet to power precision op amp and other analog circuitry with relatively small loss of dc terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes charge-pump as well as other switching type converters and supplies. This section focuses on reducing *conducted type* switching power supply noise with external post filters, as opposed to radiated type noise.

Tools useful for combating high frequency switcher noise are shown by Figure 7-57. These differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small in size.

- Capacitors
- Inductors
- Ferrites
- Resistors
- Linear Post Regulation
- Proper Layout and Grounding
- Physical Separation

**Figure 7-57: Tools useful in reducing power supply noise**

## Capacitors

*Capacitors* are probably the single most important filter component for reducing switching-related noise. As noted in the first section of this chapter, there are many different types of capacitors. It is also quite true that understanding of their individual characteristics is absolutely mandatory to the design of effective and practical power supply filters. There are generally three classes of capacitors useful in 10 kHz–100 MHz filters, broadly distinguished as the generic dielectric types; *electrolytic*, *film*, and *ceramic*. These discussions complement earlier ones, focusing on power-related concepts. With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10 kHz in some electrolytics to as high as 100 MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general-purpose aluminum electrolytic* types, available in working voltages from below 10 V up to about 500 V, and in size from one to several thousand µF (with proportional case sizes). All electrolytic capacitors are polarized, and cannot withstand more than a volt or so of reverse bias without damage.

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100 V or less, with capacitance of 500 µF or less (see Reference 7). In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses (see Reference 8). This capacitor type can compete with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte (see Reference 9). The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of minimal low temperature ESR degradation.

*Film* capacitors are available in very broad value ranges and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10 µF/50 V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes do help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50 V). Where film types excel is in their low dielectric losses, a factor that may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10 mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

As typically constructed using wound layers, film capacitors can be inductive, which limits their effectiveness for high frequency filtering. Obviously, only noninductively made film caps are useful for switching regulator filters. One specific style which is noninductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads (see References 8 and 10). Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL (see Reference 11). Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to above 10 MHz. At the highest frequencies, only stacked film types should be considered. Leadless surface-mount packages are now available for film types, minimizing inductance.

*Ceramic* is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several µF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200 V (see ceramic families of Reference 7).

Multilayer ceramic "chip caps" are very popular for bypassing and/or filtering at 10 MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1 GHz. For high frequency applications, a useful selection can be ensured by selecting a value that has a self-resonant frequency *above* the highest frequency of interest.

The capacitor model and waveforms of Figure 7-58 illustrate how the various parasitic model elements become dominant, dependent upon the operating frequency. Assume an input current pulse changing from 0 to 1 A in 100 ns, as noted in the figure, and consider what voltage will be developed across the capacitor.

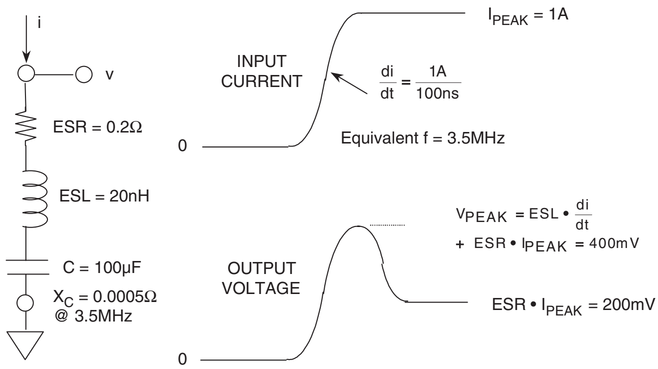


**Figure 7-58: Capacitor equivalent circuit and response to input current pulse**

The fast-rising edge of the current waveform shown results in an initial voltage peak across the capacitor, which is proportional to the ESL. After the initial transient, the voltage settles down to a longer duration level which is proportional to the ESR of the capacitor. Thus the ESL determines how effective a filter the capacitor is for the fastest components of the current signal, and the ESR is important for longer time frame components. Note that an overall time frame of a few microseconds (or even less) is relevant here. As things turn out, this means switching frequencies in the 100 kHz to 1 MHz range. Unfortunately, however, this happens to be the region where most electrolytic types begin to perform poorly.

All electrolytics will display impedance curves similar in general shape to that of Figure 7-59. In a practical capacitor, at frequencies below about 10 kHz the net impedance seen at the terminals is almost purely capacitive (C region). At intermediate frequencies, the net impedance is determined by ESR, for example

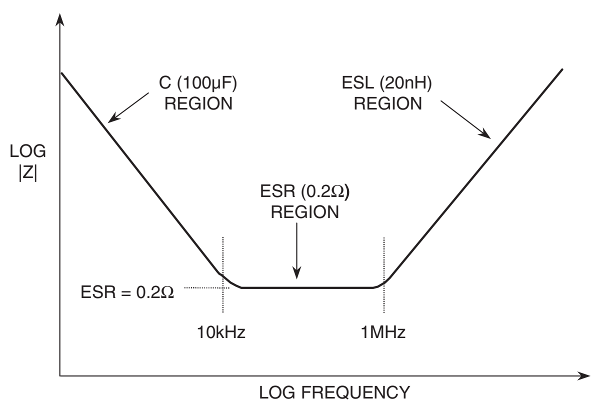


**Figure 7-59: Electrolytic capacitor impedance versus frequency**

about 0.1 Ω to 0.5 Ω at ~125 kHz, for several types (ESR region). Above about several hundred kHz to 1 MHz these capacitor types become inductive, with net impedance rising (ESL region).

The minimum impedance within the 10 kHz – 1 MHz range will vary with the magnitude of the capacitor's ESR. This is the primary reason why ESR is the most critical item in determining a given capacitor's effectiveness as a switching supply filter element. Higher up in frequency, the inductive region will vary with ESL (which in turn is also strongly affected by package style). It should go without saying that a wideband impedance plot for a capacitor being considered for a filter application will go a long way towards predicting its potential value, as well as for comparing one type against another.

It should be understood that all real-world capacitors have some finite ESR. While it is usually desirable for filter capacitors to possess low ESR, this isn't always so. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying "free" damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted in an impedance versus frequency plot. This occurs where $|Z|$ falls to a minimum level, nominally equal to the capacitor's ESR at that frequency. This low Q resonance can generally be noted to cover a relatively wide frequency range of several octaves. Contrasted to the high Q sharp resonances of film and ceramic caps, electrolytic's low Q behavior can be useful in controlling resonant peaks.

## Ferrites

A second important filter element is the inductor, available in various forms. The use of *ferrite* core materials is prevalent in inductors most practical for power supply filtering. Regarding inductors, ferrites, which are nonconductive ceramics manufactured from the oxides of nickel, zinc, manganese, and so forth., are extremely useful in power supply filters (see Reference 12). Ferrites can act as either inductors or resistors, dependent upon their construction and the frequency range. At low frequencies (<100 kHz), inductive ferrites are useful in low-pass LC filters. At higher frequencies, ferrites become resistive, which can be an important characteristic in high-frequency filters. Again, exact behavior is a function of the specifics. Ferrite impedance depends on material, operating frequency range, dc bias current, number of turns, size, shape, and temperature. Figure 7-60 summarizes a number of ferrite characteristics.

- Ferrites Good for Frequencies Above 25kHz
- Many Sizes / Shapes Available Including Leaded "Resistor Style"
- Ferrite Impedance at High Frequencies Primarily Resistive — Ideal for HF Filtering
- Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low
- High Saturation Current Versions Available
- Choice Depends Upon:
  - Source and Frequency of Interference
  - Impedance Required at Interference Frequency
  - Environmental: Temperature, AC and DC Field Strength, Size and Space Available
- Always Test the Design

**Figure 7-60: A summary of ferrite characteristics**

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 13 and 14). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, premounted on a length of wire and used as a component (see Reference 14). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface-mount beads are also available. PSpice models of Fair-Rite ferrites are available, allowing ferrite impedance estimations (see Reference 15). The models match measured rather than theoretical impedances.

Selecting the proper ferrite is not straightforward. A ferrite's impedance is dependent upon a number of interdependent variables, and is difficult to quantify analytically. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the dc current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with actual filter experimentation connected under system load conditions, should lead to a proper ferrite selection.

## Card Entry Filter

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switching supply output to produce an *analog ready* supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies.

A basic stage can be used to carry the entire load current, and filter noise by 60 dB or more up to a 1 MHz–10 MHz range. Figure 7-61 illustrates this type of filter, which is used as a *card entry filter,* providing broadband filtering for all power entering a PC card.

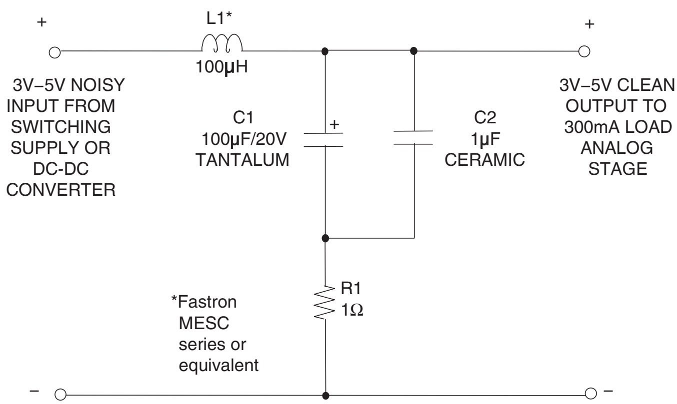


**Figure 7-61: A card-entry filter is useful for low-medium frequency power line noise filtering in analog systems**

In this filter, L1 and C1 perform the primary filtering, which provides a corner frequency of about 1.6 kHz. With the corner thus placed well below typical switching frequencies, the circuit can have good attenuation up to 1 MHZ, where the typical attenuation is on the order of 60 dB. At higher frequencies parasitics limit performance, and a second filter stage will be more useful.

The ultimate level of performance available from this filter will be related to the components used within it. L1 should be derated for the operating current, thus for 300 mA loads it is a 1 A type. The specified L1 choke has a typical DCR of 0.65 Ω, for low drop across the filter (see Reference 16). C1 can be either a tantalum or an aluminum electrolytic, with moderately low ESR. For current levels lower than 300 mA, L1 can be proportionally downsized, saving space. The resistor R1 provides damping for the LC filter, to prevent possible ringing. R1 can be reduced or even possibly eliminated, if the ESR of C1 provides a comparable impedance.

While the example shown is a single-supply configuration, obviously the same filter concepts apply for dual supplies.

### Rail Bypass/Distribution Filter

A complement to the card-entry filter is the rail-bypass filter scheme of Figure 7-62. When operating from relatively clean power supplies, the heavy noise filtering of the card entry filter may not be necessary. However, some sort of low frequency bypassing with appreciable energy storage is almost always good, and this is especially true if high currents are being delivered by the stages under power.

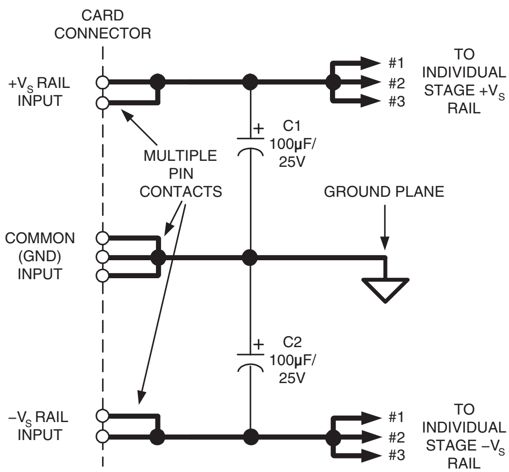


**Figure 7-62: Dual-supply low frequency rail bypass/distribution filter**

In such cases, some lumped low frequency bypassing is appropriate on the card. Although these energy storage filters need not be immediately adjacent to the ICs they serve, they should be within a few inches. This type of bypassing scheme should be considered a minimum for powering any analog circuit. The exact capacitor values aren't critical, and can vary appreciably. The most important thing is to avoid leaving them out.

The circuit shown uses C1 and C2 as these bypasses in a dual-rail system. Note that multiple card contacts are recommended for the I/O pins, especially ground connection. From the capacitors outward, supply rail traces are distributed to each stage as shown, in "star" distribution fashion. Note: while this is the optimum method to minimize inter-stage crosstalk, in practice some degree of "daisy chaining" is often difficult to avoid. A prudent designer should therefore carefully consider common supply currents effects in designing these PCB distribution paths.

Wider than normal traces are recommended for these supply rails, especially those carrying appreciable current. If the current levels are in the ampere region, then star-type supply distribution with ultrawide traces should be considered mandatory. In extreme cases, a dedicated power plane can be used. The impedance of the ground return path is minimized by the use of a ground plane.

## Local High Frequency Bypass/Decoupling

At each individual analog stage, further local, high-frequency-only filtering is used. With this technique, used in conjunction with either the card-entry filter or the low frequency bypassing network, such smaller and simpler local filter stages provide optimum high frequency decoupling. *These stages are provided directly at the power pins, of* all *individual analog stages*.

Figure 7-63 shows this technique, in both correct (left) as well as incorrect example implementations (right). In the left example, a typical 0.1 μF chip ceramic capacitor goes directly to the opposite PCB side ground plane, by virtue of the via, and on to the IC's GND pin by a second via. In contrast, the less desirable setup at the right adds additional PCB trace inductance in the ground path of the decoupling cap, reducing effectiveness.

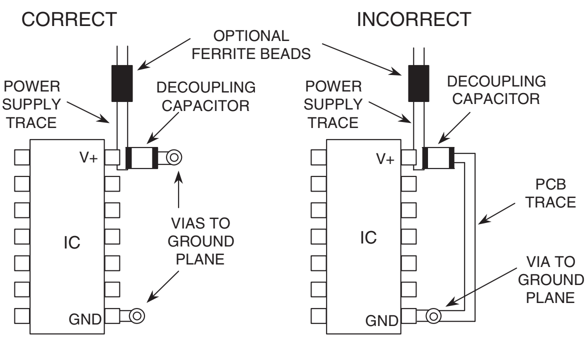


**Figure 7-63: Localized high frequency supply filter(s) provides optimum filtering and decoupling via short low-inductance path (ground plane)**

The general technique is shown here as suitable for a single-rail power supply, but the concept obviously extends to dual rail systems. Note: if the decoupled IC in question is an op amp, the GND pin shown is the $-V_S$ pin. For dual supply op amp uses, there is no op amp GND pin per se, so the dual decoupling networks should go directly to the ground plane when used, or other local ground.

*All* high frequency (i.e., ≥10 MHz) ICs should use a bypassing scheme similar to Figure 7-63 for best performance. Trying to operate op amps and other high performance ICs without local bypassing is almost always folly. It *may* be possible in a few circumstances, *if* the circuitry is strictly micropower in nature, and the gain-bandwidth in the kHz range. To put things into an overall perspective however, note that a pair of 0.1 μF ceramic bypass caps cost less than 25 cents. Hardly a worthy saving compared to the potential grief and lost time of troubleshooting a system without bypassing.

In contrast, the ferrite beads aren't 100% necessary, but they will add extra HF noise isolation and decoupling, which is often desirable. Possible caveats here would be to verify that the beads never saturate, when the op amps are handling high currents.

Note that with some ferrites, even before full saturation occurs, some beads can be nonlinear, so if a power stage is required to operate with a low distortion output, this should also be lab checked.

Figure 7-64 summarizes the previous points of this section regarding power supply conditioning techniques for op amp circuitry.

- Use Proper Layout and Grounding Techniques
- At HF Local Decoupling at IC Power Pins is Mandatory
- At HF Ground Planes are Mandatory
- External LC Filters Very Effective in Reducing Ripple
- Low ESR/ESL Capacitors Give Best Results
- Parallel Caps Lower ESR/ESL and Increase C
- Linear Post Regulation Effective for Noise Reduction and Best Regulation
- Completely Analytical Approach Difficult
  - Prototyping Required for Optimum Results

Once Design is Final, Don't Switch Vendors or Substitute Parts
  - Without First Verifying Performance within the Circuit

**Figure 7-64: A summary of power supply conditioning techniques for high performance op amp circuitry**

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