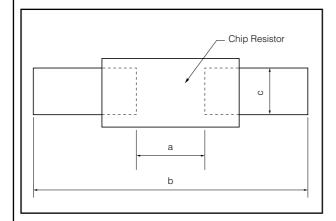
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■ Recommended Land Pattern

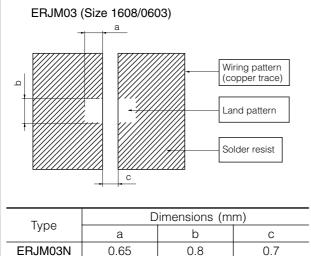
• Anexample of a land pattern for the Rectangular Type is shown below.

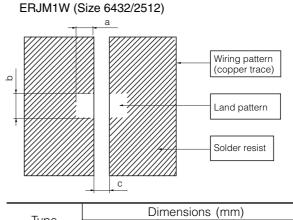


Size	Dimensions (mm)			
mm/inch	а	b	С	
0402/01005	0.15 to 0.20	0.5 to 0.7	0.20 to 0.25	
0603/0201	0.3 to 0.4	0.8 to 0.9	0.25 to 0.35	
1005/0402	0.5 to 0.6	1.4 to 1.6	0.4 to 0.6	
1005*/0402 (ERJ2BW)	0.52	1.4 to 1.6	0.4 to 0.6	
1608/0603	0.7 to 0.9	2.0 to 2.2	0.8 to 1.0	
1608*/0603 (ERJ3BW)	0.45	2.5 to 2.7	0.9 to 1.1	
2012/0805	1.0 to 1.4	3.2 to 3.8	0.9 to 1.4	
2012*/0805 (ERJ6BW)	0.9	3.2 to 3.8	1.1 to 1.4	
3216/1206	2.0 to 2.4	4.4 to 5.0	1.2 to 1.8	
3216*/1206 (ERJ8BW)	1.2	4.4 to 5.0	1.3 to 1.8	
3225/1210	2.0 to 2.4	4.4 to 5.0	1.8 to 2.8	
4532/1812	3.3 to 3.7	5.7 to 6.5	2.3 to 3.5	
5025/2010	3.6 to 4.0	6.2 to 7.0	1.8 to 2.8	
6432/2512	5.0 to 5.4	7.6 to 8.6	2.3 to 3.5	
6432/2512 (ERJL1W)	3.6 to 4.0	7.6 to 8.6	2.3 to 3.5	

^{*} High power (double-sided resistive elements structure) type

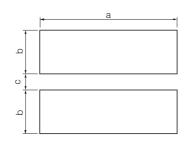
• Anexample of a land pattern for Low Resistance Value Chip Resistors is shown below.





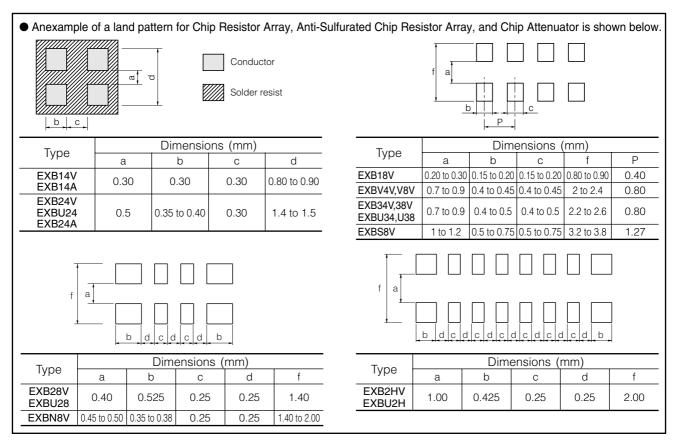
Туре	Dimensions (mm)			
	а	b	С	
	ERJM1WS	2.1	3.4	4.2
	ERJM1WT	3.1	3.4	2.2
-				

• Anexample of a land pattern for High Power Chip Resistors / Wide Terminal Type is shown below.

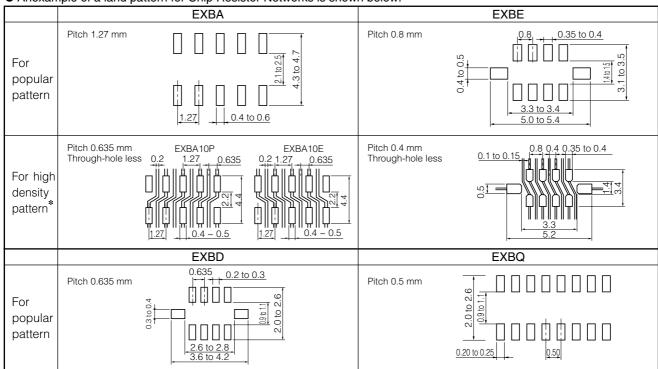


Tuno	Dimensions (mm)				
Туре	а	b	С		
ERJA1	6.4	1.70	0.60		
ERJB1	5.0	1.30	0.75		
ERJB2	3.2	0.95	0.70		
ERJB3	2.0	0.80	0.60		

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Anexample of a land pattern for Chip Resistor Networks is shown below.



* When designing high density land patterns, examine the reliability of isolation among the lines and adopt the chip resistor networks.

