PCB DESIGN PERFECTION: THE CAD LIBRARY SERIES PART 4: QFN (QUAD FLAT NO-LEAD) COMPONENTS

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ABSTRACT

This paper, the fourth in a series dedicated to CAD library quality, describes each aspect to consider when creating Quad Flat No-lead (QFN) component library parts. It also describes the impact each feature has in the PCB process.

W H I T E P A P E R

P A D S

THE UNITS

Today, 90% of all component manufacturers list their component package dimensions in metric units. Accordingly, this paper utilizes metric units for CAD library development.

THE CALCULATIONS

The examples in this document are calculated utilizing the nominal environment as defined in IPC-7351B's standard 3-tier CAD library system: See Figure 1.

1. Level A = Most – for military and medical applications.
2. Level B = Nominal – for controlled environment desktop.
3. Level C = Least – for cell phones and hand-held devices.

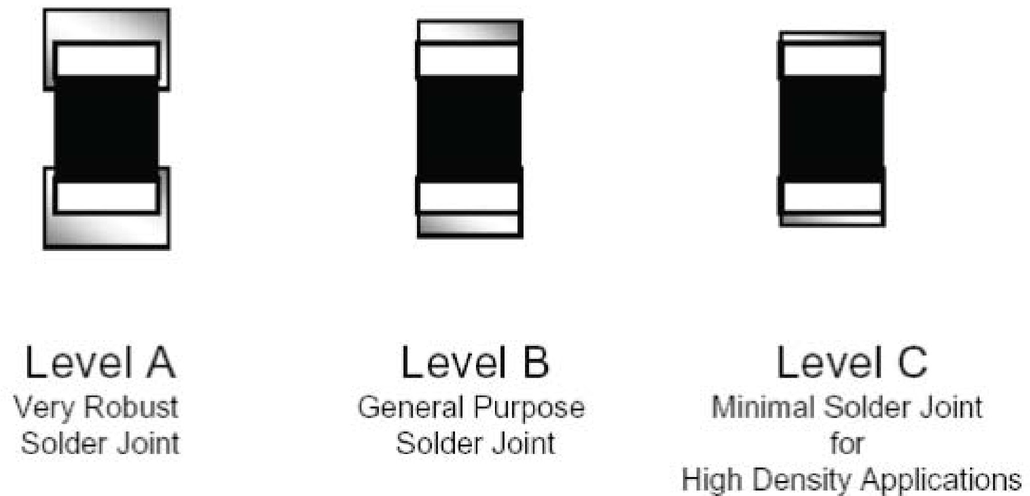

Figure 1: IPC-7351B's 3-tier solder goal density levels

QFN (QUAD FLAT NO-LEAD) COMPONENTS

The Quad Flat No-lead (QFN) component family, as shown in Figure 2, is one of the newer electronic packages to be introduced into PCB design. The QFN has pins on four edges of the bottom surface of the package. The QFN can have either a square or rectangle body as well as symmetric or asymmetric terminal patterns. The QFN with symmetric pins is only available in millimeter pin pitches of 0.8 mm, 0.65 mm, 0.5 mm, and 0.4 mm as per the standard JEDEC MO-220I.

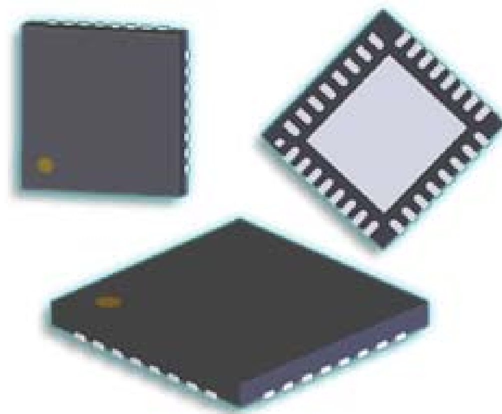

Figure 2: QFN component packages

The QFN was introduced to replace the gull-wing lead Quad Flat Package (QFP) because the component leads are embedded in the plastic and cannot be bent during handling to ensure consistent assembly attachment. The embedded lead form is also compatible with high-speed design as the die-to-lead bonding and PCB contact is much shorter. And, due to the high-speed aspect, the component generates a lot of heat. This is why most QFN packages have a thermal tab that is via-stitched to the GND planes for heat dissipation.

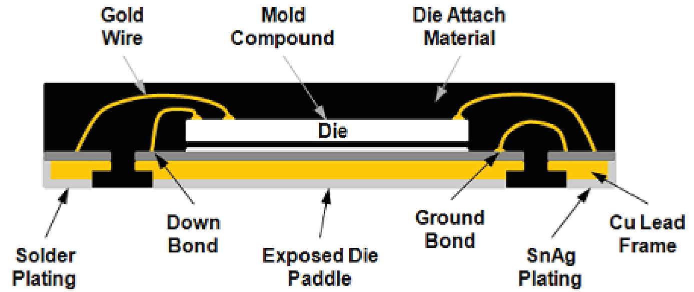

Figure 3: QFN construction cross-section

The QFN package is a CSP (plastic encapsulated package) with a copper lead frame substrate. It is also classified as a leadless package where electrical contact to the PCB is made by soldering the leads on the bottom surface of the package to the PCB, instead of the conventional formed perimeter gull-wing leads. The design of the QFN package has enhanced electrical performance that enables the standard 2 GHz frequency to be increased to 10 GHz with some design considerations.

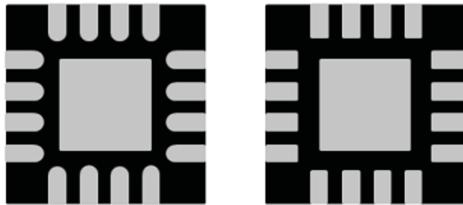

Figure 4: QFN lead styles

The QFN leads are coated with a finish that provides environmental protection and maintains solderability. See Figure 3 for a cross-section internal view of the QFN package construction. The symmetric termination leads can have either rounded or rectangle ends. See Figure 4 for the two lead styles.

The QFN uses the “Flat No-lead Edge” component lead style. See Figure 5 for a side view of the component lead. The component lead terminals are embedded in the plastic body and stick out 0.05 mm on the bottom and wrap up the component body side by 0.2 mm.

There are two types of QFN component package styles: standard and flanged. The Standard package is commonly known as the “Saw Cut” package while the Flanged type is known as “Molded Body.” See Figure 6 for the two types of component package styles.

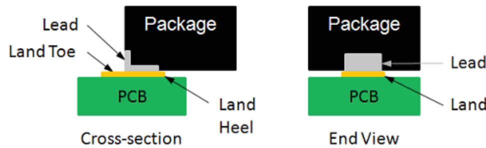

Figure 5: Flat no-lead edge terminal type

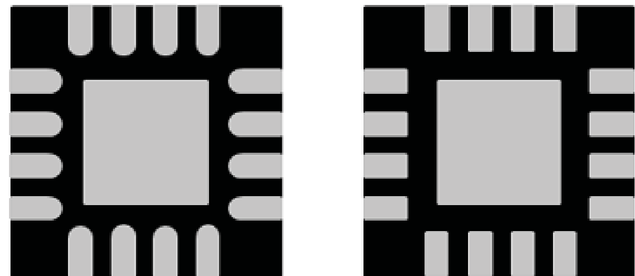

Figure 6: QFN component package styles

The thermal tab can have a chamfered corner closest to the location of Pin 1. The "Land Size" is identical to the maximum tolerance of the thermal tab size. The solder mask size is 1:1 scale of the land size. The thermal tab can also have corner radius on the other corners. See Figure 7 for an example of a thermal tab with chamfered and rounded corners.

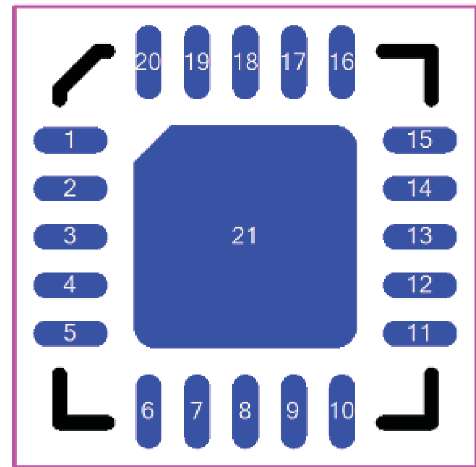

Figure 7: Thermal pad with chamfer & rounded corners

The thermal-pad paste mask size needs to be 40% - 60% of the land size and is broken up into a checkerboard pattern. The xDX Land Pattern Calculator is set to 40% paste-mask reduction by default, but the reduction percentage is user definable. The checkerboard pattern does not start until the thermal pad size exceeds 4.5 mm because the minimum paste-mask aperture opening for thermal-pad paste mask is about 1 mm square. See Figure 8 for examples of thermal-tab paste mask with a 40% reduction.

The picture on the left has a thermal pad size of 4 mm and a single paste mask of 2.5 mm. The picture on the right has a thermal pad size of 4.5 mm and a matrix of four squares of paste mask of 1.4 mm.

If there were no reduction of paste mask, the physical component would float on top of 0.15 mm of solder (the thickness of the paste mask stencil). During the reflow process users have observed that the liquidus solder lifts the device and creates a pivot point near the center of the Die Attach Pad (DAP). As the solder cools the device tends to tilt toward one side, often creating shorts in one area and opens in another.

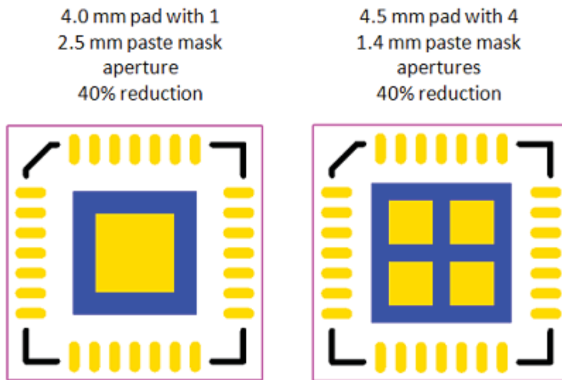

Figure 8: Thermal-pad paste mask with 40% reduction

Figure 9: Excessive thermal pad paste mask on the Die Attach Pad

By reducing the paste-mask stencil to 40% of the land size, the component will settle evenly to allow for adequate solder joints on the end termination leads. See Figure 9 for an example of excessive solder and reduced solder on the Die Attach Pad.

The primary purpose of the thermal tab is to conduct heat away from the die during operation. The best way to achieve this goal is to add stitching vias attached to the GND plane. The via hole size recommendation is 0.25 mm and should be plated, plugged, and surface finished to prevent liquidus solder from entering the holes.

Do not attempt to Tent the vias with dry-film solder mask because this will reduce the solder volume area on the pad. The via padstack is 0.5 mm pad, 0.7 mm plane clearance, 0.25 mm hole, and no thermal relief. Placing the vias on a 1 mm grid allows for two 0.1 mm trace/space routing technology on all inner layers and on the opposite side. In order to achieve the 1 mm via snap grid, the QFN must be placed on a 0.5 mm

placement grid. See Figure 10 for an example of a via matrix in a thermal pad.

Some QFN packages come in a variety of lead sizes and multiple thermal tabs. See Figures 11 thru 13 for some unique QFN variations.

Figure 11 has multiple lead lengths and “Deleted Pins.”

Figure 12 QFN has multiple thermal tabs and “Hidden Pins.” Some QFN packages have 3-5 thermal tabs with various shapes and sizes.

Figure 13 QFN has deleted pins with Pin 1 in the lower-left corner. Here, the pin order is counterclockwise, instead of in the traditional clockwise pin order.

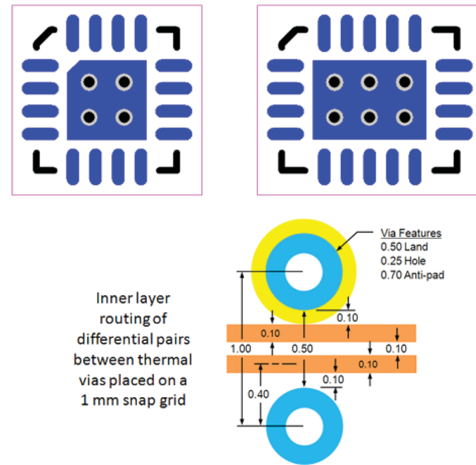

Figure 10: QFN thermal pad via stitching

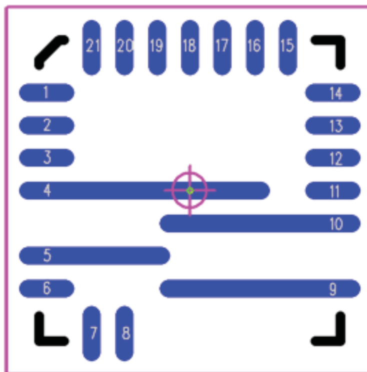

Figure 11: QFN with different lead lengths

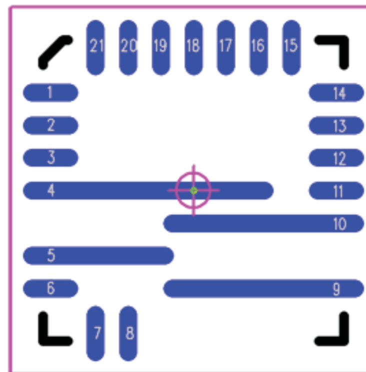

Figure 12: QFN with multiple thermal tabs and deleted pins

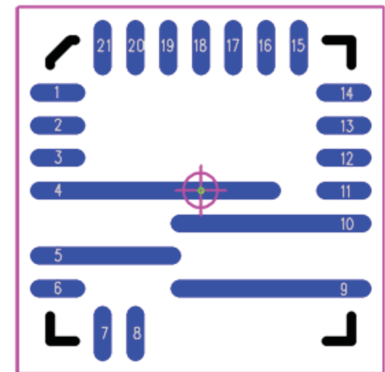

Figure 13: QFN with deleted pins. Pin 1 is in lower-left with counterclockwise pin order numbering

Figure 14 is a detailed picture of all the aspects that go into the construction of a QFN land pattern library part.

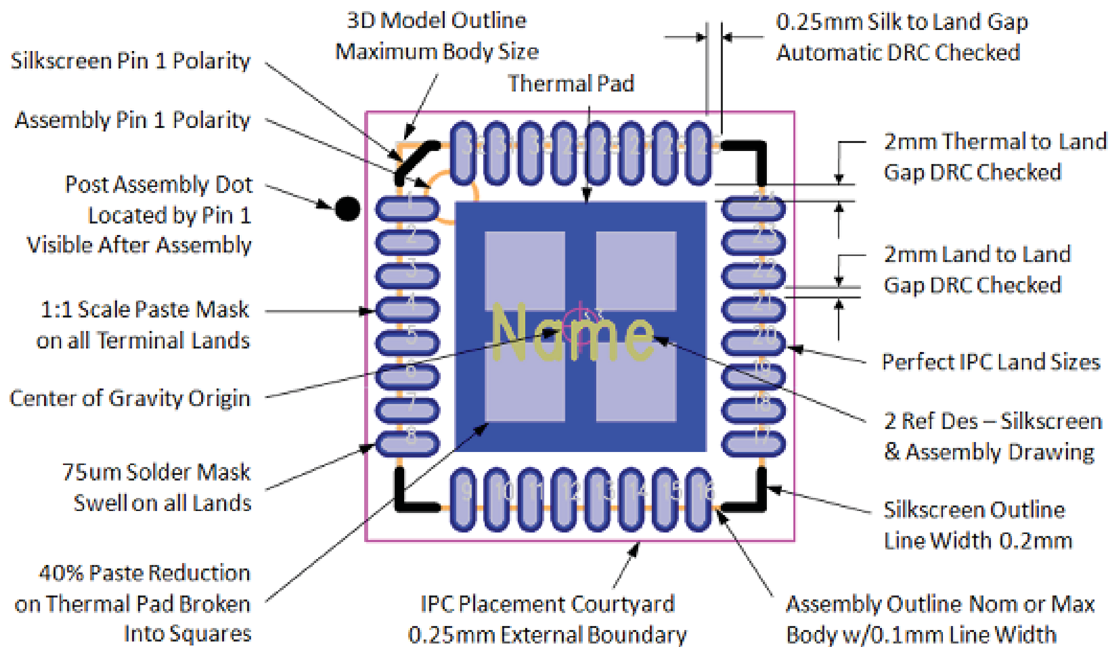

Figure 14: QFN land pattern details

The QFN component family are easily generated for all pin pitches that are on even 0.1 mm increments. These are 0.8 mm, 0.5 mm, and 0.4 mm pin pitches. SMT (Surface Mount Technology) components with a 0.65 mm pin pitch are not 100% compatible with the 0.05 mm universal grid system so we'll take a look at some via fanout solutions that help to optimize routing channels. All of the routing solutions use the identical via size (0.5 mm pad, 0.7 mm anti-pad, and 0.25 mm hole) and trace/space (0.1 mm) technology shown in Figure 10.

Figure 15 shows a 0.8 mm QFN sample via fanout and routing channel solution. This routing solution provides for one trace between vias. The red traces are on the opposite side and the green traces are the inner layer. The yellow annular ring on the via is the plane clearance. A 0.1 mm grid was used for the via fanout and trace snap grid.

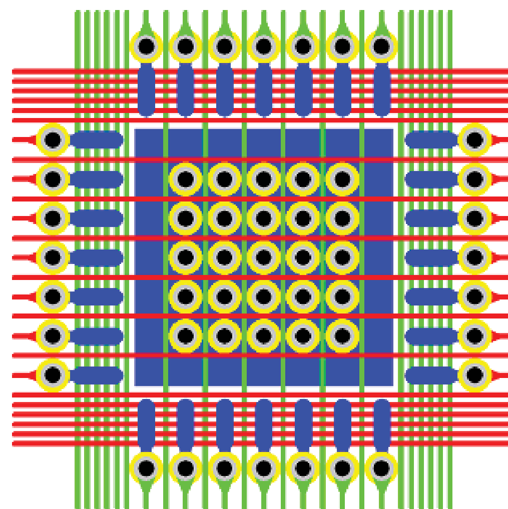

Figure 15: 0.8 mm pitch QFN via fanout and routing solution

Figure 16 is a 0.65 mm QFN via fanout and routing channel solution. The 0.65 mm pitch fanout must use a 0.05 mm grid with three traces between vias. When there is an even number of pins on each side, you have to use a 0.025 mm grid system because the components are always placed on a 0.1 mm grid system and measuring from the center of the 0.65 mm QFN to the center of the pad is 0.65 divided by 2 = 0.325 mm. This is why 0.65 mm pitch components are not optimized for the universal 0.05mm grid system.

Figure 17 shows a 0.5 mm QFN via fanout and routing channel solution. This solution provides for two traces between vias. A 0.1 mm grid was used for the via fanout and trace snap grid.

Figure 18 shows a 0.4 mm QFN via fanout and routing channel solution. This routing solution provides for one trace between vias. A 0.1 mm grid was used for the via fanout and trace snap grid.

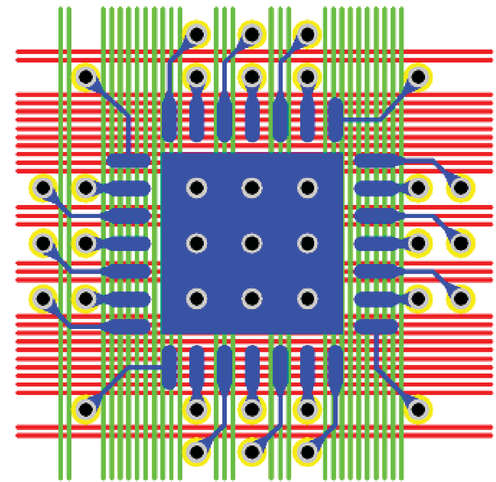

Figure 16: 0.65 mm pitch QFN via fanout & routing

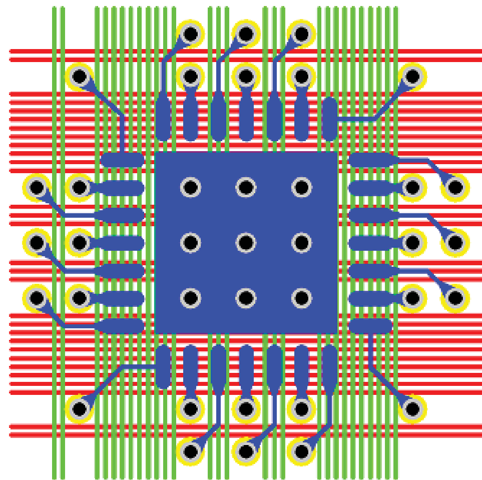

Figure 17: 0.5 mm pitch QFN via fanout & routing

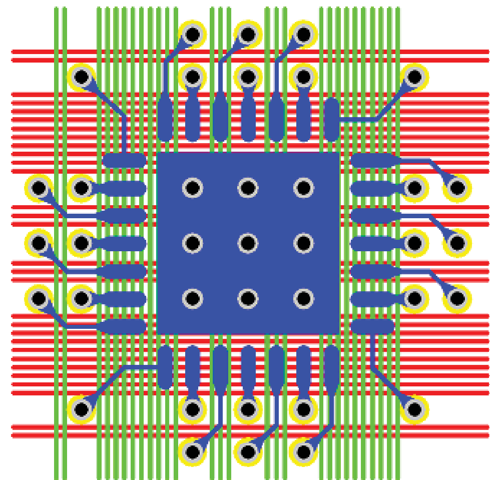

Figure 18: 0.4 mm pitch QFN via fanout & routing

CONCLUSION

When creating Quad Flat No-lead (QFN) components, every aspect of the design should be considered, including the impact that each land pattern feature has in the PCB design process.

The land pattern is the starting point that affects every process from PCB layout through PCB manufacturing and assembly. There are dozens of things to consider when creating a CAD library that are often overlooked; this paper discussed the factors to consider when creating QFN component library parts. Each factor can directly affect the quality of the part placement, via fanout, trace routing, post processing, and fabrication and assembly processes.

DID YOU KNOW?

PADS, Mentor Graphics' Personal Automated Design System, includes everything you need in order to create your component library. PADS provides a highly integrated library and component management environment that meets designers' and engineers' needs in creating and maintaining PCB design libraries.

PADS LIBRARY MANAGEMENT COMBINES:

- A starter library containing more than 10,000 ready-to-use, IPC-compliant, proven parts provided by Optimum Design Associates for a quick start to new design projects.
- Web access to component supplier data with an ability to load contents into PADS
- A central library for maintaining up-to-date design data. The central library contains all library elements in the same location, and is available at all design stages. PADS makes it possible to maintain an up-to-date library in real time, without any compilation, and includes all library elements (e.g., symbols, part data, footprints, simulation models, drawing items, and part common-property definitions).
- A component management system, integrated with schematic design and library management environments.
- A built-in consistency check of library data to make sure your library is constantly in-sync.
- Live verification of symbols placed in your schematic against the latest component and library data to eliminate costly redesigns and quality problems that might otherwise go undetected until late in the design cycle.
- A land pattern creator for quick creation of IPC-standard footprints.
- A migration path for 3rd-party libraries and component databases.

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